DOCKET

SUPREME COURT
OF THE UNITED STATES

No. 10-1219
Title: David J. Kappos, Under Secretary of Commerce for Intellectual Property and Director, Patent and Trademark Office, Petitioner

v.

Gilbert P. Hyatt

Docketed: April 7, 2011
Linked with 10A735
Lower Ct: United States Court of Appeals for the Federal Circuit
Case Nos.: (2007-1066)
Decision Date: November 8, 2010
Questions Presented

~~Date~~~	~~~~~~~Proceedings and Orders~~~~~~~~~~~~~~~~~~~~
Jan 25 2011	Application (10A735) to extend the time to file a petition for a writ of certiorari from February 6, 2011 to March 8, 2011, submitted to The Chief Justice.
Jan 26 2011	Application (10A735) granted by The Chief Justice extending the time to file until March 8, 2011.
Feb 24 2011	Application (10A735) to extend further the time to file a petition for a writ of certiorari from March 8, 2011 to April 7, 2011, submitted to The Chief Justice.
Feb 25 2011	Application (10A735) granted by The Chief Justice extending the time to file until April 7, 2011.
Apr 7 2011	Petition for a writ of certiorari filed. (Response due May 9, 2011)
May 2 2011	Order extending time to file response to petition to and including May 27, 2011.
May 27 2011	Brief of respondent Gilbert P. Hyatt in opposition filed.
Jun 6 2011	Reply of petitioner David J. Kappos, Under Secretary of Commerce for Intellectual Property and Director, Patent and Trademark Office filed.
Jun 7 2011	DISTRIBUTED for Conference of June 23, 2011.
Jun 14 2011	Supplemental brief of respondent Gilbert P. Hyatt filed. (Distributed)
Jun 17 2011	Supplemental brief of petitioner David J. Kappos, Under Secretary of Commerce for Intellectual Property and Director, Patent and Trademark Office filed. (Distributed)
Jun 27 2011	Petition GRANTED.
Jul 13 2011	The time to file the joint appendix and petitioner's brief on the merits is extended to and including August 29, 2011.
Jul 13 2011	The time to file respondent's brief on the merits is extended to and including October 17, 2011.
Aug 24 2011	Consent to the filing of amicus curiae briefs in support of either party or neither party received from counsel for the respondent.

Aug 29 2011	Joint appendix filed. (Four Volumes)
Aug 29 2011	Brief of petitioner David J. Kappos, Under Secretary of Commerce for Intellectual Property and Director, Patent and Trademark Office filed.
Sep 6 2011	Brief amici curiae of Verizon Communications Inc., et al. filed.
Sep 6 2011	Brief amici curiae of Intel Corp., et al. filed.
Sep 6 2011	Brief amicus curiae of IEEE-USA in support of neither party filed.
Sep 6 2011	Brief amicus curiae of Intellectual Property Owners Association in support of neither party filed.
Sep 6 2011	Brief amicus curiae of New York Intellectual Property Law Association in support of neither party filed.
Oct 7 2011	The time to file respondent's brief on the merits is further extended to and including October 31, 2011.
Oct 25 2011	Brief amicus curiae of American Intellectual Property Law Association filed.
Oct 31 2011	Brief of respondent Gilbert P. Hyatt filed.
Nov 14 2011	SET FOR ARGUMENT ON Monday, January 9, 2012.
Nov 15 2011	CIRCULATED.
Nov 30 2011	Reply of petitioner David J. Kappos, Under Secretary of Commerce for Intellectual Property and Director, Patent and Trademark Office filed. (Distributed)
Jan 9 2012	Argued. For petitioner: Ginger D. Anders, Assistant to the Solicitor General, Department of Justice, Washington, D. C. For respondent: Aaron M. Panner, Washington, D. C.
Apr 18 2012	Judgment is affirmed and case remanded. Thomas, J., delivered the opinion for a unanimous Court. Sotomayor, J., filed a concurring opinion, in which Breyer, J., joined.

PETITION FOR WRIT OF CERTIORARI

No. 10-1219

In the Supreme Court of the United States

DAVID J. KAPPOS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR, UNITED STATES PATENT AND TRADEMARK OFFICE, PETITIONER

v.

GILBERT P. HYATT

ON PETITION FOR A WRIT OF CERTIORARI TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

PETITION FOR A WRIT OF CERTIORARI

NEAL KUMAR KATYAL
Acting Solicitor General
Counsel of Record
TONY WEST
Assistant Attorney General
MALCOLM L. STEWART
Deputy Solicitor General
GINGER D. ANDERS
Assistant to the Solicitor General
SCOTT R. MCINTOSH
MARK R. FREEMAN
Attorneys
Department of Justice
Washington, D.C. 20530-0001
SupremeCtBriefs@usdoj.gov
(202) 514-2217

BERNARD J. KNIGHT, JR.
General Counsel
RAYMOND T. CHEN
Solicitor and Deputy General Counsel
ROBERT J. MCMANUS
THOMAS W. KRAUSE
Associate Solicitors
U.S. Patent and Trademark Office
Alexandria, Va. 22313

QUESTIONS PRESENTED

When the United States Patent and Trademark Office (PTO) denies an application for a patent, the applicant may seek judicial review of the agency's final action through either of two avenues. The applicant may obtain direct review of the agency's determination in the Federal Circuit under 35 U.S.C. 141. Alternatively, the applicant may commence a civil action against the Director of the PTO in federal district court under 35 U.S.C. 145. In a Section 145 action, the applicant may in certain circumstances introduce evidence of patentability that was not presented to the agency. The questions presented are as follows:

1. Whether the plaintiff in a Section 145 action may introduce new evidence that could have been presented to the agency in the first instance.

2. Whether, when new evidence is introduced under Section 145, the district court may decide de novo the factual questions to which the evidence pertains, without giving deference to the prior decision of the PTO.

TABLE OF CONTENTS

Page

Opinions below 1
Jurisdiction 2
Statutory provision involved 2
Statement 2
Reasons for granting the petition 10
I. The court of appeals' decision disregards fundamental principles of administrative law and departs from the prevailing understanding of Section 145's predecessor statute 11
A. The regime established by the court of appeals conflicts with established administrative-review principles 11
1. Permitting introduction of new evidence that could have been presented to the agency conflicts with administrative-exhaustion principles 13
2. Permitting de novo review of issues involving new evidence conflicts with longstanding principles of administrative deference 16
B. Before Congress reenacted R.S. 4915 as Section 145 of the 1952 Patent Act, courts in R.S. 4915 proceedings consistently limited the introduction of new evidence and applied a deferential standard of review 18
C. The district court should admit new evidence only if its proponent had no reasonable opportunity to present it to the PTO, and the Court should overturn the PTO's decision only if the evidence clearly establishes that the agency erred 23

Table of Contents—Continued: Page

II. The court of appeals' decision deviates from the decisions of the regional circuit courts 25
III. The questions presented are important 27
IV. The Court should hold this petition pending its decision in *Microsoft* 29
Conclusion 32
Appendix A – Court of appeals en banc opinion (Nov. 8, 2010) 1a
Appendix B – Court of appeals panel opinion (Aug. 11, 2009) 81a
Appendix C – District court memorandum opinion (Sept. 30, 2005) 173a
Appendix D – Opinion of the Board of Patent Appeals and Interferences (July 30, 2002) 200a
Appendix E – Decision on request for rehearing of the Board of Patent Appeals and Interferences (Jan. 23, 2003) 255a
Appendix F – Table-1 (from administrative briefing) 260a
Appendix G – Declaration of Gilbert P. Hyatt in support of opposition to motion for summary judgment (Jan. 28, 2004) 261a
Appendix H – Statutory provision 280a

TABLE OF AUTHORITIES

Cases:

American Hoist & Derrick Co. v. *Sowa & Sons, Inc.*, 725 F.2d 1350 (Fed. Cir.), cert. denied, 469 U.S. 821 (1984) 24, 25, 30
Barrett Co. v. *Koppers Co.*, 22 F.2d 395 (3d Cir. 1927) 21, 26

Cases—Continued: Page

Beard v. *Burts*, 95 U.S. 434 (1877) 19
Boucher Inventions, Ltd. v. *Sola Elec. Co.*, 131 F.2d 225 (D.C. Cir. 1942) 21
Bryan v. *United States*, 524 U.S. 184 (1998) 23
Butterworth v. *United States ex rel. Hoe*, 112 U.S. 50 (1884) 18, 21
California Research Corp. v. *Ladd*, 356 F.2d 815 (D.C. Cir. 1966) 25
Chandler v. *Roudebush*, 425 U.S. 840 (1976) 8, 15, 16
Citizens to Preserve Overton Park, Inc. v. *Volpe*, 401 U.S. 402 (1971) 13
Consolo v. *Federal Mar. Comm'n*, 383 U.S. 607 (1966) 16
Cordis Corp. v. *Boston Scientific Corp.*, 561 F.3d 1319 (Fed. Cir.), cert. denied, 130 S. Ct. 748, and 130 S. Ct. 749 (2009) 3, 17
DeSeversky v. *Brenner*, 424 F.2d 857 (D.C. Cir. 1970) 25, 26
Dickinson v. *Zurko*, 527 U.S. 150 (1999) 4, 9, 12, 18, 23, 27
Dowling v. *Jones*, 67 F.2d 537 (2d Cir. 1933) 22, 26
ExxonMobil Chem. Patents Inc. v. *Godici*, No. Civ.A. 01-00377, 2002 WL 34233002 (D.D.C. Feb. 12, 2002) 24
Florida Power & Light Co. v. *Lorion*, 470 U.S. 729 (1985) 13, 17, 24
Forest Grove Sch. Dist. v. *T.A.*, 129 S. Ct. 2484 (2009) ... 22
Gandy v. *Marble*, 122 U.S. 432 (1887) 21

Cases—Continued: Page

Globe-Union, Inc. v. *Chicago Tel. Supply Co.*, 103 F.2d 722 (7th Cir. 1939) 21, 22, 23, 26
Graham v. *John Deere Co.*, 383 U.S. 1 (1966) 3
Greene v. *Beidler*, 58 F.2d 207 (2d Cir. 1932) 21
Hien, In re, 166 U.S. 432 (1897) 21
Hoover Co. v. *Coe*, 325 U.S. 79 (1945) 4, 5, 18, 21
INS v. *Orlando Ventura*, 537 U.S. 12 (2002) 17
Kelly v. *Robinson*, 479 U.S. 36 (1986) 23
Lorillard v. *Pons*, 434 U.S. 575 (1978) 22
McCarthy v. *Madigan*, 503 U.S. 140 (1992) 13
McKart v. *United States*, 395 U.S. 185 (1969) 13, 24
Minnesota Mining & Mfg. Co. v. *Carborundum Co.*, 155 F.2d 746 (3d Cir. 1946) 22, 26
Morgan v. *Daniels*, 153 U.S. 120 (1894) ..... *passim*
Nichols v. *Minnesota Mining & Mfg. Co.*, 109 F.2d 162 (4th Cir. 1940) 22, 26
Pfaff v. *Wells Elecs., Inc.*, 525 U.S. 55 (1998) 27
Schering Corp. v. *Marzall*, 101 F. Supp. 571 (D.D.C. 1951) 21
Schilling v. *Schwitzer-Cummins Co.*, 142 F.2d 82 (D.C. Cir. 1944) 21, 22, 26
Scotten v. *Littlefield*, 235 U.S. 407 (1914) 19
Southard v. *Russell*, 57 U.S. (16 How.) 547 (1854) 20
Squire, In re, 22 F. Cas. 1015 (C.C.E.D. Mo. 1877) 21
Tagg Bros. & Moorhead v. *United States*, 280 U.S. 420 (1930) 13, 16

Cases—Continued: Page

Takeda Pharm. Co. v. *Dudas*, 511 F. Supp. 2d 81 (D.D.C. 2007), vacated on other grounds, 561 F.3d 1372 (Fed. Cir. 2009) 18

United States v. *Carlo Bianchi & Co.*, 373 U.S. 709 (1963) 14, 16

Western Elec. Co. v. *Fowler*, 177 F. 224 (7th Cir. 1910) 21

Statutes and regulations:

Act of Mar. 3, 1839, ch. 88, § 10, 5 Stat. 354 4

Act of Mar. 2, 1927, ch. 273, § 8, 44 Stat. 1336 5

Administrative Procedure Act, 5 U.S.C. 701 *et seq.* 4

Civil Rights Act of 1964, Tit. VII, 42 U.S.C. 2000e *et seq.* 15

Patent Act of 1836, ch. 357, § 16, 5 Stat. 123 4

Rev. Stat. § 4915 (1878) ..... *passim*

35 U.S.C. 2(a)(1) 2

35 U.S.C. 6 (2006 & Supp. III 2009) 3

35 U.S.C. 6(a) (Supp. III 2009) 3

35 U.S.C. 101 2

35 U.S.C. 101-103 27

35 U.S.C. 102 2

35 U.S.C. 103(a) 2

35 U.S.C. 112 ..... 3, 6, 27

35 U.S.C. 120 3

35 U.S.C. 131 2

35 U.S.C. 132(a) 5

35 U.S.C. 134 3

Statutes and regulations—Continued: Page

35 U.S.C. 135 5
35 U.S.C. 141-145 3
35 U.S.C. 141 ..... 4, 12, 25, 28
35 U.S.C. 144 4
35 U.S.C. 145 ..... *passim*
35 U.S.C. 146 5
37 C.F.R.:
Section 1.2 24
Section 1.53(b) 3, 15
Section 1.105(a)(1) 5
Section 1.114 ..... 3, 15
Section 41.33(d)(1) 14
Section 41.37(c)(1)(vii) 7, 14
Section 41.39(b)(1) 14
Section 41.50(a)(2)(i) 14
Section 41.50(b)(1) 14
Section 41.52 3

Miscellaneous:

Monte Cooper & Robert M. Isackson, *The Fed. Circ. Stance in* Hyatt v. Kappos, http://www.law360.com/ip/articles/211544 (Dec. 3, 2010) 28
David J. Muzilla, *Patent Stalled at the USPTO? Consider Presenting New Evidence in Federal District Court*, http://www.hahnlaw.com/references/73542574-85f1-4e77-b7aa-1094244516b1.pdf (2011) 28
S. Rep. No. 1979, 82d Cong., 2d Sess. (1952) 5, 22

Miscellaneous—Continued: Page

Benjamin J. Shipman, *Handbook of the Law of Equity Pleading* (1897) 20

Thomas Atkins Street, *Federal Equity Practice* (1909) 20

U.S. Patent & Trademark Office, U.S. Dep't of Commerce, *Manual of Patent Examining Procedure* (8th ed. Rev. 8, July 2010) 2

In the Supreme Court of the United States

No. 10-1219

DAVID J. KAPPOS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR, UNITED STATES PATENT AND TRADEMARK OFFICE, PETITIONER

v.

GILBERT P. HYATT

ON PETITION FOR A WRIT OF CERTIORARI TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

PETITION FOR A WRIT OF CERTIORARI

The Acting Solicitor General, on behalf of the Director of the United States Patent and Trademark Office (PTO), respectfully petitions for a writ of certiorari to review the judgment of the United States Court of Appeals for the Federal Circuit in this case.

OPINIONS BELOW

The opinion of the en banc court of appeals (App., *infra*, 1a-80a) is reported at 625 F.3d 1320. The opinion of the court of appeals panel (App., *infra*, 81a-172a) is reported at 576 F.3d 1246. The opinion of the district court (App., *infra*, 173a-199a) is unreported. The order of the Board of Patent Appeals and Interferences (App., *infra*, 200a-254a) is unreported.

JURISDICTION

The judgment of the court of appeals was entered on November 8, 2010. On January 26, 2011, the Chief Justice extended the time in which to file a petition for a writ of certiorari to and including March 8, 2011. On February 25, 2011, the Chief Justice further extended the time to and including April 7, 2011. The jurisdiction of this Court is invoked under 28 U.S.C. 1254(1).

STATUTORY PROVISION INVOLVED

The pertinent statutory provision is reprinted in the appendix to this petition (App., *infra*, 280a).

STATEMENT

1. a. The PTO is the agency "responsible for the granting and issuing of patents." 35 U.S.C. 2(a)(1). When an inventor applies for a patent, the PTO undertakes an examination process to determine whether a patent should issue. 35 U.S.C. 131. An examiner with expertise in the relevant technological fields analyzes the application and the invention it describes, as well as the prior art in the field, in order to determine whether the statutory requirements for patentability are satisfied. *Ibid.*; PTO, U.S. Dep't of Commerce, *Manual of Patent Examining Procedure* §§ 704-706, 903.08(e), 904-904.02 (8th ed. Rev. 8, July 2010).

A number of statutory prerequisites must be satisfied before a patent may issue. *Inter alia*, an invention must consist of patent-eligible subject matter, 35 U.S.C. 101; and it must be novel, see 35 U.S.C. 102, and non-obvious, 35 U.S.C. 103(a). The patent's specification must contain a written description of the invention "and of the manner and process of making and using it," and it must enable a person of ordinary skill in the art to

"make and use the same." 35 U.S.C. 112. In applying those requirements, the PTO may make a number of factual determinations regarding, *inter alia*, the nature of the invention's advancement over existing technology, the level of ordinary skill in the art, and the way in which a person of ordinary skill would understand the patent's specification. See, *e.g.*, *Graham* v. *John Deere Co.*, 383 U.S. 1, 17 (1966). Certain patentability requirements, such as whether the claims are supported by adequate written description, see 35 U.S.C. 112, are pure questions of fact. See *Cordis Corp.* v. *Boston Scientific Corp.*, 561 F.3d 1319, 1331-1332, 1335 (Fed. Cir.), cert. denied, 130 S. Ct. 748, and 130 S. Ct. 749 (2009).

If the examiner denies a patent application, the applicant may appeal the decision to the PTO's Board of Patent Appeals and Interferences (Board). See 35 U.S.C. 6 (2006 & Supp. III 2009); 35 U.S.C. 134. The Board is composed of "administrative patent judges" who possess "competent legal knowledge and scientific ability." 35 U.S.C. 6(a) (Supp. III 2009). An applicant who believes the Board's decision is erroneous may file a request for Board rehearing. 37 C.F.R. 41.52. Alternatively, an applicant who wishes to overcome the Board's decision by introducing new evidence of patentability before the PTO may file a request for continued examination, 37 C.F.R. 1.114, or a continuation application, 37 C.F.R. 1.53(b); see also 35 U.S.C. 120. In either case, the examiner considers the application in light of the new evidence, and the applicant may appeal the examiner's decision to the Board.

b. An applicant aggrieved by the Board's final determination may obtain judicial review through either of two avenues. 35 U.S.C. 141-145. The applicant may directly "appeal the decision to the United States Court of

Appeals for the Federal Circuit," 35 U.S.C. 141, which "review[s] the [Board's] decision * * * on the record before the [PTO]," 35 U.S.C. 144. In Section 141 proceedings, the Federal Circuit reviews the PTO's decision under the deferential standards that govern judicial review of final agency action under the Administrative Procedure Act (APA), 5 U.S.C. 701 *et seq.* See *Dickinson* v. *Zurko*, 527 U.S. 150, 154-165 (1999).

Alternatively, an unsuccessful applicant may "have remedy by civil action against the Director" of the PTO in the District Court for the District of Columbia. 35 U.S.C. 145. In such an action, the "court may adjudge that such applicant is entitled to receive a patent for his invention, as specified in any of his claims involved in the decision of the [Board], as the facts in the case may appear." *Ibid.* This Court has observed that, in some circumstances, Section 145 "permits the disappointed applicant to present to the court evidence that the applicant did not present to the PTO," which "makes a factfinder of the district judge." *Zurko*, 527 U.S. at 164. The Court in *Zurko* did not, however, address the circumstances in which new evidence may be admitted in a Section 145 suit. See *ibid.*

c. Section 145 is the current embodiment of a statutory provision that has authorized judicial review of PTO (or Patent Office) decisions in district court since 1836, when Congress first created an agency responsible for the examination of patents. Patent Act of 1836, ch. 357, § 16, 5 Stat. 123. See generally *Hoover Co.* v. *Coe*, 325 U.S. 79, 84-87 (1945). Eventually codified at Rev. Stat. § 4915 (1878) (R.S. 4915), the provision permitted an action (called a "bill in equity") to obtain review of "all cases where patents are refused for any reason whatever," Act of Mar. 3, 1839, ch. 88, § 10, 5 Stat. 354, in-

cluding both patent denials and priority determinations made after "interference" proceedings, see 35 U.S.C. 135.

Until 1927, an unsuccessful patent applicant could file a bill in equity in district court under R.S. 4915 only after obtaining initial judicial review in the courts of the District of Columbia. See *Hoover Co.*, 325 U.S. at 85-86; App., *infra*, 97a-101a. In 1927, Congress amended the statutory scheme to permit a disappointed applicant to "have the decision of the Patent Office reviewed either by the court of appeals or by filing a bill in equity, but not both." *Hoover Co.*, 325 U.S. at 87 (citation omitted); see Act of Mar. 2, 1927, ch. 273, § 8, 44 Stat. 1336. In the 1952 Patent Act, Congress divided R.S. 4915 into two sections—Section 145, governing *ex parte* proceedings, and Section 146, governing interferences—and indicated that "no fundamental change" was intended "in the various appeals and other review of Patent Office action." S. Rep. No. 1979, 82d Cong., 2d Sess. 7 (1952).

2. a. Respondent is the named inventor of the invention disclosed in the patent application at issue in this case, known as the '702 application. App., *infra*, 3a. The invention relates generally to a computerized display system for processing image information. *Ibid.*

Respondent filed the '702 application in 1995. After a series of amendments, he deleted the original claims in the application and presented 117 new claims for examination. App., *infra*, 177a; C.A. App. A11009-A11087. Concerned that the amendment was not supported by the original application, see 35 U.S.C. 132(a) (barring amendments introducing "new matter"), the PTO examiner directed respondent to "point out where in the specification support may be found" for the new claims. C.A. App. A10493; see 37 C.F.R. 1.105(a)(1). Finding respon-

dent's submission insufficiently specific, the examiner rejected all 117 claims under 35 U.S.C. 112 for lack of an adequate written description. App., *infra*, 4a.

b. Respondent appealed to the Board. The Board noted that respondent's appellate submission did not identify any support in the specification for the rejected claims beyond a table showing where certain terms appeared in the specification. See App., *infra*, 213a, 218a-219a; see also *id.* at 260a. Stating that "merely pointing to isolated words scattered throughout the specification does not describe the invention claimed as a combination of elements, functions, and interconnections, anymore than a dictionary provides written description support for a book where words are used in combination to provide a certain meaning," the Board concluded that respondent had failed to refute the examiner's findings under Section 112. *Id.* at 213a. The Board nevertheless conducted its own search of the specification for supporting disclosures. *Id.* at 219a-240a; see *id.* at 257a ("This panel spent three weeks considering the 238 page specification, the 42 drawing figures, the 128 page appeal brief, and the 64 page reply brief as applied to 54 independent claims and 63 dependent claims in writing our original decision."). The Board ultimately found adequate support for 38 claims, but affirmed the examiner's rejection of 79 claims for lack of written description.[1] *Id.* at 252a-253a.

Respondent filed a request for rehearing before the Board and offered, for the first time, claim-by-claim responses to the examiner's written-description rejections. See App., *infra*, 257a. The Board denied reconsidera-

---

[1] The Board reversed the examiner's rejections based on obviousness, anticipation, and other grounds not at issue here. App., *infra*, 5a.

tion, explaining that under PTO rules, respondent had forfeited his written-description arguments by failing to present them in his appeal brief. *Id.* at 256a; see 37 C.F.R. 41.37(c)(1)(vii) (arguments not presented to the Board in appeal briefs are waived).

3. Respondent sought judicial review of the PTO's decision in federal district court under 35 U.S.C. 145. The Director moved for summary judgment, arguing that the Board's findings on the written-description issue were supported by substantial evidence in the record. App., *infra*, 6a. In response, respondent submitted his own written declaration, in which he identified portions of the specification that, in his view, supported the claims held invalid by the Board. *Ibid.*; see *id.* at 261a-279a. The Director urged the district court not to consider the declaration because respondent had failed, without reasonable excuse, to provide the same information to the agency.

The district court excluded respondent's declaration, concluding that Section 145 does not permit a plaintiff to introduce new evidence that he had a reasonable opportunity to present to the PTO during the administrative process. App., *infra*, 173a-199a. Finding no basis in the administrative record for disturbing the Board's findings, the court granted summary judgment to the Director. *Id.* at 190a-199a.

4. A panel of the court of appeals affirmed. App., *infra*, 81a-172a. The panel explained that Congress could not reasonably have intended "to allow a patent applicant in a § 145 action to introduce new evidence with no regard whatsoever as to his conduct before the PTO." *Id.* at 146a. The panel emphasized that "it has been the general practice of federal courts for over eighty years in certain circumstances to exclude evi-

dence which a party could and should have introduced before the Patent Office but did not despite an obligation to do so." *Id.* at 121a. Judge Moore dissented. *Id.* at 149a-172a.

5. a. The court of appeals granted rehearing en banc and reversed the district court's grant of summary judgment. The en banc court held that Section 145 permits patent applicants to challenge the Board's determination based on any evidence admissible under the Federal Rules of Evidence, even if the applicant had no justification for failing to provide the evidence to the agency. App., *infra*, 21a. The court stated that Section 145 "provides no indication that this civil action is somehow different from a customary civil action," *id.* at 11a-12a, and that "[w]here [a] statute permits a 'civil action' in relation to agency actions, the Supreme Court has held that this amounts to a trial de novo," *id.* at 30a (citing *Chandler* v. *Roudebush*, 425 U.S. 840 (1976)). The court also relied on testimony by witnesses during congressional hearings preceding the 1927 revisions to the Patent Act, in which opponents of R.S. 4915 characterized the provision as permitting a "de novo" proceeding in district court. See App., *infra*, 14a-17a. The court viewed that testimony as indicating that Congress understood R.S. 4915 to "allow[] an applicant to introduce new evidence in district court, regardless of whether that evidence had been provided to the Patent Office in earlier proceedings." *Id.* at 17a.

The court of appeals further held that "once an applicant introduces new evidence on an issue, the district court reviews that issue de novo," App., *infra*, 2a, and makes "de novo fact findings if the evidence conflicts with any related [PTO] finding," *id.* at 32a. In the court's view, permitting de novo review when new evi-

dence is introduced does not conflict with "principles of deference to agency fact finding" because a deferential "court/agency standard of review" applies when the applicant does not offer new evidence. *Id.* at 31a; see *id.* at 30a. The court also noted that a district court may consider "the proceedings before and findings of the Patent Office in deciding what weight to afford an applicant's newly admitted evidence." *Id.* at 28a. The en banc court accordingly vacated the district court's grant of summary judgment to the PTO, and remanded for further proceedings. *Id.* at 34a-35a.

b. Judge Newman concurred in part and dissented in part. App., *infra*, 36a-43a. She agreed with the majority that Section 145 authorizes the admission of new evidence without regard to the applicant's conduct before the PTO, but she would have held that Section 145 authorizes de novo review even when the applicant does not introduce new evidence. *Id.* at 38a.

c. Judge Dyk, joined by Judge Gajarsa, dissented. App., *infra*, 44a-80a. The dissenting judges described the en banc court's decision as "a remarkable departure from settled principles of administrative law" and "yet another misguided effort to craft special rules for patent cases that the Supreme Court in other cases has held to be impermissible." *Id.* at 44a, 46a (citing *Zurko*, 527 U.S. at 152). They emphasized that courts historically had limited the admissibility of new evidence in Section 145 proceedings, and that Congress has often provided for deferential review in civil actions brought in district court. *Id.* at 53a-78a. They would have held that Section 145 does not permit a disappointed patent applicant to introduce new evidence that could have been submitted to the PTO. *Id.* at 51a-52a. In the dissenting judges' view, "[t]he majority opinion invites applicants to delib-

infringement suit asserts that the relevant patent is invalid based on evidence that the PTO did not consider in the examination process. Like a defendant who challenges the validity of a patent in infringement litigation, a Section 145 plaintiff seeks to overturn the PTO's disposition of a patent application, and principles of administrative deference should inform the nature and scope of judicial review in both contexts. See *Morgan*, 153 U.S. at 123-124. It would therefore be appropriate in the first instance to hold this petition pending the Court's decision in *Microsoft*.

I. THE COURT OF APPEALS' DECISION DISREGARDS FUNDAMENTAL PRINCIPLES OF ADMINISTRATIVE LAW AND DEPARTS FROM THE PREVAILING UNDERSTANDING OF SECTION 145'S PREDECESSOR STATUTE

A. The Regime Established By The Court Of Appeals Conflicts With Established Administrative-Review Principles

Section 145 permits a patent applicant "dissatisfied with the decision" of the PTO to seek a "remedy by civil action against the Director" in district court. 35 U.S.C. 145. More than a century ago, this Court held that a suit under Section 145's predecessor, R.S. 4915, is not a free-standing cause of action to obtain a patent, but is rather "an application to the court to set aside the action of one of the executive departments of the government." *Morgan*, 153 U.S. at 124. Because the decision to deny a patent or award priority is made by "[t]he one charged with the administration of the patent system" after "finish[ing] its investigations and ma[king] its determination," *ibid.*, the agency's determination should be overturned only if its error "is established by testimony which in character and amount carries thorough convic-

tion." *Id.* at 125. When the evidence is "doubtful, the decision of the Patent Office must control." *Ibid.* Consistent with those principles, this Court has held that when a disappointed patent applicant challenges the PTO's denial through a direct appeal under Section 141, the PTO's decision is final agency action that must be reviewed under the APA's deferential standards. See *Dickinson* v. *Zurko*, 527 U.S. 150, 154-165 (1999).

In the en banc court of appeals' view, the fact that the plaintiff in a Section 145 suit is sometimes permitted to introduce new evidence "distinguishes a civil action under § 145 from an appeal" in which a deferential standard of review would be appropriate. App., *infra*, 2a. That analysis is misconceived. To be sure, the potential for introduction of new evidence in a Section 145 suit reflects a limited exception to the usual rule that judicial review of agency action is confined to the administrative record. That limited exception, however, does not alter the fundamental character of a Section 145 suit as a request to set aside the decision of an expert agency made within the scope of its delegated authority. Nor does it justify the en banc court's wholesale disregard of other background principles that govern judicial review of agency action. Those principles counsel that, even when judicial review is conducted under a statutory provision that does not wholly bar the introduction of new evidence, the plaintiff must first present his evidence to the agency when that opportunity is reasonably available, and the court's review must reflect appropriate deference to the agency's expertise and statutory authority.

1. Permitting introduction of new evidence that could have been presented to the agency conflicts with administrative-exhaustion principles

Ordinarily, an applicant before an agency must provide a complete presentation of his arguments and evidence, thereby affording the agency a full opportunity to apply its judgment and expertise to the issues at hand, before seeking judicial review of the agency's decision. *McKart* v. *United States*, 395 U.S. 185, 193 (1969); see *Citizens to Preserve Overton Park, Inc.* v. *Volpe*, 401 U.S. 402, 413-414 (1971). Judicial review then takes place using the existing administrative record, and when material new evidence bearing on the agency's determination is brought to the court's attention, the proper course is generally "to remand to the agency for additional investigation or explanation." *Florida Power & Light Co.* v. *Lorion*, 470 U.S. 729, 744 (1985); see *Tagg Bros. & Moorhead* v. *United States*, 280 U.S. 420, 445 (1930). The requirement of administrative exhaustion permits the agency to "develop the necessary factual background upon which decisions should be based" and gives the agency the opportunity to "apply[] a statute in the first instance." *McKart*, 395 U.S. at 193-194; see *McCarthy* v. *Madigan*, 503 U.S. 140, 145 (1992) (Exhaustion concerns have "particular force * * * when the agency proceedings in question allow the agency to apply its special expertise."). The exhaustion requirement also ensures that the agency is "given a chance to discover and correct its own errors" and prevents "frequent and deliberate flouting of administrative processes." *McKart*, 395 U.S. at 195.

Contrary to the court of appeals' view, those rationales are not rendered inapposite simply because Section 145 does not wholly preclude the introduction of

new evidence. Section 145 provides a safety valve in the situations where a disappointed patent applicant had no reasonable opportunity to present particular relevant evidence to the PTO. With respect to evidence that *could* have been submitted to the agency, however, the reasons for treating exhaustion as a prerequisite to consideration of the evidence by a reviewing court apply with full force here. Congress conferred patent examination authority on the PTO, and it required that examiners and Board judges have extensive technical expertise. As applied in this setting, exhaustion principles serve their usual purpose of protecting the expert agency's ability to consider the full range of relevant information and to correct any errors that may occur at lower levels of the administrative process.

The court of appeals disregarded these principles by creating a regime in which a patent applicant may purposefully withhold relevant evidence from the PTO in order to present that evidence to a non-expert judge, who then must evaluate the evidence without the benefit of the agency's expert judgment. That system undermines Congress's decision to entrust the issuance of patents to an expert agency. See *United States* v. *Carlo Bianchi & Co.*, 373 U.S. 709, 717 (1963) (Congress's purpose "would be frustrated if either side were free to withhold evidence at the administrative level and then introduce it in a judicial proceeding."). It also hinders the PTO's effectiveness by excusing violations of the PTO's own rules of practice. Those rules provide that arguments not timely presented to the Board are forfeited, see 37 C.F.R. 41.37(c)(1)(vii), and they limit the circumstances in which new evidence may be submitted after an appeal has been taken, see 37 C.F.R. 41.33(d)(1); see also 37 C.F.R. 41.39(b)(1), 41.50(a)(2)(i)

and (b)(1). Moreover, the PTO's procedures permit applicants who have received an adverse Board decision to introduce new evidence of patentability to the PTO before seeking judicial review, by filing a request for continued examination or a continuation application. See 37 C.F.R. 1.53(b), 1.114. When these procedures are available, they provide applicants with a means of alerting the PTO to new evidence and persuading the agency to correct its errors without resorting to judicial review. Exhaustion principles are disserved if applicants are encouraged to bypass the agency's examination procedures in favor of district-court review.

Relying on *Chandler* v. *Roudebush*, 425 U.S. 840 (1976), the court of appeals stated that "[w]here the statute permits a 'civil action' in relation to agency actions, the Supreme Court has held that this amounts to a trial de novo" in which "the admission of new evidence" is "subject only to the Federal Rules of Evidence and Civil Procedure." App., *infra*, 30a. The en banc court's reliance on *Chandler* was misplaced. The Court in *Chandler* held that Title VII of the Civil Rights Act of 1964, 42 U.S.C. 2000e *et seq.*, conferred on federal employees the right to "trials *de novo*" on their discrimination claims, rather than simply to "'substantial evidence' review" of "administrative dispositions of federal employee discrimination complaints." 425 U.S. at 863. As the dissent below explained, however, the Court did not base that conclusion on the statute's use of the term "civil action" standing alone. Rather, the Court relied on the facts that Title VII gave federal workers the *same* right as private-sector employees to file suit alleging unlawful employment discrimination, and that private-sector employees had an unquestioned right to

trial de novo. See *id.* at 844-846, 863; App., *infra*, 59a-60a (distinguishing *Chandler*).

The PTO's disposition of patent applications, by contrast, has no private-sector analogue, and the en banc court identified no structural feature of the Patent Act (beyond Section 145's use of the term "civil action") suggesting an exception to usual exhaustion principles. The mere fact that Section 145 provides for review in district court rather than in a court of appeals does not render those principles inapplicable. See *Carlo Bianchi & Co.*, 373 U.S. at 715 (stating that "the function of reviewing an administrative decision can be and frequently is performed by a court of original jurisdiction as well as by an appellate tribunal"). This Court's decisions further establish that, absent evidence of contrary congressional intent, see pp. 22-23, *infra*, a statute authorizing a civil suit in district court to challenge an agency's action should not be interpreted to permit a plenary proceeding involving the unrestricted introduction of new evidence. *Ibid.*; *Tagg Bros. & Moorhead*, 280 U.S. at 443-445; see, *e.g.*, *Consolo* v. *Federal Mar. Comm'n*, 383 U.S. 607, 619 n.17 (1966).

2. ***Permitting de novo review of issues involving new evidence conflicts with longstanding principles of administrative deference***

Having allowed respondent to introduce new evidence that could have been presented to the PTO, the court of appeals compounded its error by directing the district court to "make de novo fact findings with respect to factual issues to which the new evidence relates." App., *infra*, 31a. That holding conflicts with the longstanding rule that a court reviewing an agency's conclusions "is not generally empowered to conduct a *de*

novo inquiry into the matter being reviewed and to reach its own conclusions based on such an inquiry." *Lorion*, 470 U.S. at 744; see *INS* v. *Orlando Ventura*, 537 U.S. 12, 16 (2002) (per curiam). Because most questions of patentability are "either entirely factual or ha[ve] factual components," see App., *infra*, 47a (Dyk, J., dissenting), the en banc court's approach permits the district court to substitute its judgment for that of the PTO not only on subsidiary factual issues where the new "evidence conflicts with any related Patent Office finding," *id.* at 32a, but also on ultimate questions of patentability such as anticipation or the adequacy of the written description, both of which are questions of fact. See *Cordis Corp.* v. *Boston Scientific Corp.*, 561 F.3d 1319, 1331-1332, 1335 (Fed. Cir.), cert. denied, 130 S. Ct. 748, and 130 S. Ct. 749 (2009).

The en banc court of appeals viewed its approach as consistent with "principles of deference to agency fact finding" because the court would apply de novo review only "[w]hen new evidence is introduced" and would apply the deferential APA standard "when no party introduces new evidence." App., *infra*, 31a-32a. In fact, that two-tiered approach exacerbates the ill effects of the court's erroneous determination that the plaintiff in a Section 145 suit may introduce new evidence that he failed without cause to present during the administrative proceedings. By holding that a more plaintiff-friendly standard of review applies in new-evidence cases, even when the plaintiff had a reasonable opportunity to present the relevant information to the agency, the en banc court of appeals created an affirmative incentive for patent applicants to withhold relevant evidence from the PTO in order to improve their chances of success in court. And as the dissenting judges recog-

nized, that incentive will be especially strong "in those circumstances where an expert agency would reject the evidence but a non-expert district court might be convinced to accept it." *Id.* at 80a.[2]

B. Before Congress Reenacted R.S. 4915 As Section 145 Of The 1952 Patent Act, Courts In R.S. 4915 Proceedings Consistently Limited The Introduction Of New Evidence And Applied A Deferential Standard Of Review

The court of appeals believed that its approach was justified because Section 145's predecessor (R.S. 4915) had been construed to permit the district court to consider evidence beyond the administrative record. App., *infra*, 12a-21a; see *Zurko*, 527 U.S. at 164; *Hoover Co.* v. *Coe*, 325 U.S. 79, 83 (1945) (evidence "may include evidence not presented in the Patent Office"); *Butterworth* v. *United States ex rel. Hoe*, 112 U.S. 50, 61 (1884) (same). The en banc court's analysis reflects a misunderstanding of the manner in which suits of this nature were traditionally adjudicated. Although the admission of new evidence in R.S. 4915 proceedings was not categorically prohibited, courts adjudicating such actions in the early twentieth century recognized that the provision should be construed in light of administrative-law principles, and they routinely excluded evidence that

---

[2] Although the Federal Circuit had previously held that de novo review is appropriate when new evidence is admitted, App., *infra*, 31a, the decision below exacerbates the adverse consequences of those prior holdings and threatens to render de novo review the rule rather than the exception. Until the decision of the en banc court below, the practical effect of the availability of de novo review was substantially limited by district courts' consistent practice of excluding evidence that could have been presented to the PTO. See, *e.g.*, *Takeda Pharm. Co.* v. *Dudas*, 511 F. Supp. 2d 81, 87 (D.D.C. 2007), vacated on other grounds, 561 F.3d 1372 (Fed. Cir. 2009).

could have been presented to the PTO. Congress's reenactment of R.S. 4915, as Section 145 of the Patent Act of 1952, should be understood to adopt that settled judicial practice.

1. As discussed above, this Court recognized in *Morgan* that the "bill in equity" authorized under R.S. 4915 "is something more than a mere appeal." 153 U.S. at 124. It is, rather, "an application to the court to set aside the action of one of the executive departments of the government," made in the exercise of its delegated authority and expert judgment. *Ibid.* A judicial proceeding to overturn such a determination, the Court explained, "is something in the nature of a suit to set aside a judgment, and as such is not to be sustained by a mere preponderance of evidence." *Ibid.* Rather, any error in the agency's decision must be established "by testimony which in character and amount carries thorough conviction." *Id.* at 125.

The *Morgan* Court's description of equity proceedings under R.S. 4915 as "something in the nature of a suit to set aside a judgment," 153 U.S. at 124, is revealing. Under the settled principles of federal equity practice that prevailed at the time, a district court presented with a bill to set aside a prior judgment (known as a "bill of review" or an "original bill in the nature of a bill of review") would not rehear arguments or evidence that had been adjudicated in the prior proceeding, nor would it consider evidence that could have been produced during that proceeding in the exercise of reasonable diligence. See, *e.g.*, *Beard* v. *Burts*, 95 U.S. 434, 436 (1877) ("The facts are not open for a re-trial, unless the bill asserts that new evidence has been discovered, not obtainable before the first trial by the exercise of reasonable diligence."); see also *Scotten* v. *Littlefield*, 235 U.S.

407, 411 (1914); 2 Thomas Atkins Street, *Federal Equity Practice* § 2119, at 1256 (1909) (*Federal Equity Practice*); *id.* § 2150, at 1272; Benjamin J. Shipman, *Handbook of the Law of Equity Pleading* §§ 215-220, at 309-315 (1897). In addition, a bill of review could not be obtained unless the new evidence clearly established the claimant's right to relief. See *Southard* v. *Russell*, 57 U.S. (16 How.) 547, 567, 569 (1854) (new evidence must be "decided and controlling" on the disputed questions); *Federal Equity Practice* § 2151, at 1272 (To obtain leave to file a bill of review, new evidence "must be so controlling in its effect" as to "probably induce a different conclusion" on the merits.). The *Morgan* Court would have been aware of those principles—both the requirement of reasonable diligence, and the heightened standard necessary to overcome deference to the existing judgment—when it described a bill in equity under R.S. 4915 as "something in the nature of a suit to set aside a judgment."[3]

2. In the years preceding the enactment of the Patent Act of 1952, federal courts considering suits brought under R.S. 4915 routinely recognized limits on the admissibility of new evidence that the proponent could

---

[3] The court of appeals disregarded *Morgan*'s analogy to a "suit to set aside a judgment" on the ground that the bill authorized under R.S. 4915 was not literally termed a bill of review. See App., *infra*, 27a. But the fact that R.S. 4915 was not *in fact* a bill of review—the Court in *Morgan* described it as "*something in the nature of* a suit to set aside a judgment," 153 U.S. at 124 (emphasis added)—does not diminish the force of the analogy. The *Morgan* Court used the comparison to illustrate the deference due the Patent Office's decision and the resulting rule that the agency's action should not lightly be overturned. See *id.* at 124-125. The evidentiary limitations on a bill of review are therefore relevant to the *Morgan* Court's understanding of the nature of review in an R.S. 4915 proceeding.

have presented to the PTO in the first instance.[4] See, *e.g.*, *Schilling* v. *Schwitzer-Cummins Co.*, 142 F.2d 82, 85 (D.C. Cir. 1944) (R.S. 4915 "was not intended to encourage the practice of suppressing evidence before the administrative agency"; withheld evidence is inadmissible.); *Boucher Inventions, Ltd.* v. *Sola Elec. Co.*, 131 F.2d 225, 227 (D.C. Cir. 1942) ("Section 4915 * * * contemplates a full disclosure to that office, so far as is reasonably possible."); *Globe-Union, Inc.* v. *Chicago Tel. Supply Co.*, 103 F.2d 722, 728 (7th Cir. 1939); *Greene* v. *Beidler*, 58 F.2d 207, 209-210 (2d Cir. 1932); *Barrett Co.* v. *Koppers Co.*, 22 F.2d 395, 396 (3d Cir. 1927); *Western Elec. Co.* v. *Fowler*, 177 F. 224, 228 (7th Cir. 1910); see also *Schering Corp.* v. *Marzall*, 101 F. Supp. 571, 573 (D.D.C. 1951); App., *infra*, 74a-78a (Dyk, J., dissenting). And even when courts admitted new evidence in R.S. 4915 proceedings, they continued to apply *Morgan*'s deferential standard of review, rather than reviewing

---

[4] The court of appeals relied on *Butterworth*, in which the Court stated that an R.S. 4915 proceeding is "heard upon all competent evidence adduced and upon the whole merits." 112 U.S. at 61; see App., *infra*, 23a-24a. *Butterworth*, like the lower-court decisions on which it relied, predated *Morgan*'s holding that a suit brought under R.S. 4915 is an administrative-review proceeding involving deferential review. See, *e.g.*, *In re Squire*, 22 F. Cas. 1015, 1016 (C.C.E.D. Mo. 1877) (No. 13,269); see also *Gandy* v. *Marble*, 122 U.S. 432, 439 (1887) (citing *Butterworth* in describing R.S. 4915); App., *infra*, 67a-70a (Dyk, J., dissenting). Moreover, *Butterworth* and *Gandy*, like the subsequent decisions on which the court of appeals relied, see App., *infra*, 25a, 41a (citing *Hoover Co.*, 325 U.S. at 83, and *In re Hien*, 166 U.S. 432, 439 (1897)), stated only that new evidence was admissible in R.S. 4915 proceedings; they did not address the circumstances in which new evidence could be introduced. See, *e.g.*, *Hien*, 166 U.S. at 439 (noting the admissibility of new evidence in R.S. 4915 proceedings in order to "distinguish[] the proceeding by bill in equity under section 4915 from an appeal under section 4911").

the Patent Office's findings de novo. See *Minnesota Mining & Mfg. Co.* v. *Carborundum Co.*, 155 F.2d 746, 748-749 (3d Cir. 1946) (citing *Morgan* and stating that "[t]he question therefore is whether all competent evidence, 'new' and 'old', offered to the District Court carries 'thorough conviction' that the Patent Office erred"); *Schilling*, 142 F.2d at 85; *Nichols* v. *Minnesota Mining & Mfg. Co.*, 109 F.2d 162, 163-164 (4th Cir. 1940) (district court "properly applied the rule of Morgan v. Daniels" to newly available evidence); *Globe-Union, Inc.*, 103 F.2d at 732; *Dowling* v. *Jones*, 67 F.2d 537, 538 (2d Cir. 1933) (L. Hand, J.).

It was against this background—and in the wake of the 1946 enactment of the APA—that Congress readopted without material change the provisions governing judicial review of Patent Office decisions. The reports accompanying the 1952 Patent Act explained that the Act effected "no fundamental change in the various appeals and other review of Patent Office action." S. Rep. No. 1979, 82d Cong., 2d Sess. 7 (1952). "Congress is presumed to be aware of an administrative or judicial interpretation of a statute and to adopt that interpretation when it re-enacts a statute without change." *Forest Grove Sch. Dist.* v. *T.A.*, 129 S. Ct. 2484, 2492 (2009) (quoting *Lorillard* v. *Pons*, 434 U.S. 575, 580 (1978)). In view of the prevailing judicial practice with respect to new evidence in R.S. 4915 proceedings, there is no reason to conclude that Congress intended Section 145 to authorize a more intrusive judicial inquiry.

3. The en banc court of appeals relied substantially on testimony from congressional hearings preceding the 1927 Patent Act amendments, during which various witnesses urged the repeal or modification of R.S. 4915 and characterized the procedure authorized by the statute as

a "de novo" proceeding in district court. See App., *infra*, 14a-17a. As this Court has repeatedly made clear, however, isolated hearing testimony of this kind—and especially the testimony of opponents of proposed legislation—is not reliable evidence of Congress's intent and warrants little weight in the interpretation of federal statutes. *Bryan* v. *United States*, 524 U.S. 184, 196 (1998); *Kelly* v. *Robinson*, 479 U.S. 36, 51 n.13 (1986). Nor can those witnesses' use of the term "de novo," more than 20 years before the enactment of the APA, provide any reliable insight into congressional intent regarding the precise nature and scope of judicial review. Cf. *Zurko*, 527 U.S. at 156 (noting that the "relevant linguistic conventions" of administrative law "were less firmly established before adoption of the APA"); *Globe-Union, Inc.*, 103 F.2d at 728 (describing R.S. 4915 as a "de novo" proceeding while imposing limits on admissibility of new evidence).

C. The District Court Should Admit New Evidence Only If Its Proponent Had No Reasonable Opportunity To Present It To The PTO, And The Court Should Overturn The PTO's Decision Only If The Evidence Clearly Establishes That The Agency Erred

Consistent with principles of administrative exhaustion and deference to agency authority and expertise, as well as the historical practice that prevailed when Congress readopted Section 145, a plaintiff should be permitted to introduce new evidence only if he had no reasonable opportunity to provide that evidence to the PTO in the first instance. Restricting the introduction of new evidence in that manner reflects the PTO's primary decisionmaking authority, increases the incentive for patent applicants to compile a full factual record in the

agency proceedings, and limits the frequency with which courts must consider new information without the benefit of the agency's expertise. See pp. 13-16, *supra*.

When new evidence is admitted under this standard, the manner in which that evidence is considered may vary depending on the nature of the evidence. When the evidence consists of materials that the PTO can consider as part of its examination process (such as published prior art), the court ordinarily should remand the case to the PTO to permit the agency to consider the evidence in the first instance. See App., *infra*, 52a n.4 (Dyk, J., dissenting). That approach is consistent with administrative exhaustion principles, see *Lorion*, 470 U.S. at 744, and conserves judicial resources by enabling the PTO to correct any errors in its prior decision, which may obviate the need for subsequent judicial review.[5] See *McKart*, 395 U.S. at 193-195.

When the plaintiff in a Section 145 suit introduces new evidence that the PTO may not consider (such as oral testimony, see 37 C.F.R. 1.2), remanding to the agency is not a useful option, and the district court must evaluate the new evidence in the first instance. In considering the new evidence together with the evidence on which the PTO based its decision, the court may give the new evidence more weight in the analysis, in recognition of the fact that the PTO's conclusions did not take that evidence into account. Cf. *American Hoist & Derrick*

---

[5] Before the issuance of the decision in this case, district courts routinely remanded to the PTO to permit it to consider new evidence. See, *e.g.*, *ExxonMobil Chem. Patents Inc.* v. *Godici*, No. Civ. A. 01-00377 (HHK), 2002 WL 34233002, at *3-*4 (D.D.C. Feb. 12, 2002) (citing cases in which courts remanded to the "Patent Office after the discovery of additional prior art in order to benefit from the Patent Office's technical expertise in assessing the art").

Co. v. *Sowa & Sons*, 725 F.2d 1350, 1359-1360 (Fed. Cir.) (adopting this approach for new-evidence challenges to the PTO's grant of a patent), cert. denied, 469 U.S. 821 (1984). But the court should overturn the agency's decision only if the new evidence, considered together with the administrative record, creates a "thorough conviction" that the PTO erred. See *Morgan*, 153 U.S. at 125. This approach recognizes that the agency's decision should not be reversed unless the court has a high degree of confidence that the decision was incorrect, while permitting the court to give effect to the fact that the district court has before it a fuller record than the PTO. It is also consistent with the Federal Circuit's treatment of new-evidence challenges to the validity of granted patents. See *American Hoist*, 725 F.2d at 1359-1360.

II. THE COURT OF APPEALS' DECISION DEVIATES FROM THE DECISIONS OF THE REGIONAL CIRCUIT COURTS

The court of appeals' construction of Section 145 conflicts with the decisions of several regional courts of appeals. Before the Federal Circuit was established and given exclusive appellate jurisdiction over actions under Sections 141 and 145, the D.C. Circuit had held that in Section 145 suits, "the plaintiff may not submit for the first time evidence which he was negligent in failing to submit to the Patent Office." *DeSeversky* v. *Brenner*, 424 F.2d 857, 858 n.5 (1970); see *California Research Corp.* v. *Ladd*, 356 F.2d 815, 820 n.18 (1966). Section 145 suits, the court observed, "may not be conducted in disregard of the general policy of encouraging full disclosure to administrative tribunals." *DeSeversky*, 424 F.2d at 858-859 n.5. Even when new evidence was introduced, moreover, the court applied a deferential standard of review derived from *Morgan*: "[G]reat weight

attaches to the expertise of the Patent Office and its findings on the issue of obviousness, particularly in highly technical matters, and the decision of the Patent Office will not be overturned unless new evidence is introduced which carries thorough conviction that the Patent Office erred." *Id.* at 858 (internal quotation marks omitted).

The decision below also conflicts with pre-1952 circuit-court decisions addressing the admissibility and use of new evidence in proceedings under R.S. 4915. The Second, Third, Seventh, and D.C. Circuits held that evidence that had intentionally been withheld from the Patent Office was not admissible. See *Dowling*, 67 F.2d at 538; *Carborundum Co.*, 155 F.2d at 748; *Barrett Co.*, 22 F.2d at 396-397; *Globe-Union, Inc.*, 103 F.2d at 728; *Schilling*, 142 F.2d at 85; see also App., *infra*, 74a-78a (Dyk, J., dissenting). And even in cases where new evidence was admitted, the Second, Third, Fourth, Seventh, and D.C. Circuits applied *Morgan*'s deferential standard of review, requiring the plaintiff to create a "thorough conviction" that the Patent Office had erred. See *Dowling*, 67 F.2d at 538; *Carborundum Co.*, 155 F.2d at 748-749; *Nichols*, 109 F.2d at 163-164; *Globe-Union, Inc.*, 103 F.2d at 729; *Schilling*, 142 F.2d at 85; see also pp. 20-22, *supra*.

The en banc court below regarded these decisions as irrelevant because the regional courts of appeals excluded evidence under Section 145 "under an array of inconsistent standards." App., *infra*, 19a. But while the regional courts of appeals employed a range of different verbal formulations, they consistently placed significant limitations on new evidence and insisted on a deferential standard of review. The Federal Circuit is thus alone in departing from established administrative-law princi-

ples in its implementation of Section 145. See App., *infra*, 73a, 78a (Dyk, J., dissenting).

III. THE QUESTIONS PRESENTED ARE IMPORTANT

The Federal Circuit's ruling subjects the PTO's expert decisions to a form of heightened judicial scrutiny that has no statutory or historical foundation and contravenes basic principles of administrative law. Congress placed the administration of the patent system—which by its nature involves the evaluation of claimed advances at the forefront of scientific and technical knowledge—in a specialized agency equipped to make the many factual determinations necessary to decide whether a putative invention should be patented. See 35 U.S.C. 101-103, 112; *Pfaff* v. *Wells Elecs., Inc.*, 525 U.S. 55, 63 (1998). Absent clear textual or historical evidence that Congress intended the PTO's expert determinations to be a warmup for a judicial redetermination of patentability, based on evidence withheld from the PTO, the court of appeals should not have departed from the background principles that govern judicial review of agency action.

This Court has previously reversed the Federal Circuit's deviation from administrative-law principles in its review of PTO decisions. In *Zurko*, the Federal Circuit ruled that the PTO's patent denials should be subjected to judicial scrutiny under a standard more demanding than that set forth in the APA. 527 U.S. at 153. This Court rejected that approach, holding that there is no reason "why direct review of the PTO's patent denials demands a stricter fact-related review standard than is applicable to other agencies." *Id.* at 165. A similar result is warranted here.

That is especially so because the decision below creates an unjustified disparity between the two statutory avenues for judicial review of the PTO's patent denials. Under *Zurko*, challenges brought directly in the Federal Circuit pursuant to Section 141 are subject to the deferential standards set forth in the APA. Under the decision below, by contrast, challenges brought in district court pursuant to Section 145 will proceed under a regime that bears little resemblance to ordinary administrative review. Simply by proffering a declaration or other readily available evidence, a Section 145 plaintiff can obtain searching judicial review of the sort that this Court rejected in *Zurko*.

The court of appeals' decision gives patent applicants an obvious incentive to utilize Section 145 in an attempt to bypass the PTO in favor of patent consideration by a non-expert court. The decision not only permits judicial consideration of evidence that the patent applicant withheld from the examiner; it rewards applicants for such behavior by providing them a more favorable standard of judicial review. Indeed, patent practitioners are already advising their clients that they may "avoid the deference to be given to USPTO fact determinations under the APA * * * merely by the submission of new evidence and/or live testimony" under Section 145. See Monte Cooper & Robert M. Isackson, *The Fed. Circ. Stance in* Hyatt v. Kappos, http://www.law360.com/ip/articles/211544 (Dec. 3, 2010); see also David J. Muzilla, *Patent Stalled at the USPTO? Consider Presenting New Evidence in Federal District Court*, http://www.hahnlaw.com/references/73542574-85f1-4e77-b7aa-1094244516b1.pdf (2011). This derogation of the PTO's expertise and authority is precisely the result that the organizing principles of administrative law are meant to

avoid. As the dissenting judges on the en banc court of appeals observed, applicants are most likely to "bypass the PTO in favor of a second bite at the apple in the district court * * * in those circumstances where an expert agency would reject the evidence but a non-expert district court might be convinced to accept it. A more pernicious approach is difficult to imagine." App., *infra*, 80a.

2. This case vividly illustrates the perverse consequences of the court of appeals' rule. The Board held that, under the PTO's rules governing practice before the agency, respondent had forfeited his new arguments by failing to present them at the appropriate stage of the administrative proceedings. The district court found that respondent had been given a reasonable opportunity to present his new evidence to the PTO but had negligently failed to do so. The en banc Federal Circuit nevertheless held that the district court was required not only to admit the new evidence, but to consider de novo every factual question to which that evidence relates. Such an extraordinary and disruptive rule warrants this Court's review.

IV. THE COURT SHOULD HOLD THIS PETITION PENDING ITS DECISION IN *MICROSOFT*

In *Microsoft*, this Court is considering what evidentiary standard should apply when the defendant in a patent-infringement suit asserts as an affirmative defense that the relevant patent is invalid. That question is substantially related to the questions presented in this case. More than a century ago, this Court recognized that a challenge to the validity of a granted patent in infringement litigation is "closely" related to an action challenging the PTO's decision that a party is not enti-

tled to a patent. *Morgan*, 153 U.S. at 123. Both types of challenges, the Court explained, are in essence attacks on the PTO's disposition of a patent application. *Id.* at 124. The Court therefore concluded that in both contexts, judicial review should be conducted using a deferential standard of review that requires more than "a mere preponderance" to overturn the PTO's decision. *Ibid.*; *id.* at 125.

In its brief as amicus curiae supporting respondents in *Microsoft*, the United States has argued that this Court should affirm the Federal Circuit's longstanding rule that the party asserting invalidity must establish it by clear and convincing evidence, even when the evidence of invalidity was not considered by the PTO in the examination process. U.S. Amicus Br. at 6, *Microsoft*, *supra* (No. 10-290). New evidence, however, may be given greater weight in the analysis. *Ibid.*; see *American Hoist*, 725 F.2d at 1359-1360. In the United States' view, the principles announced in *Morgan*—which anticipate contemporary rules of administrative review—are best served by adopting that approach in *Microsoft* and reversing the Federal Circuit's deviation from administrative-law principles in this case. That result also best effects the *Morgan* Court's recognition that the two types of challenges implicate common principles of administrative deference that should inform the nature and scope of judicial review in both contexts. By contrast, the decision below, taken together with the clear-and-convincing-evidence standard that the Federal Circuit applies in invalidity challenges, creates a particularly anomalous regime in which the PTO's decision to *grant* a patent receives deference even when the challenger presents new evidence of invalidity, but the

PTO's decision to *deny* a patent receives no deference whenever new evidence is introduced.

To be sure, the decision in *Microsoft* is unlikely fully to resolve the questions presented here. In particular, the first question presented in this case—*i.e.*, whether a patent applicant may introduce in Section 145 proceedings evidence that he failed without reasonable cause to present to the PTO in the first instance—has no analogue in *Microsoft*. Nevertheless, because both cases involve the application of administrative-review principles to the PTO's patenting decisions, the Court's decision in *Microsoft* may shed light on the proper disposition of this case. Although the questions presented in this case are sufficiently important to warrant the Court's plenary review, it therefore would be appropriate in the first instance to hold the petition pending the decision in *Microsoft*.[6] That approach would also ensure that, if the Court ultimately grants certiorari in this case, the parties' briefs on the merits can address the implications of the *Microsoft* decision for the proper implementation of Section 145.

---

[6] Copies of this petition will be provided to counsel for the petitioner and respondents in *Microsoft*.

CONCLUSION

The petition for a writ of certiorari should held pending this Court's decision in *Microsoft Corp.* v. *i4i Ltd. Partnership*, No. 10-290 (oral argument scheduled for Apr. 18, 2011).

Respectfully submitted.

NEAL KUMAR KATYAL
Acting Solicitor General

BERNARD J. KNIGHT, JR.
General Counsel

TONY WEST
Assistant Attorney General

RAYMOND T. CHEN
Solicitor and Deputy General Counsel

MALCOLM L. STEWART
Deputy Solicitor General

GINGER D. ANDERS
Assistant to the Solicitor General

ROBERT J. MCMANUS
THOMAS W. KRAUSE
Associate Solicitors
U.S. Patent and Trademark Office

SCOTT R. MCINTOSH
MARK R. FREEMAN
Attorneys

APRIL 2011

APPENDIX A

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

No. 2007-1066

GILBERT P. HYATT, PLAINTIFF-APPELLANT

v.

DAVID KAPPOS, DIRECTOR, PATENT AND TRADEMARK OFFICE, DEFENDANT-APPELLEE

Decided: Nov. 8, 2010

Appeal from the United States District Court for the District of Columbia in Case No. 03-CV-901, Judge Henry H. Kennedy, Jr.

Before: RADER, Chief Judge, NEWMAN, LOURIE, BRYSON, GAJARSA, LINN, DYK, PROST, and MOORE, *Circuit Judges.*

MOORE, *Circuit Judge.*

Under the patent laws, a patent applicant who is dissatisfied with the decision of the Board of Patent Appeals and Interferences (Board) regarding his application may choose one of two paths. The applicant may appeal the Board's decision to the Court of Appeals for the Federal Circuit, which will review the Board's decision on the record that was before the U.S. Patent and

Trademark Office (Patent Office). Alternatively, the applicant may file a civil action in district court, and the court will determine whether the applicant "is entitled to receive a patent for his invention . . . as the facts in the case may appear." 35 U.S.C. § 145. This case presents the issue of what limitations exist on an applicant's right to introduce new evidence in a § 145 civil action.

We have characterized this civil action as a "hybrid" action. It is not an appeal; the language of § 145 expressly distinguishes its civil action from a direct appeal, and the Supreme Court has recognized that an applicant may introduce new evidence before the district court that was not presented to the Patent Office. However, it is also not an entirely de novo proceeding. Issues that were not considered by the Patent Office cannot be raised with the district court in most circumstances, and if no new evidence is introduced, the court reviews the action on the administrative record, subject to the court/agency standard of review. The particular significance of a § 145 civil action is that it affords an applicant the opportunity to introduce new evidence after the close of the administrative proceedings—and once an applicant introduces new evidence on an issue, the district court reviews that issue de novo. Thus, an applicant's ability to introduce new evidence is the hallmark of a § 145 action. It is the primary factor that distinguishes a civil action under § 145 from an appeal.

We hold that 35 U.S.C. § 145 imposes no limitation on an applicant's right to introduce new evidence before the district court, apart from the evidentiary limitations applicable to all civil actions contained in the Federal Rules of Evidence and Federal Rules of Civil Procedure. In doing so, we reject the Director's proposal that only

"new evidence that could not reasonably have been provided to the agency in the first instance" is admissible in a § 145 action. Dir. Br. at 8. While the proceedings before the Patent Office do not limit the admissibility of new evidence in the district court, they may be considered by the district court if they cast doubt on the reliability of late-produced evidence, as with inconsistent statements or new recollections of previously forgotten events. As with any evidence introduced in a civil action, the district court as factfinder may give less weight to evidence introduced by an applicant in a § 145 action if the district court questions its credibility or reliability. Because the district court abused its discretion when it excluded Mr. Hyatt's declaration under the wrong legal standard, we vacate the decision of the district court and remand.

I. Background

Gilbert P. Hyatt is the sole named inventor of U.S. Patent Application No. 08/471,702 (the '702 application), titled "Improved Memory Architecture Having a Multiple Buffer Output Arrangement." The '702 application related to a computerized display system for processing image information.

Mr. Hyatt filed the '702 application on June 6, 1995. As filed, the '702 application included a 238-page specification, 40 pages of figures, and 15 claims; it originally claimed priority through a chain of related applications to an application filed in 1984 and was later amended to claim priority to a 1975 application. Mr. Hyatt filed several preliminary amendments in which he amended the drawings and specification and added 74 new claims.

description had "extensive basis" in the specification. J.A. 10830. Mr. Hyatt included a table (Table 1) that listed representative pages in the specification containing the "terminology" objected to by the examiner. J.A. 10832. For certain terms, Mr. Hyatt also identified figures and page ranges of the specification that described the relevant terms.

The Board reversed all of the examiner's rejections for obvious-type and *Schneller*-type double patenting. The Board also reversed all of the anticipation and obviousness rejections. With respect to the written description rejections, the Board noted that merely pointing to the occurrence of isolated words in the specification—as Mr. Hyatt had done in Table I—did not adequately establish that the specification contained written description for the particular combination of elements that made up each limitation. Still, after performing its own review of the specification, as it is required to do, the Board reversed all of the examiner's written description and enablement rejections with respect to 38 of the pending claims and many of these rejections for the other 79 claims, finding that the features identified by the examiner as lacking written description were either adequately disclosed or were not claimed. Thus, Mr. Hyatt prevailed on over 93% of the examiner's rejections at the Board level. The Board affirmed at least one of the examiner's written description and enablement rejections with respect to each of 79 claims. Mr. Hyatt filed a Request for Rehearing; the Board dismissed the Request without considering the merits, finding that Mr. Hyatt raised new arguments that could have been presented earlier to either the examiner or the Board.

Following the Board's decision dismissing his Request for Rehearing, Mr. Hyatt filed a civil action in the United States District Court for the District of Columbia against the Director of the Patent Office (Director) pursuant to 35 U.S.C. § 145. The Director moved for summary judgment that the pending claims were invalid for failure to comply with the written description requirement. Mr. Hyatt opposed the motion, arguing that genuine issues of material fact existed to preclude summary judgment as to written description. In support of his opposition, Mr. Hyatt submitted a written declaration in which he identified portions of the specification that one of skill in the art would understand to describe the limitations challenged by the Director. The Director argued that the court should not consider Mr. Hyatt's declaration because he did not previously submit it to the examiner or the Board.

The district court determined that it could not consider Mr. Hyatt's declaration. *Hyatt v. Dudas*, 2005 U.S. Dist. LEXIS 45319, at *12 (D.D.C. Sept. 30, 2005). The court found that the Board's written description rejections were substantively identical to, albeit more detailed than, the rejections issued by the examiner. *Id.* at *19. Because Mr. Hyatt's declaration was directed to those written description rejections, the court concluded that he could have presented the declaration earlier, "certainly by the time his patent application was considered by the Board." *Id.* at 24. Finding that Mr. Hyatt had no explanation for why he failed to offer his declaration during the proceedings before the Board, the court determined that "[Mr.] Hyatt's failure to explain why he didn't submit his declaration earlier is negligent, and the district court need not consider evidence negligently

submitted after the end of administrative proceedings." *Id.* at *26.

Mr. Hyatt did not submit any evidence to the district court apart from his declaration, which the court excluded. Therefore, the court reviewed the Board's fact findings for substantial evidence and granted summary judgment to the Director that the pending claims were unpatentable for failure to comply with the written description requirement. *Id.* at *27.

Mr. Hyatt appealed, and a divided panel of this court affirmed. *Hyatt v. Doll*, 576 F.3d 1246 (Fed. Cir. 2009). The panel majority acknowledged that "it is beyond question that in appropriate circumstances new evidence may be submitted to the district court in a § 145 action (subject, at least, to the Federal Rules of Evidence)." *Id.* at 1266. However, the majority stated that there was a "general practice" among federal courts "in some circumstances to exclude evidence which a party could and should have introduced before the Patent Office but did not despite an obligation to do so." *Id.* at 1266. The majority also concluded that the Administrative Procedure Act (APA) imposed restrictions on the admission of new evidence in a § 145 action. *Id.* at 1270. The majority noted that judicial review of an agency action is generally restricted to the agency record and that the Patent Office is an agency whose findings of fact must be reviewed according to the APA's court/agency standard of review. *Id.* at 1267, 1269. Therefore, the majority determined that although review in a § 145 action is "[o]f course . . . not strictly confined to the agency record," "neither are [§ 145] proceedings wholly de novo." *Id.* at 1269.

Turning to the merits of Mr. Hyatt's case, the majority stated that although Mr. Hyatt could have identified the portions in the specification that provided written description support for the disputed limitations any time after the office action, he "refused to cooperate, even though he necessarily possessed the information the examiner sought by the time he filed his application." *Id.* Although the majority acknowledged the district court's finding that Mr. Hyatt's failure to submit the evidence in his declaration earlier was negligent, the majority determined that "it is clear from the record that Hyatt *willfully* refused to provide evidence in his possession in response to a valid action by the examiner." *Id.* (emphasis added). In light of Mr. Hyatt's "willful non-cooperation," the majority held that the district court did not abuse its discretion in excluding the declaration. *Id.* The majority then affirmed the court's grant of summary judgment. *Id.* at 1279.

The dissenting judge disagreed, arguing that the district court abused its discretion by applying the wrong legal test for the admissibility of the evidence. The dissent argued that the plain language, legislative history, and Supreme Court jurisprudence relating to § 145 establish that an applicant's right to present new evidence in a § 145 action is subject only to the Federal Rules of Evidence and Civil Procedure. *Id.* at 1280-81, 1284. Further, the dissent disputed the propriety of determining on appeal that Mr. Hyatt willfully withheld his declaration.

We agreed to rehear the appeal en banc and vacated the judgment of the panel. *Hyatt v. Kappos*, 366 Fed. Appx. 170 (Fed. Cir. 2010). We asked the parties to direct their briefs to the following questions:

(a) Are there any limitations on the admissibility of evidence in section 145 proceedings? In particular-

(i) Does the Administrative Procedure Act require review on the agency record in proceedings pursuant to section 145?

(ii) Does section 145 provide for a de novo proceeding in the district court?

(iii) If section 145 does not provide for a de novo proceeding in the district court, what limitations exist on the presentation of new evidence before the district court?

(b) Did the district court properly exclude the Hyatt declaration?

In addition to the parties' briefs, we received seven amicus briefs. Amicus briefs submitted by amici Public Patent Foundation, American Intellectual Property Law Association (AIPLA), Fédération Internationale des Conseils en Propriété Industrielle, New York Intellectual Property Law Association (NYIPLA), and Intellectual Property Owners Association (IPO) opposed the panel majority's imposition of limitations on the evidence admissible in a § 145 action. Amici Intel Corporation and the Franklin Pierce Law Center submitted briefs arguing in favor of greater limitations on the admissibility of evidence in § 145 actions, though neither argued in favor of the standard proposed by the Patent Office in this case.

We heard oral argument on July 8, 2010. For the reasons below, we hold that the only limitations on the admissibility of evidence applicable to a § 145 proceeding are the limitations imposed by the Federal Rules of

Evidence and Federal Rules of Civil Procedure. Therefore, we hold that the district court applied the wrong legal standard for the admissibility of evidence in a § 145 proceeding and abused its discretion when it excluded Mr. Hyatt's declaration.

II. DISCUSSION

On rehearing, Mr. Hyatt argues that the only limitations on the admissibility of new evidence in a § 145 proceeding are the rules of evidence generally applicable to all civil actions. Mr. Hyatt asserts that the legislative history of § 145 and its predecessor statute shows that Congress intended to provide a genuine alternative to an on-the-record appeal that permits an applicant to bring a new case, complete with new evidence, to show that his patent should issue. Mr. Hyatt asserts that case law from the Supreme Court and this circuit supports his interpretation. Mr. Hyatt also argues that nothing in the APA limits the introduction of new evidence in a § 145 proceeding. Therefore, Mr. Hyatt contends that the district court acted improperly in excluding his declaration.

The Director, in contrast, argues that § 145 should be interpreted to prohibit an applicant from introducing new evidence before the district court unless the applicant could not reasonably have provided that evidence to the Patent Office in the first instance. The Director asserts that the proceeding authorized by the predecessor statute of § 145 was effectively a suit to set aside a judgment and that under established rules of equity practice, a court presiding over such a suit would have excluded evidence that the plaintiff failed, without reasonable excuse, to present previously. Further, the Director

argues that APA principles and various policy considerations weigh in favor of limiting an applicant's right to introduce new evidence. The Director contends that because Mr. Hyatt could have presented the declaration to the examiner and the Board prior to instigating the present action, the district court correctly excluded the declaration.

A.

Section 145, titled "Civil action to obtain patent," provides as follows:

> An applicant dissatisfied with the decision of the Board of Patent Appeals and Interferences in an appeal under section 134(a) of this title may, *unless appeal has been taken* to the United States Court of Appeals for the Federal Circuit, *have remedy by civil action* against the Director in the United States District Court for the District of Columbia if commenced within such time after such decision, not less than sixty days, as the Director appoints. The court may adjudge that such applicant is entitled to receive a patent for his invention, as specified in any of his claims involved in the decision of the Board of Patent Appeals and Interferences, *as the facts in the case may appear* and such adjudication shall authorize the Director to issue such patent on compliance with the requirements of law. All the expenses of the proceedings shall be paid by the applicant.

35 U.S.C. § 145 (emphases added).

On its face, § 145 authorizes a civil action in district court by which an applicant can prove his entitlement to a patent. The statute provides no indication that this

civil action is somehow different from a customary civil action. In particular, § 145 does not provide that unique rules of evidence, separate from or supplementary to the Federal Rules of Evidence that apply to all civil actions, control to limit an applicant's ability to introduce new evidence before the district court. Additionally, § 145 makes clear that the civil action is distinct from an appeal, in which the applicant would be limited to the record before the Patent Office. *See* 35 U.S.C. § 144. Pursuant to the plain language of § 145, this civil action does not merely afford judicial review of agency action. Rather, the statute directs that the district court may "adjudge that such applicant is entitled to receive a patent for his invention . . . as the facts in the case may appear."

B.

The lengthy legislative history of § 145 and its predecessor statute, which dates back nearly to the creation of the Patent Office, shows that Congress intended to provide for a civil action in which an applicant would be free to introduce new evidence. Congress established the Patent Office and the patent examination scheme in 1836. Act of July 4, 1836, ch. 357, 5 Stat. 117 (1836 Act). The 1836 Act provided that the Commissioner of Patents would determine whether each applicant was entitled to a patent on his application. *Id.* §§ 1, 7, 5 Stat. 117, 120. An applicant dissatisfied with the Commissioner's decision regarding his application could appeal to a board of three examiners, which could overturn the Commissioner's decision in full or in part. *Id.* § 7, 5 Stat. 121.

The decision of the board of examiners was final in ex parte cases. *Id.*; *see also* P.J. Federico, *Evolution of*

Patent Office Appeals, 22 J. Pat. Off. Soc'y 838, 840 (1940). However, in cases where the board rejected an application on the ground that it interfered with an unexpired patent, the 1836 Act provided that the applicant "may have remedy by bill in equity." *Id.* § 16, 5 Stat. 123-24. A bill in equity was the written mechanism that commenced an original suit in a court of equity. *See* Shipman, *Handbook of the Law of Equity Pleading* § 101, p. 168 (West 1897). Courts with jurisdiction over an applicant's bill in equity could "adjudge that such applicant is entitled . . . to have and receive a patent for his invention . . . as the fact of priority of right or invention shall in any such case be made to appear." 1836 Act, § 16, 5 Stat. 124. Three years later, Congress extended an applicant's remedy by bill in equity beyond interferences to "all cases where patents are refused for any reason whatever." Act of Mar. 3, 1839, ch. 88, § 10, 5 Stat. 353, 354.

Congress made various changes to the appeal structure within the Patent Office over the next few decades. None of these changes affected an applicant's separate remedy by bill in equity, which continued to be available. In 1870, Congress passed an act to "revise, consolidate, and amend the Statutes relating to Patents and Copyrights." Act of July 8, 1870, ch. 230, 16 Stat. 198 (1870 Act). The 1870 Act provided for a three-tier appeal process within the Patent Office. An applicant whose application was rejected by the primary examiner could appeal to a board of examiners-in-chief. *Id.* § 46, 16 Stat. 204-05. Similarly, a party to an interference could appeal an adverse decision by the examiner in charge of interferences to the board. *Id.* If the applicant or party to the interference was dissatisfied with the board's decision, he could appeal first to the Commissioner of Pat-

ents and then to the supreme court of the District of Columbia. *Id.* §§ 47-48, 16 Stat. 205.

Pursuant to the 1870 Act, after all of these appeals were exhausted, the applicant could still seek remedy by bill in equity:

> [W]henever a patent on application is refused . . . the applicant may have remedy by bill in equity; and the court . . . may adjudge that such applicant is entitled, according to law, to receive a patent for his invention . . . as the facts in the case may appear. . . . [A]nd all the expenses of the proceeding shall be paid by the applicant, whether the final decision is in his favor or not.

Id. § 52. Congress later recodified this section as § 4915 of the Revised Statutes.

Congress significantly modified the patent application review process in 1927, primarily in response to criticism regarding the length and complexity of the process. Act of March 2, 1927, ch. 273, 44 Stat. 1335 (1927 Act); *see also* Federico, 22 J. Pat. Off. Soc'y at 941.[1] Various schemes were proposed to Congress for simplifying the process. Some proposals advocated eliminating one of the appeals; others advocated doing away with the bill in equity under § 4915. *Id.* at 941-42. The con-

---

[1] As P.J. Frederico explained in 1940, the "bill in equity" which in 1839 applied to both ex parte and interference cases "was thus at this time [1839] given the scope which has been maintained to the present day." Federico, 22 J. Pat. Off. Soc'y at 935. While Congress considered and changed the appeals process in 1927, the language of § 4915 in the bills debated in February 1927 and December 1927 was identical, and was ultimately enacted in § 4915 including the requirement that "the record in the Patent Office shall be admitted . . . without prejudice, however, to the right of the parties to take further testimony."

tinued viability of § 4915 was a particularly disputed issue, and Congress heard extensive testimony regarding the merits of the remedy by bill in equity in the hearings that preceded the Act.

Those who favored retaining § 4915 argued that an applicant's right to introduce evidence that had not been before the Patent Office created a truly distinct, and therefore valuable, alternative to an on-the-record appeal. Charles E. Howson, Chairman of the Committee on Patent Law Revision for the American Bar Association, explained the significance of § 4915 as follows:

> Section 4915 has always been regarded by the patent bar, or those experienced in patent practice, as the final check on the Patent Office to enable a deserving inventor to get his just deserts if everything else fails. The advantage of section 4915 is that it enables the party in interest, desiring to obtain a patent, to take evidence in a court or tribunal whose business it is to try issues of facts *and make up a record in addition to that he has been enabled to furnish the examiners in the Patent Office*, and therefore get before a court of competent jurisdiction everything connected with his rights and every fact connected with his patent; in other words, *have before him everything that courts in the country have before them in infringement cases.*

To Amend Section 52 of Judicial Code and Other Statutes Affecting Procedure in Patent Office: Hearings on H.R. 6252 and H.R. 7087 Before the H. Comm. on Patents, 69th Cong., 1st Sess. 20-21 (1926) *(To Amend Section 52)* (emphases added). Another proponent of § 4915, A.C. Paul, the Chairman of the Patent Section of the Legislation Committee of the American Bar Associa-

tion, testified that he understood § 4915 to grant an applicant the right to "have the case start *de novo* after the decision of the board." *Id.* at 81. Mr. Paul distinguished the bill in equity under § 4915 from an on-the-record appeal, explaining that "the difference [between § 4915 and an appeal] would be then if we went to the court of appeals by an appeal the decision must be based upon the same record. If we go into a court of equity the *parties may use the record that they have in the Patent Office and may supplement it by additional evidence.*" *Id.* (emphasis added). Another committee member testified that the original suit under § 4915 allowed an inventor to strengthen his case by enabling an applicant to "take testimony and bring out all the facts pertinent and have an absolutely full hearing in the matter." *Id.* at 13 (statement of Henry Huxley, Member of the Patent Section of the Legislation Committee of the American Bar Association). Congressman Albert Vestal similarly explained that "if a party feels aggrieved, he can bring his suit in the equity court [under § 4915], but it is not an appeal. It is the bringing of a new suit." *Id.* at 36; *see also id.* at 66 (under § 4915, "you may go to a court of equity and take testimony in open court and use the testimony in the Patent Office or both and have it as a proceeding de novo, not appeal with the presumption in favor of what has been done, but where you stand and the court listens to what you have to say and decides it on the merits") (statement of Otto R. Barnett, President, American Patent Law Association, Chicago, Ill.).

The opponents of § 4915 also recognized that the remedy by bill in equity allowed an applicant to freely introduce new evidence in the district court. Indeed, they objected to the provision on precisely this basis.

For example, the Commissioner of Patents testified that § 4915 entitled an applicant to "start de novo . . . and build up a new record" in district court. *Id.* at 80 (statement of Hon. Thomas E. Robertson, Commissioner of Patents). He cautioned that § 4915 permitted applicants to "bring[] in evidence that they could have brought in before [the Patent Office] but did not." *Id.* at 81. The Commissioner also recognized that this new action allowed the relitigation of matters already decided by the Patent Office, permitting the applicant "to build up a new record for dragging an opponent through a second time." *Id.* at 80; *see also id.* at 81 ("after dragging a man through all this procedure which you have said is so complicated and burdensome, [an applicant can] start de novo in court, and bring in testimony not taken the first time"). The former Assistant Commissioner similarly opposed § 4915, arguing that § 4915 "should be cut out entirely for ex parte applications" to force an applicant to introduce "all the testimony pertinent to his case" to the Patent Office. *Id.* at 76 (statement of Karl Fenning, former Assistant Commissioner of Patents).

Thus, proponents and opponents of § 4915 alike recognized, and conveyed to Congress, that the remedy by bill in equity allowed an applicant to introduce new evidence in the district court, regardless of whether that evidence had been provided to the Patent Office in earlier proceedings. Nothing in the Congressional record leading up to the 1927 Act indicates that any member of Congress or the bar contemplated any limit on this right apart from the limits imposed by the normal rules of equity practice.

Despite being presented with the policy reasons for eliminating the remedy by bill in equity, Congress chose

to retain § 4915. 1927 Act, § 3, 44 Stat. 1335-36. However, Congress gave applicants a right to choose between an appeal and the remedy by bill in equity. An applicant who chose to appeal an adverse decision by the Patent Office thus "waive[d] his right to proceed under section 4915." *Id.* § 8, 44 Stat. 1336.

Congress bifurcated § 4915 into two provisions in 1952, sections 145 and 146 of Title 35 of the United States Code.[2] Act of July 19, 1952, ch. 950, §§ 145-46, 66 Stat. 792, 803 (1952 Act). Section 145, which controlled ex parte proceedings, provided that an "applicant dissatisfied with the decision of the Board of Appeals may unless appeal has been taken to the United States Court of Customs and Patent Appeals have *remedy by civil action* against the Commissioner." *Id.* § 145, 66 Stat. 803 (emphasis added). Section 146, which applied to interferences, similarly provided for parties to an interference to have a "remedy by civil action" and that "the record in the Patent and Trademark Office shall be admitted . . . without prejudice to the right of the parties to take further testimony." *Id.* § 146, 66 Stat. 803. Congress stressed that the 1952 Act made "no fundamental change in the various appeals and other review of Patent Office action." *See* S. Rep. No. 82-1979 (1952), reprinted in 1952 U.S.C.C.A.N. 2394, 2400. Subsequent changes to § 145 have not altered the substantive application of the statute in any way relevant to our analysis.

---

[2] As sections 145 and 146 both stem from § 4915, we have characterized these sections as "parallel provisions" to be treated similarly. *Winner Int'l Royalty Corp. v. Wang*, 202 F.3d 1340, 1345 (Fed. Cir. 2000). We see no rationale that would justify distinguishing between interferences and ex parte actions for admissibility purposes.

Though the Director does not directly dispute any of the relevant legislative history, he nonetheless argues that Congress intended for new evidence to be admitted in § 145 actions only where it could not reasonably have been presented to the agency in the first instance. Dir. Br. at 28. The Director points to pre-1952 decisions of some federal courts which he characterizes as having "excluded or discounted evidence which the applicant had failed, without reasonable excuse, to present to the agency." *Id.* at 26. According to the Director, Congress must have intended to codify this "longstanding" interpretation when Congress reenacted § 4915 without substantive change as § 145. *Id.* at 28. The flaw with the Director's claim is inherent in his argument—Congress could not have implicitly adopted the different approaches various courts took with regard to an admissibility standard.

The Director is correct that, prior to the 1952 Act, some regional circuits excluded or gave less weight to evidence based on an applicant's conduct before the Patent Office. The courts did so under an array of inconsistent standards (including willful withholding, intentional suppression, and bad faith). *See, e.g., Barrett Co. v. Koppers Co.*, 22 F.2d 395, 397 (3d Cir. 1927) (holding that when a party intentionally withholds evidence within his possession before the Patent Office, he may not later introduce that evidence in a suit under § 4915); *Dowling v. Jones*, 67 F.2d 537, 538 (2d Cir. 1933) (explaining that in *Barrett* "the Third Circuit refused to consider evidence which the inventor had deliberately suppressed in the interference, and used broader language than the exact situation required . . . However, it does not follow that it would have extended the doctrine to evidence not suppressed, but merely neglected

through the plaintiff's slackness in preparation."); *Knutson v. Gallsworthy*, 164 F.2d 497, 509 (D.C. Cir. 1947) ("[I]f no bad faith on the part of the profferer is involved, such as deliberate withholding for some tactical reason, the court could receive the evidence.").[3] In many of the cases cited by the Director, the court both admitted and considered the applicant's new evidence. *See, e.g., Globe-Union, Inc. v. Chicago Tel. Supply Co.*, 103 F.2d 722, 727 (7th Cir. 1939) ("We can not escape the strength and the compelling influence of the additional evidence that was adduced in the district court.") Some courts held that an applicant's failure to previously introduce the evidence before the Patent Office goes to the weight of the evidence, not to its admissibility. *E.g., Western Electric Co. v. Fowler*, 177 F. 224, 228-29 (7th Cir. 1910); *Standard Cartridge Co. v. Peters Cartridge Co.*, 77 F. 630, 638 (6th Cir. 1896). As we explain in greater detail below, when failure to introduce the evi-

---

[3] Post-1952 cases added to the hodgepodge of standards. *See, e.g., Standard Oil Co. v. Montedison, S.p.A.*, 664 F.2d 356, 376 (3d Cir. 1981) (rejecting the argument that the district court should have required the party to explain why it was offering evidence for the first time before the district court and holding that "new expert testimony is clearly admissible in a section 146 action without such justification"); *Velsicol Chem. Co. v. Monsanto Co.*, 579 F.2d 1038 (7th Cir. 1978) (adopting a reasonably diligent standard); *Heil Co. v. Snyder Indus. Inc.*, 763 F. Supp. 422, 426 (D. Neb. 1991) (holding that new evidence is admissible subject only to the rules of evidence). Our court previously recognized: "We are aware that this provision has received varying interpretations in the circuits. In our view, since an action under 35 U.S.C. § 146 has the hybrid nature of an appeal and a trial de novo, the statute authorizes the district court to accept all proffered testimony on issues raised by the parties during the proceedings below or by the board's decision." *Case v. CPC Int'l, Inc.*, 730 F.2d 745, 752 (Fed. Cir. 1984).

dence earlier casts doubt as to its credibility or reliability, we believe this is the correct approach.

We are not persuaded by the Director's argument that Congress intended that only evidence that could not have reasonably been presented to the Patent Office in the first instance is admissible in § 145 proceedings. In view of the language of the statute and the extensive legislative history, we agree with Mr. Hyatt that Congress intended that applicants would be free to introduce new evidence in § 145 proceedings subject only to the rules applicable to all civil actions, the Federal Rules of Evidence and the Federal Rules of Civil Procedure.

C.

The Director does not dispute that § 145, like its predecessor provisions, permits applicants to introduce new evidence in the district court proceedings. *See, e.g.*, Dir. Br. at 9, 12, 18. However, the Director contends that the applicant is only allowed to introduce new evidence that "the applicant could not reasonably have provided to the agency in the first instance." *Id.* at 9. The Director argues that this limitation stems from the rules of equity practice applicable to § 4915 actions, which would have prohibited an applicant from introducing new evidence except in limited circumstances. The Director also asserts that the APA and various policy considerations operate to impose additional limitations on an applicant's right to introduce new evidence. We address each of these arguments in turn.

1.

The Director argues that the rules of equity practice barred an applicant from introducing evidence in a

§ 4915 suit if the applicant failed, without reasonable excuse, to provide the evidence to the Patent Office in the first instance. The Director relies for this proposition on *Morgan v. Daniels*, 153 U.S. 120 (1894), where the Supreme Court characterized a suit under § 4915 as "something in the nature of a suit to set aside a judgment." *Id.* at 124. The Director argues that a suit to set aside a judgment is a specific type of bill in equity used to seek reversal of a prior decree or judgment and was called a "bill of review." The Director explains that a court presented with a bill of review to overturn a judgment would not consider any new evidence unless the plaintiff could not have obtained the evidence before the first trial without reasonable diligence. *See* Shipman, *supra*, at § 101, p. 168. The Director argues that the evidentiary constraints applicable to a bill of review applied to actions under § 4915 and, therefore, asserts that an applicant could not introduce any new evidence in a § 4915 action unless he could not reasonably have introduced it to the Patent Office in the first instance.

There are several problems with the Director's reliance on *Morgan* and the analogy to a bill of review. The Supreme Court's decision in *Morgan* does not provide support for the Director's "reasonable excuse" admissibility standard. In fact, *Morgan* does not relate to the admissibility of new evidence at all: the parties in that case did not seek to introduce any new evidence before the Circuit Court. 153 U.S. at 122. Instead, when the Supreme Court indicated that the suit under § 4915 was "something in the nature of a suit to set aside a judgement," it was referring to the standard of review applicable to Patent Office fact findings when no new evidence is introduced in the district court. The Supreme Court considered what "rule . . . should control the

[reviewing] court in the determination of this case." *Id.* at 123. The Court observed that the Circuit Court, which had required the plaintiff to provide "a clear and undoubted preponderance of proof," apparently applied the standard of review used by "an appellate court in reviewing findings of fact made by the trial court." *Id.* at 123. "The [*Morgan*] Court, in other words, reasoned strongly that a court/court review standard is *not* proper [for a court reviewing Patent Office fact findings] . . . And its reasoning makes clear that it meant those words to stand for the court/agency review standard." *Dickinson v. Zurko*, 527 U.S. 150, 159-60 (1999).

Thus, *Morgan* is a case about what standard of review ought to apply when the district court decides whether an applicant is entitled to a patent on exactly the same record that was before the Patent Office. When no new evidence is introduced, the § 145 action is "something in the nature of a suit to set aside a judgment," and the district court reviews the Patent Office fact findings for substantial evidence (i.e., according to the court/agency standard of review). *Morgan* offers no guidance on the scope of admissibility of evidence in a § 4915 proceeding. There are, however, other Supreme Court cases that have spoken to the admissibility of evidence in these types of proceedings. In *Butterworth v. Hoe*, 112 U.S. 50 (1884), the Supreme Court explained:

> It is thereby provided [in § 4915] that the applicant may have remedy by bill in equity. This means a proceeding in a court of the United States having original equity jurisdiction under the patent laws, *according to the ordinary course of equity practice and procedure.* It is not a technical appeal from the patent-office, like that authorized in section 4911,

> confined to the case as made in the record of that office, but is prepared and heard upon *all competent evidence adduced and upon the whole merits.*

Id. at 61 (emphasis added).

The *Butterworth* Court identified three circuit court cases as exemplifying "the uniform and correct practice in the Circuit Courts" with respect to suits under § 4915. 112 U.S. at 61. In each of these cases, the Circuit Court explicitly recognized that a § 4915 suit was to be heard upon all competent evidence that the parties chose to introduce, regardless of whether the evidence was or could have been provided to the Patent Office. Evidence was "competent" for admissibility purposes so long as it complied with the "rules and practice of a court of equity." *See In re Squire*, 22 F. Cas. 1015, 1016 (C.C.E.D. Mo. 1877) ("Either party, therefore, is at liberty to introduce additional evidence, or rather, to speak more accurately, the hearing is altogether independent of that before the commissioner, and takes place on such testimony as the parties may see fit to produce agreeably to the rules and practice of a court of equity."); *Butler v. Shaw*, 21 F. 321, 327 (C.C.D. Mass. 1884) ("[§ 4915] contains no provision requiring the case to be heard upon the evidence produced before the commissioner . . . and, as has been held in this and other circuits, the court may receive new evidence, and has the same powers as in other cases in equity"); *Whipple v. Miner*, 15 F. 117, 118 (C.C.D. Mass. 1883) ("[§ 4915] is, plainly, an independent, original jurisdiction which is given to the courts"). Admitting evidence in accordance with the "ordinary course of equity practice and procedure" is admitting evidence in accordance with the Federal Rules of Evidence and Civil Procedure.

The Supreme Court has consistently recognized that new evidence may be introduced in these district court proceedings. *See, e.g., Gandy v. Marble*, 122 U.S. 432, 439 (1887) (explaining that the § 4915 suit in equity was "not a technical appeal from the Patent Office, nor confined to the case as made in the record on that office"); *Hoover Co. v. Coe*, 325 U.S. 79, 83 (1945) (explaining that the bill in equity in a § 4915 action afforded applicants "a formal trial . . . on proof which may include evidence not presented in the Patent Office"). No Supreme Court case has ever placed any limitations on the admissibility of evidence in a § 145 or § 4915 proceeding apart from the ordinary rules applicable to all civil actions. To the contrary, the Supreme Court observed that the remedy by bill in equity provided by § 4915 "sav[ed] to litigants *the option* of producing new evidence in a court." *Hoover Co.*, 325 U.S. at 87. Most recently, in *Zurko*, the Supreme Court stated that "[Section 145] *permits* the disappointed applicant to present to the court evidence that the applicant did not present to the PTO. The presence of such new or different evidence makes a factfinder of the district judge." 527 U.S. at 164. Our court has likewise held that a § 145 applicant is "entitled to" and may "choose to" to introduce new evidence in the district court proceedings. *See, e.g., Mazzari v. Rogan*, 323 F.3d 1000, 1004-05 (Fed. Cir. 2003) ("A section 145 review . . . affords the applicant an opportunity to present additional evidence or argue the previous evidence afresh" and "[i]f the parties *choose to* present additional evidence to the district court . . . the district court would make de novo factual finding.") (emphasis added); *Fregeau v. Mossinghoff*, 776 F.2d 1034, 1037 (Fed. Cir. 1985) ("The [§145] proceeding, however, is not simply an

appeal since the parties are *entitled to* submit additional evidence.") (emphasis added).

To the extent that the Supreme Court precedent offers guidance on the admissibility of evidence in these proceedings, it indicates that all competent evidence is admissible subject only to the ordinary course of equity practice and procedure, which is the Federal Rules of Evidence and Civil Procedure that are applicable to all civil actions. There is no support for the Director's proposed standard, which would allow new evidence only if the evidence could not reasonably have been provided to the Patent Office.

The Director's argument also fails because the bill in equity authorized by § 4915 is not a bill in review. The Director is correct in his characterization of the admissibility rules that would apply if a § 145 proceeding was nothing more than a bill of review. As the Director points out, a party filing a bill of review could introduce new evidence only if that evidence "could not have been discovered and presented by the exercise of due diligence before the decree in question was made." Shipman, *supra*, at § 216; *see also Beard v. Burts*, 95 U.S. 434, 436 (1877). However, the bill in equity authorized by § 4915 is not a bill of review. A bill in equity was the written mechanism that began a judicial proceeding in any court of equity. *See* 1 Street, *Federal Equity Practice* § 135 (1909). A bill in equity could be either an original bill, which began "an independent suit in equity unconnected with any other previous or pending suit in the same court," or a "dependent" bill, which "relate[d] to some matter already litigated in the court by the same parties." *Id.* § 141, § 142. A bill of review was a particular type of dependent bill. *Id.* at § 146.

The bill in equity authorized by § 4915 is fundamentally different from a bill of review. Although the § 4915 action is "in fact, and necessarily, a part of the application for a patent," *Gandy*, 122 U.S. at 439, it is not a bill of review. A bill of review was a mechanism by which a court could reverse its own decree. 2 Street, *Federal Equity Practice* § 2121 (1909) ("that a bill of review will lie *only in the court where the decree to be reversed was rendered is subject to no exception whatever*") (emphasis added). The Supreme Court explained the distinction in *Barrow v. Hunton*, 99 U.S. 80 (1878): a bill in equity authorized "the investigation of a new case arising upon new facts, although having relation to the validity of an actual judgment or decree," while a bill of review involved "a mere revision of errors and irregularities, or of the legality and correctness of the judgments and decrees." *Id.* at 82-83. Because the bill in equity under § 4915 was not a bill of review, the evidentiary constraints peculiar to a bill of review do not control the admissibility of evidence in a § 145 civil action. Rather, the action is a civil action in which the district court is authorized to "adjudge that such applicant is entitled to receive a patent for his invention . . . as the facts of the case may appear." 35 U.S.C. § 145. While a § 145 proceeding is not completely independent from the prosecution process in the Patent Office, neither is it comparable to a bill of review.

Certainly, the proceedings before the Patent Office remain relevant in a § 145 action. As we explained in *Fregeau*, "in the absence of additional evidence affecting a particular finding," the district court must apply the court/agency standard of review to that fact finding. 776 F.2d at 1038. This deferential standard of review applies in recognition that the fact findings were made by

the Patent Office—the knowledgeable agency charged with assessing patentability. "On the other hand, where new evidence is presented to the district court on a disputed fact question, a *de novo* finding will be necessary to take such evidence into account together with the evidence before the board." *Id.* We have also concluded that issues (and evidence relating to new issues) that were not raised in the Patent Office proceedings generally may not be raised in a § 145 proceeding. *See Conservolite, Inc. v. Widmayer*, 21 F.3d 1098, 1102 (Fed. Cir. 1994) (listing circumstances in which new issues may be raised before the district court). Moreover, as we observed in *Fregeau*, in adjudicating entitlement to a patent, the district court must consider the record before the Patent Office as well as any new evidence admitted by the applicant. 776 F.2d at 1038. Although the Patent Office proceedings do impact § 145 proceedings in these various ways, we conclude that, consonant with the language of the statute, legislative history, and Supreme Court precedent, the only limitations on the admissibility of evidence in § 145 proceedings (for issues raised before the Patent Office) are the Federal Rules of Evidence and Civil Procedure.

Although we reject the Director's proposed restriction on admissibility, the district court may consider the proceedings before and findings of the Patent Office in deciding what weight to afford an applicant's newly-admitted evidence. As with any evidence introduced in a civil action, the weight given to evidence introduced by an applicant in a § 145 action falls within the discretion of the district court. Should the facts of a particular case cast suspicion on new evidence that an applicant failed to introduce before the Patent Office, the district court in a § 145 action would be within its discretion

to give that evidence less weight. Indeed, as discussed above, courts have considered an applicant's failure to introduce evidence before the Patent Office in determining what weight to afford to the evidence. *See Standard Cartridge Co.*, 77 F. at 638 (concluding that the evidentiary weight of new witness testimony on oral declarations supposedly made by the patentee who died and thus lost all opportunity to explain or deny was "much impaired from the fact that . . . it was not introduced during the interference proceedings"); *Western Electric Co.*, 177 F. at 228-29 (finding new recollections unconvincing: "And how comes it that the testimony of these witnesses, at this later date, comes out with so much greater definiteness than it came out at the earlier date, when, under ordinary circumstances, the event, being much more recent, ought to have been fresher in the witnesses' minds?") The practice of giving less weight to evidence whose reliability is impacted by an applicant's failure, without explanation, to provide it to the Patent Office, is entirely proper, and this practice is fully consistent with the rule that we announce today.

Quite separate from the Director's proposal, the dissent would have us rely on *Citizens to Preserve Overton Park v. Volpe*, 401 U.S. 402, 414-20 (1971) to hold that the only new evidence that we should allow is that which the applicant could not bring to the Patent Office due to the inadequacies of the Patent Office's procedures. Dissent 7- 9. First, the Director expressly rejects the applicability of *Overton Park* to § 145. Dir. Br. 19, n.4 ("We do not contend that an applicant's ability to introduce new evidence under Section 145 is limited to circumstances in which 'agency factfinding procedures are inadequate.'" citing *Overton Park*). Additionally, the statute in question in *Overton Park* only provided for "judi-

cial review" of agency action. 401 U.S. at 410. Section 145 specifically permits a "civil action" where the district court may adjudge entitlement to a patent "as the facts in the case may appear." Where the statute permits a "civil action" in relation to agency actions, the Supreme Court has held that this amounts to a trial de novo. *See Chandler v. Roudebush*, 425 U.S. 840, 845-46, 862 (1976) ("Here, by contrast, there is 'specific statutory authorization' of a district court 'civil action,' which both the plain language of the statute and the legislative history reveal to be a trial de novo."). Here, the language of the statute and legislative history support the admission of new evidence in § 145 actions subject only to the Federal Rules of Evidence and Civil Procedure.

2.

With respect to the Director's APA argument, the Director does not assert that the APA controls the admissibility of evidence in a § 145 action. To the contrary, the Director consistently acknowledges throughout his brief that new evidence is admissible in a § 145 action—unlike a typical APA action, in which judicial review is strictly limited to the administrative record. The Director's argument instead is that when no new evidence is admitted in a § 145 action, the district court must review the fact findings of the Patent Office on the administrative record and subject to the APA.

This is an uncontroversial proposition: it is well-settled that a reviewing court must apply the APA's court/agency standard of review to Patent Office fact findings when no new evidence is admitted in a § 145 action. If the parties to a § 145 action do not introduce any new evidence before the district court, the court reviews

the case on the same record presented to the agency and the reviewing court must apply the APA's substantial evidence standard to Patent Office fact findings. *See Mazzari*, 323 F.3d at 1005.

But when a party to a § 145 action does introduce new evidence, the court's review is no longer limited to the administrative record. Instead, the court must consider the new evidence in addition to the record, and "[t]he presence of such new or different evidence makes a fact-finder of the district judge." *Zurko*, 527 U.S. at 164. Because the court must determine the weight and import of this new evidence, we have held that the district court in a § 145 action must make de novo fact findings with respect to factual issues to which the new evidence relates. *Fregeau*, 776 F.2d at 1038 ("where new evidence is presented to the district court on a disputed fact question, a *de novo* finding will be necessary to take such evidence into account together with the evidence before the board"); *see also Mazzari*, 323 F.3d at 1005 ("if the parties choose to present additional evidence to the district court [§ 145 action] . . . the district court would make *de novo* factual findings if the evidence is conflicting [with the administrative record]"). The Director does not dispute that these standards of review apply in a § 145 action.

At most, the Director argues that the principles of deference to agency fact finding inherent in the APA scheme would tend to support more restrictions on the admissibility of evidence. However, this deference is already embodied in the standard of review applicable in a § 145 action. When the court reviews a case on the administrative record—that is, when no party introduces new evidence—the court applies the APA standard of

review to Patent Office fact findings. *Mazzari*, 323 F.3d at 1005. When new evidence is introduced, the court acts as a factfinder with respect to that new evidence and would make de novo fact findings if the evidence conflicts with any related Patent Office finding. *Id.*; *see also Zurko*, 527 U.S. at 164. However, the court must still consider the administrative record in making its fact findings; we have made clear that the court's de novo finding must "take [new] evidence into account together with the evidence before the board." *Fregeau*, 776 F.2d at 1038. Therefore, the dual standards of review applicable in a § 145 action maintain an appropriate level of deference to agency findings, while preserving to the court its role as factfinder with respect to new evidence.

3.

Finally, the Director presents various policy considerations in support of its proposal that evidence is not admissible unless it could not have reasonably been presented to the Patent Office first. The Director first argues that requiring plaintiffs to completely present all arguments and evidence to the agency in the first instance protects agency authority and promotes judicial efficiency. Although we agree that encouraging full disclosure to administrative tribunals is sound policy, Congress—not the Federal Circuit—must decide how best to do this. Congress heard extensive testimony on the advantages and disadvantages of providing applicants with a civil action to obtain a patent. In fact, Congress heard testimony on this very issue: the former Assistant Commissioner of Patents argued that § 4915 "should be cut out entirely for ex parte applications," to force an applicant to introduce "all the testimony pertinent to his

case" to the Patent Office. *To Amend Section 52*, 69th Cong., 1st Sess., at 76. This was a policy decision committed to the sole discretion of Congress; we may not replace Congress' judgment with our own.

The Director asserts that if we do not limit an applicant's right to introduce new evidence in a § 145 action, applicants will inevitably choose this route of review over a direct appeal under § 141 or will withhold evidence from the Patent Office to avoid generating adverse prosecution history. To deter applicants from exactly the type of procedural gaming that concerns the Director, Congress imposed on the applicant the heavy economic burden of paying "[a]ll the expenses of the proceedings" regardless of the outcome. 35 U.S.C. § 145. An applicant has every incentive to provide the Patent Office with the best evidence in its possession, to obtain a patent as quickly and inexpensively as possible. "It would be counterintuitive for an applicant to deliberately withhold non-cumulative evidence that would help persuade the BPAI to reverse the examiner's rejection, and instead . . . present it later on in a civil action when the party (as plaintiff) would be obligated to pay all the expenses—including the defendant PTO's expenses." NYIPLA Br. at 13; *see also* IPO Br. at 17 ("applicants proceeding before the PTO strike a strategic balance, submitting evidence likely sufficient to obtain a patent while avoiding overburdening the PTO"). Indeed, the fact that the vast majority of applicants pursue an on-the-record appeal instead of a § 145 action indicates that applicants generally consider the evidence before the Patent Office to be sufficient. Where an applicant decides to pursue a § 145 action, this may reflect a belief that the application at issue is or could be especially commercially significant; in such a case, the appli-

cant likely believes that the additional cost of a § 145 action may be merited. *See* AIPLA Br. at 1.

Next, the Director asserts that interpreting § 145 to allow applicants to freely introduce new evidence before the district court would disturb the rule that arguments waived in administrative proceedings may not be raised for the first time in federal court. We have held that, in general, parties may not raise issues in the district court that were not raised during the proceedings before the Patent Office or by the Board's final decision. *Conservolite*, 21 F.3d at 1102 (listing exceptions where courts may allow new evidence on new issues). However, this rule does not preclude parties from introducing additional *evidence* as to issues that were raised before the Patent Office. Here, the issue is written description—the subject of Mr. Hyatt's excluded declaration—and was raised before the Patent Office. Therefore, the doctrine of waiver is not applicable to this case.

D.

We hold that new evidence is admissible in a civil action under 35 U.S.C. § 145, subject only to the Federal Rules of Evidence and Federal Rules of Civil Procedure. We now consider whether, under this standard, the district court abused its discretion in excluding Mr. Hyatt's declaration.

The district court found that Mr. Hyatt's failure to explain why he did not submit his declaration to the Patent Office was negligent. Stating that it "need not consider evidence negligently submitted after the end of administrative proceedings," the court excluded Mr. Hyatt's declaration. *Hyatt*, 2005 U.S. Dist. LEXIS 45319, at *26. The district court erred in determining

that Mr. Hyatt's negligence affected admissibility and therefore abused its discretion in excluding the declaration.[4]

CONCLUSION

For the reasons stated herein, the district court abused its discretion in excluding Mr. Hyatt's declaration. We therefore vacate the judgment of the District Court for the District of Columbia and remand for further proceedings consistent with this opinion.

VACATED AND REMANDED

---

[4] Nothing in *In re Alton*, 76 F.3d 1168 (Fed. Cir. 1996) is inconsistent with our decision today. An applicant may respond to a written description rejection in whatever way the applicant deems effective.

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

2007-1066

GILBERT P. HYATT, PLAINTIFF-APPELLANT

v.

DAVID KAPPOS, DIRECTOR, PATENT AND TRADEMARK OFFICE, DEFENDANT-APPELLEE

Decided: Nov. 8, 2010

Appeal from the United States District Court for the District of Columbia in Case No. 03-CV-901, Judge Henry H. Kennedy, Jr.

NEWMAN, *Circuit Judge*, concurring in part, dissenting in part.

I join the en banc court's holding that new evidence may be provided in a civil action brought in the district court under 35 U.S.C. §145. However, the court also holds that when no new evidence is provided, the findings and rulings of the PTO receive the same deferential treatment in the district court as would apply if the cause were not a civil action under section 145, but instead were an Administrative Procedure Act direct appeal to the Federal Circuit under 35 U.S.C. §141. That is not the statutory plan.

The statutory plan is designed to differ from such a duplicative procedure, not to create it. Nonetheless, the court today holds that for those issues for which the applicant relies on the same evidence as was before the patent examiner, the ruling of the PTO is not determined *de novo* but is reviewed with APA deference, identically to the section 141 appeal, except that the decision is initially made by one judge in the district court, en route to three-judge review if appeal is then taken to the Federal Circuit. No party presented or even contemplated such a redundant procedure, and no *amicus* discussed it. It is contrary to statute, to precedent, and to almost two centuries of legislative policy.

Section 145 requires the district court to determine whether "such applicant is entitled to receive a patent for his invention . . . as the facts in the case may appear." Since it is a *de novo* proceeding, the PTO findings and fact-based rulings are not reviewed on the deferential "substantial evidence" standard, and the methodology of analysis of the evidence does not depend on whether the PTO had also received the same evidence. Although an applicant who chooses a section 145 civil action is quite likely to present new evidence as to some issues, on other issues the applicant may choose to reargue the evidence that was before the PTO.

Usually the evidence before the PTO consists of references cited during examination—with the applicant arguing, in a section 145 action, that the PTO misweighed or misapplied or misunderstood the evidence. Such issues are often present in a section 145 action, where they receive *de novo* determination, whether or not new evidence is adduced in the district court. The purpose of the section 145 proceeding is to achieve fresh

judicial determination of patentability issues that had been decided by the Patent Office, and to conduct this determination *de novo* on the evidence before the court, whether or not the same evidence or all of it was before the examiner. Thus, although this court's affirmation of the principle of the *de novo* section 145 action is salutary, somehow a new flaw has crept in. The court's promulgation of a different intellectual mechanism, depending on whether an issue did or did not receive evidence in addition to that which was before the examiner, creates a convoluted analytical process, a burden on the court as well as on objective analysis.

As the en banc court explains, the legislative purpose of the equity action was to assure that the courts had the last word as to entitlement to a patent. For a brief period after patent examination was renewed in 1836, only priority contests between competing inventors had judicial recourse. The Patent Act of 1839 extended judicial participation to "all cases where patents are refused for any reason whatever." As the patent statutes continued to receive legislative attention, the Court explained in *Butterworth v. Hoe*, 112 U.S. 50, 61 (1884):

> It is thereby provided that the applicant may have remedy by bill in equity. This means a proceeding in a court of the United States having original equity jurisdiction under the patent laws, according to the ordinary course of equity practice and procedure. It is not a technical appeal from the patent office . . . confined to the case as made in the record of that office, but is prepared and heard upon all competent evidence adduced, and upon the whole merits.

The Court observed that "such *de novo* determination has been the uniform and correct practice in the circuit

courts." *Id.*; *see, e.g., Ex parte Squire*, 22 F. Cas. 1015, 1016 (C.C.E.D. Mo. 1877) ("[T]he hearing is altogether independent of that before the commissioner, and takes place on such testimony as the parties may see fit to produce agreeably to the rules and practice of a court of equity.").

The Court's decision in *Dickinson v. Zurko*, 527 U.S. 150 (1999), applying the Administrative Procedure Act's standard of review to direct appeals to the Federal Circuit on the administrative record, did not deal with the section 145 civil action. Indeed, the APA recognized the preservation of previously existing judicial review mechanisms including those that provided for a trial *de novo*, stating that "[t]he form of the proceeding for judicial review is the special statutory review proceeding relevant to the subject matter in a court specified by the statute." 5 U.S.C. §703. The APA states that nothing in the judicial review provisions of the APA "limit[s] or repeal[s] additional requirements imposed by statute or otherwise recognized by law." 5 U.S.C. §559.

Neither the APA nor *Zurko* obliterated the purpose or changed the structure of the section 145 action as a full *de novo* proceeding. In preserving this traditional path, analogy is seen to tax refund suits in the district courts or the Court of Federal Claims, where "a refund suit is a *de novo* proceeding." *Democratic Leadership Council, Inc. v. United States*, 542 F. Supp. 2d 63,70 (D.D.C. 2008); *see Vons Cos. v. United States*, 51 Fed. Cl. 1, 5 (2001) ("We begin with the axiomatic principle that tax refund cases are *de novo* proceedings. *Lewis v. Reynolds*, 284 U.S. 281, 283 (1932). Factual issues in such cases 'are tried . . . with no weight given to subsidiary factual findings made by the Service in its inter-

nal administrative proceedings.' *Cook v. United States*, 46 Fed. Cl. 110, 113 (2000). *See also Dixon v. United States*, 381 U.S. 68, 74-75 (1965).").

Such a *de novo* path, whether or not on the same evidence that was before the examiner, has long characterized section 145 actions and its predecessor bills in equity. *See, e.g., Bernardin v. Northall*, 77 F. 849, 851 (C.C.D. Ind. 1897) ("The constitution and laws give a property right in his invention or discovery to an inventor, and it was the manifest legislative intent that such inventor should not be deprived of his property right in his invention until he had had his day in a court in which the party aggrieved by the determination of an executive officer might pursue his remedy judicially, according to the practice of a court of chancery.").

Legislation concerning the bill of equity/civil action consistently recognized that the proceeding is a "new suit." For example, in connection with the Patent Act of 1927 the Chairman of the House Committee on Patents, Congressman Albert H. Vestal, stated "if a party feels aggrieved, he can bring his suit in the equity court, but it is not an appeal. It is the bringing of a new suit." *To Amend Section 52 of Judicial Code and Other Statutes Affecting Procedure in Patent Office: Hearings on H.R. 6252 and H.R. 7087 Before the H. Comm. on Patents*, 69th Cong., 1st Sess. 36 (1926). The issues of patentability are determined in accordance with the laws of patentability, on original jurisdiction undisturbed by whether the same evidence was previously before the patent examiners. As summarized by Emerson Stringham, *Patent Interference Equity Suits* §7942, at 69 (1930): "A suit by a defeated applicant is an action *de novo* for the purpose of securing a patent."

No rule or protocol requires that the civil suit cannot receive *de novo* adjudication based on the same documentary evidence that was before the Patent Office. *See Central Ry. Signal Co. v. Jackson*, 254 F. 103, 105 (E.D. Pa. 1918) (observing that although the purpose of a proceeding under section 4915 "is to secure the issue of a patent, the issue of which has been refused, it does not seek that issue through a reversal of the ruling first made, but through an independent finding that the applicant is entitled upon the merits of his application to a patent"). The Court has repeatedly confirmed this understanding. *See In re Hein*, 166 U.S. 432, 439 (1897) ("The bill in equity provided for by section 4915 is wholly different from the proceeding by appeal from the decision of the commissioner. . . . The one is in the exercise of original, the other of appellate, jurisdiction."); *Gandy v. Marble*, 122 U.S. 432, 439 (1887) ("[T]he proceeding by bill in equity, under section 4915, on the refusal to grant an application for a patent, intends a suit according to the ordinary course of equity practice and procedure, and is not a technical appeal from the patent office, nor confined to the case as made in the record of that office, but is prepared and heard upon all competent evidence adduced, and upon the whole merits. . . . " (citing *Butterworth*, 112 U.S. at 61)).

The applicant may not wish, or need, to present new evidence as to every issue of patentability. P.J. Federico observed in his definitive article, "Evolution of Patent Office Appeals," that "[t]he bill in equity is not a technical appeal from a decision of the Patent Office, but is 'a suit according to the ordinary course of equity practice and procedure.'" 22 J. Pat. Off. Soc'y 838, 937 (1940). Such "ordinary course" takes up the issues that the examiner had decided adversely to the applicant, on

whatever evidence the applicant and the Patent Office present to the district court. I have come upon no legislative or precedential hint that there should be judicial deference in the equity action to the examiner's findings for those issues upon which no new evidence is presented to the court.

The history of section 145 differs from that for priority contests between competing inventors, as discussed in *Morgan v. Daniels*, 153 U.S. 120 (1894), now relied on by this court as meaning that in the absence of new evidence "the district court reviews the Patent Office fact findings for substantial evidence (i.e., according to the court/agency standard of review)." Maj. Op. 25. That interpretation is contrary to *Morgan v. Daniels* itself, for the Court there recognized that it was dealing with a different statute, "where the question decided in the Patent Office is one between contesting parties as to priority of invention." 153 U.S. at 125. Judicial review of priority contests is now codified at 35 U.S.C. §146, which expressly provides for admission of the PTO record to "have the same effect as if originally taken and produced in the suit." There is no similar provision in section 145, which instead requires the district court to adjudge entitlement to a patent "as the facts in the case may appear." Section 145 calls upon the independent judgment of the district court, whether the evidence before the court augments or simply repeats the evidence that was before the Patent Office. [1]

---

[1] The PTO Solicitor and my colleagues in dissent argue that applicants will deliberately withhold evidence in their possession, in order to spring it on the district court under section 145. I share the view of the *amici curiae* that it is unlikely that applicants will withhold winning evidence from the examiner, in favor of a multi-year and expensive civil action in the district court.

This court's new dual standard of evidentiary analysis in section 145 actions will not only come as a surprise to practitioners, but raises new problems of adjudication, for the weight of findings on various issues often must be balanced, in reaching the ultimate determination of patentability. I must, respectfully, dissent from this additional and unnecessary encumbrance on the patenting process.

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

No. 2007-1066

GILBERT P. HYATT, PLAINTIFF-APPELLANT

v.

DAVID KAPPOS, DIRECTOR, PATENT AND TRADEMARK OFFICE, DEFENDANT-APPELLEE

Decided: Nov. 8, 2010

Appeal from the United States District Court for the District of Columbia in Case No. 03-CV-901, Judge Henry H. Kennedy, Jr.

ON PETITION FOR REHEARING EN BANC

DYK, *Circuit Judge*, with whom GAJARSA, *Circuit Judge*, joins, dissenting.

In my view today's majority decision reflects a remarkable departure from settled principles of administrative law. The majority holds today that a patent applicant may decline to present his evidence supporting a patent application to the Patent and Trademark Office ("PTO"), the expert agency charged by Congress with reviewing patent applications. Instead, he may elect to present that evidence to a district court in a de novo pro-

ceeding. As the majority itself states, "We hold that 35 U.S.C. § 145 imposes *no limitation* on an applicant's right to introduce new evidence before the district court, apart from the evidentiary limitations applicable to all civil actions. . . . " Maj. op. at 5 (emphasis added). Moreover, when the district court considers that new evidence, it owes no deference to the PTO's resolution of the fact issues. Rather, the district court makes de novo findings of fact. *See id.*

The established administrative law standard, embodied in section 706 of the Administrative Procedure Act ("APA"), 5 U.S.C. § 706, requires judicial review on the agency record and submission of all relevant evidence to the agency. In general, it permits supplementation in court only when agency procedures are inadequate. *See Citizens to Preserve Overton Park v. Volpe*, 401 U.S. 402, 414-20 (1971). Here, the agency procedures are inadequate only insofar as they do not provide for live testimony.

There is no question that Hyatt's affidavit evidence here could have been submitted to the Patent Office during the examination. The PTO rules specifically provide that "[w]hen any claim of an application . . . is rejected or objected to, any evidence submitted to traverse the rejection or objection on a basis not otherwise provided for must be by way of an oath or declaration under this section." 37 C.F.R. § 1.132. The Manual of Patent Examining Procedures recognizes that section 1.132 "sets forth the general policy of the Office consistently followed for a long period of time of receiving affidavit evidence traversing rejections or objections." MPEP § 716

(8th ed. Rev. 7, Sept. 2008).[1] But the examination proceedings are based on a paper record (except for interviews with the examiner). There is no provision for the receipt of live testimony from witnesses.

As discussed below, while section 145 contemplates the introduction of live testimony (because that testimony could not be submitted to the PTO), section 145 does not provide for a trial de novo or excuse the applicant from submitting affidavit evidence to the PTO. Limiting new evidence in the section 145 action to evidence, such as live testimony, that could not be presented to the PTO in the first instance would recognize that section 145 is fully consistent with traditional administrative law standards.

Allowing a trial de novo in the district court denigrates the important expertise of the PTO, is contrary to established principles of administrative law, finds no support in the language of the statute, and is contrary to decisions of at least five other circuits. The majority opinion invites applicants to deliberately withhold evidence from the PTO in favor of a more hospitable district court forum. Today's decision reflects yet another misguided effort to craft special rules for patent cases that the Supreme Court in other cases has held to be impermissible. *See eBay v. MercExchange, LLP*, 547 U.S. 388 (2006) (overturning this court's special test for issuing permanent injunctions in patent cases); *MedImmune v. Genetech, Inc.*, 549 U.S. 118 (2007) (rejecting this court's Declaratory Judgment Act test). The major-

---

[1] The PTO rules also provide that affidavits may be submitted after final rejection "upon a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented." 37 C.F.R. § 1.116(e).

ity decision is all the more remarkable because the Court has previously rejected our efforts to craft a special rule for review of PTO decisions in *Dickinson v. Zurko*, 527 U.S. 150, 152 (1999), holding that review under section 141 must proceed under the established administrative law substantial evidence standard. I respectfully dissent.

I

The majority speaks hardly at all to the important expert role that the PTO plays in patent examination proceedings. The statute provides a variety of grounds for rejecting a patent application. In each case the inquiry is either entirely factual or has factual components. For example, questions involving anticipation, obviousness, indefiniteness, written description, and enablement typically involve fact questions that are beyond the knowledge of an ordinary layman, and must be addressed by those skilled in the particular art.

The PTO examiner corps and the Board of Patent Appeals and Interferences ("Board") possess such expertise, and the examination process is carefully structured to utilize that expertise. For example, when a patent application is received, the proposed invention is classified so that it can be given to the proper art unit, which then determines whether the application "properly belongs" in the unit and assigns the application to an examiner within the art unit with the expertise necessary to conduct a field search of the prior art. *See* MPEP §§ 903.02, 903.08, 904 (8th ed. Rev. 7, Sept. 2008). With respect to the Board, its Standard Operating Procedures state that the Chief Judge should "designate judges as the merits panel to decide ex parte appeals

based upon their legal and technical expertise." B.P.A.I., Standard Operating Procedure 1 (Revision 13) (2009), *available at* http://www.uspto.gov/web/offices/dcom/bpai/sop1.pdf.

The importance of PTO expertise in the examination process is confirmed by the history of the statute. Although the original patent act provided for examination of patents, Act of Apr. 10, 1790, ch. 7, 1 Stat. 109, 112, three years later, Congress abolished the examination of patents, and for the next three decades the United States operated under a regime of patent registration. *See* Act of Feb. 21, 1793, ch. 11, § 1, 1 Stat. 318; P.J. Federico, *Evolution of Patent Office Appeals*, 22 J. Pat. Off. Soc'y 838 (1940). This approach was found to be entirely unsatisfying.

The legislative history of the 1836 Act, substituting an examination system for the registration system, cites the following evils of the existing registration system:

> [1] A considerable portion of all the patents granted are worthless and void . . . ; [2] The country becomes flooded with patent monopolies, embarrassing to bona fide patentees, whose rights are thus invaded on all sides . . . ; [3] Out of this interference and collision of patents and privileges, a great number of lawsuits arise, which are daily increasing in alarming degree, onerous to the courts, ruinous to the parties, and injurious to society; [4] It opens the door to frauds, which have already become extensive and serious.

S. Rept. No. 24-338, at 3 (1836). In the new law in 1836, Congress created the Patent Office and the post of Commissioner of Patents, and this was intended to "establish

a check upon the granting of patents, allowing them to issue only for such inventions as are in fact new and entitled, by the merit of originality and utility, to be protected by law." *Id.* at 4.

The system created by Congress relied heavily on the expertise of the Commissioner and his staff who were responsible for evaluating the merits of patent applications. *See* Act of July 4, 1836, ch. 357 at §§ 2, 7, 5 Stat. 117, 118-20. As the legislative history reveals, the purpose of the act was to bring specialized expertise to bear on questions of patentability:

> The *duty of examination and investigation necessary* to a first decision at the Patent Office, is an important one, and *will call for the exercise and application of much scientific acquirement and knowledge of the existing state of the arts in all their branches, not only our own, but in other countries. Such qualifications in the officers charged with the duty, will be the more necessary and desirable, because the information upon which a rejection is made at the office, will be available in the final decision.* It becomes necessary, then, to give the Patent Office a new organization, and secure to it a character altogether above a mere clerkship. The competency and efficiency of its officers should correspond with their responsibility, and with the nature and importance of the duties required of them.

S. Rep. No. 24-338, at 4 (emphases added). An applicant dissatisfied with the Commissioner's decision could appeal to a "board of examiners" appointed by the Secretary of State. In creating the Board, Congress also drew on the expertise of those skilled in the art. At least one board member was "to be selected, if practicable

and convenient, for his knowledge and skill in the particular art, manufacture, or branch of science to which the alleged invention appertains." Act of July 4, 1836, ch. 357 at § 7, 5, Stat. 117, 119-20. The de novo standard in today's decision will allow applicants to bypass the PTO expertise that Congress viewed as critical to effective patent examinations.[2]

II

Today's decision not only departs from the Congressional design for the examination of patents. It also departs from settled principles of administrative law applicable to expert agency review generally and to the PTO in particular. The Supreme Court has emphasized that in general the PTO should be treated like other administrative agencies; that patent cases are subject to the same general administrative law principles under the APA; and that departure from those principles requires clear statutory language—language that is absent here.

---

[2] Allowing the applicant to bypass PTO expertise is particularly problematic where, as here, the applicant submitted multiple applications over a long period with multiple claims and multiple rejections. The '702 application at issue in this case is one of at least 39 identical applications filed by Hyatt in 1995. Appellee's Brief at 3. Indeed, Hyatt appears to have a long history before the Board as well as this court. *See, e.g.*, *Hyatt v. Dudas*, 492 F.3d 1365, 1371 (Fed. Cir. 2007) (rejecting Hyatt's claim that the examiner failed to establish a prima facie case for a lack of written description); *In re Hyatt*, 211 F.3d 1367, 1371 (Fed. Cir. 2000) (rejecting Hyatt's claim that the Board failed to analyze the claims on an element-by-element and claim-by-claim basis and affirming the Board's anticipation determination); *In re Hyatt*, No. 87-1597, 1988 WL 57813. at *2 (Fed. Cir. 1988) (holding that the examiner raised substantial questions concerning enablement, shifting the burden to applicant, who failed to offer any competent evidence to overcome the examiner's prima facie case).

See Zurko, 527 U.S. at 161-65; *In re Comiskey*, 554 F.3d 967, 974 (Fed. Cir. 2009).

Except in very rare circumstances, judicial review of administrative action is based on the agency record. *See, e.g., Camp v. Pitts*, 411 U.S. 138, 141-42 (1973); *Overton Park*, 401 U.S. at 414-20; *Axiom Res. Mgmt., Inc. v. United States*, 564 F.3d 1374, 1381 (Fed. Cir. 2009) ("The focus of judicial review of agency action remains the administrative record, which should be supplemented only if the existing record is insufficient to permit meaningful review consistent with the APA."); 33 Wright & Koch, *Federal Practice and Procedure: Judicial Review of Administrative Action* § 8306 (2006) ("[E]xcept in the rare case, review in a federal court must be based on the record before the agency and, hence, a reviewing court may not go outside the administrative record.").

As the Supreme Court stated in *Overton Park*, the circumstances under which de novo review of factual issues is appropriate are "narrow" indeed. 401 U.S. at 414. One example of such an exception is when "the agency fact-finding procedures are inadequate.[3] *Id.* at 415. This same standard could apply to PTO review. As noted earlier, the PTO in examination proceedings generally can receive affidavit evidence but cannot receive live testimony. The PTO agrees that in such circum-

---

[3] Another exception enumerated in *Overton Park* is not applicable here. De novo review is also authorized "when issues that were not before the agency are raised in a proceeding to enforce nonadjudicatory agency action." 401 U.S. at 415. This exception does not apply to section 145 cases because new issues cannot be raised in a section 145 action. *See Newman v. Quigg*, 877 F.2d 1575, 1579 (Fed. Cir. 1989) (citing *DeSeversky v. Brenner*, 424 F.2d 857, 858 (D.C. Cir. 1970)).

stances live testimony in district court may be appropriate. Appellee's Brief at 9 (noting an applicant can introduce new evidence that "the applicant could not reasonably have provided to the agency in the first instance"). For example, in a narrow class of cases under section 145, the outcome will hinge on credibility determinations, such as where there is a question about the date of reduction to practice. In such circumstances, PTO procedures may be inadequate and it makes sense to permit the district court to take live testimony under *Overton Park* to resolve credibility issues. Where credibility issues are not presented, however, there is nothing inadequate about the PTO factfinding process, and under general administrative law principles, the district court should be confined to the record presented to the PTO where the applicant could have presented the evidence in the first instance.[4]

---

[4] While the PTO states that "[w]e do not contend that an applicant's ability to introduce new evidence is limited to situations in which 'agency factfinding procedures are inadequate,'" Appellee's Brief at 19 n.4, there is little difference between the standard for the receipt of new evidence urged by the PTO and the standard I think is appropriate. The PTO agrees that new evidence that could not be submitted to the PTO may be introduced in district court. *Id.* at 29. In exceptional circumstances, the PTO apparently would allow other evidence in district court where there was a reasonable excuse for not submitting it to the PTO in the first instance and the evidence would be conclusive. *See id.* Those circumstances seem to be limited to situations where the evidence "in character and amount carries thorough conviction that the agency's decision was mistaken." *Id.* (internal quotation omitted). That describes situations where the failure to submit the evidence to the PTO would be harmless error. Where new evidence is discovered after the PTO proceeding and is presented to the district court, the district court in most instances should remand to the agency for its initial consideration.

The necessity of presenting evidence to the administrative agency in the first instance when the agency can receive the evidence is supported as well by principles of administrative exhaustion, which require that evidence and arguments both be presented in the first instance to the agency. The ordinary rule is that "no one is entitled to judicial relief for a supposed or threatened injury until the prescribed administrative remedy has been exhausted." *McKart v. United States*, 395 U.S. 185, 194 (1969) (internal quotation omitted); *see Woodford v. Ngo*, 548 U.S. 81, 90 (2006). "Exhaustion concerns apply with particular force when the action under review involves exercise of the agency's discretionary power or when the agency proceedings in question allow the agency to *apply its special expertise*." *McCarthy v. Madigan*, 503 U.S. 140, 145 (1992) (citing *McKart*, 395 U.S. at 194) (emphasis added). The majority ignores these important principles of administrative law, adopting a rule that effectively allows a patentee to decline to present his evidence supporting patent issuance to the PTO in the first instance.

III

The majority's approach also finds no support in the language of the statute. Section 145 provides:

> An applicant dissatisfied with the decision of the Board of Patent Appeals and Interferences in an appeal under section 134(a) of this title may, unless appeal has been taken to the United States Court of Appeals for the Federal Circuit, *have remedy by civil action* against the Director in the United States District Court for the District of Columbia if commenced within such time after such decision, not less

> than sixty days, as the Director appoints. The court may adjudge that such applicant is entitled to receive a patent for his invention, as specified in any of his claims involved in the decision of the Board of Patent Appeals and Interferences, as the facts in the case may appear and such adjudication shall authorize the Director to issue such patent on compliance with the requirements of law. All the expenses of the proceedings shall be paid by the applicant.

35 U.S.C. § 145 (emphasis added).[5]

Contrary to the majority, the language of section 145 providing for district court review does not in any way suggest that the proceedings should be de novo rather than generally on the agency record. Even before the 1946 enactment of the APA, *see* Act of June 11, 1946, ch. 324, 60 Stat. 237, the Supreme Court had held that provisions for district court or trial court review of agency

---

[5] The comparable provision for interference proceedings, section 146, provides:

> Any party to an interference dissatisfied with the decision of the Board of Patent Appeals and Interferences on the interference, *may have remedy by civil action*, if commenced within such time after such decision, not less than sixty days, as the Director appoints or as provided in section 141 of this title, unless he has appealed to the United States Court of Appeals for the Federal Circuit, and such appeal is pending or has been decided. In such suits the record in the Patent and Trademark Office shall be admitted on motion of either party upon the terms and conditions as to costs, expenses, and the further cross-examination of the witnesses as the court imposes, without prejudice to the right of the parties to take further testimony. The testimony and exhibits of the record in the Patent and Trademark Office when admitted shall have the same effect as if originally taken and produced in the suit.

35 U.S.C. § 146 (emphasis added).

action would not be read to imply the power to go outside the agency record. For example, in *Tagg Bros. & Moorhead v. United States*, 280 U.S. 420 (1930), the Court held that although the Packers and Stockyards Act of 1921, 7 U.S.C. §§ 181-229, provided for suits to be brought in federal district court to enjoin the enforcement of agency orders, this did not imply a trial de novo. 280 U.S. at 444-45. The Court explained:

> A proceeding under section 316 of the Packers and Stockyards Act is a *judicial review, not a trial de novo. The validity of an order of the Secretary, like that of an order of the Interstate Commerce Commission, must be determined upon the record of the proceedings before him* . . . . On all other issues his findings must be accepted by the court as conclusive, if the evidence before him was legally sufficient to sustain them and there was no irregularity in the proceeding. *To allow his findings to be attacked or supported in court by new evidence would substitute the court for the administrative tribunal as the rate-making body.* Where it is believed that the Secretary erred in his findings because important evidence was not brought to his attention, the appropriate remedy is to apply for a rehearing before him or to institute new proceedings.

Id. at 443-45 (emphases added; footnote omitted; citations omitted).

The Court disposed of similar arguments in the context of district court actions authorized by the judicial review provision of the Communications Act of 1934, 47 U.S.C. § 402(a). *See Nat'l Broad. Co. v. United States*, 319 U.S. 190, 227 (1943). The statute initially provided for "suits in equity" to "enjoin, set aside, annul, or

suspend any order or requirement of the Commission . . . . "[6] Communications Act of 1934, ch. 652, Title IV, § 402(a), 48 Stat. 1064, 1093. The Court held that such suits were not de novo, and the review was limited to the agency record: "The court below correctly held that its inquiry was limited to review of the evidence before the Commission. *Trial de novo of the matters heard by the Commission and dealt with in its Report would have been improper.*" *Id.* at 227 (emphasis added).

After enactment of the APA in 1946, the Supreme Court and other courts of appeals have repeatedly held that broad, general language such as "bill in equity" or "civil action" providing for trial court review does not create trial de novo, and that much more specific language is required. For example, in *United States v. Carlo Bianchi & Co.*, 373 U.S. 709 (1963), the Court held that "suit[s]" brought in the Court of Claims under the Wunderlich Act, Pub. L. No. 83-356, 68 Stat. 81 (1954),[7]

---

[6] This statute was later amended to transfer jurisdiction to three-judge panels of the district courts under the Urgent Deficiencies Act of 1913, 38 Stat. 208, 219. A proceeding to set aside an order of the Commission under that act was also considered "a plenary suit in equity." *Columbia Broad. Sys., Inc. v. United States*, 316 U.S. 407, 415 (1942).

[7] The statute provides:

> No provision of any contract entered into by the United States, relating to the finality or conclusiveness of any decision of the head of any department or agency or his duly authorized representative or board in a dispute involving a question arising under such contract, shall be pleaded in any suit now filed or to be filed as limiting judicial review of any such decision to cases where fraud by such official or his said representative or board is alleged: *Provided, however*, [t]hat any such decision shall be final and conclusive unless the same is fraudu-

were not trials de novo. 373 U.S. at 713-15 (1963). The Court noted that "the standards of review adopted in the Wunderlich Act—'arbitrary,' 'capricious,' and 'not supported by substantial evidence'—have frequently been used by Congress and have consistently been associated with a review limited to the administrative record." *Id.* at 715. The Court gave the following general rule:

> [T]he reviewing function is one ordinarily limited to consideration of the decision of the agency or court below *and of the evidence on which it was based.* Indeed, in cases where Congress has simply *provided for review, without setting forth the standard to be used or the procedures to be followed, this Court has held that consideration is to be confined to the administrative record and that no de novo proceeding may be held.*

Id. at 715 (emphases added). Similarly, in *Anderson v. District of Columbia*, 877 F.2d 1018 (D.C. Cir. 1989), the District of Columbia Circuit held that under the Individuals with Disabilities Education Act, which explicitly provides for a "civil action" in which the district court can hear' "additional evidence at the request of a party," 20 U.S.C. § 1415(i)(2), "[t]he authority of the district court to receive new evidence does not transform the review proceedings into a trial de novo," 877 F.2d at 1025.

There is only one feature that distinguishes actions under section 145 from agency review in other contexts. Congress has provided for a dual avenue of review—review in this court under section 141 based on the

---

lent or capricious or arbitrary or so grossly erroneous as necessarily to imply bad faith, or is not supported by substantial evidence.

41 U.S.C. § 321 (emphasis in original).

agency record and review under section 145. This suggests that the two types of review proceedings are different, and that evidence that could not be submitted to the PTO may be received in section 145 actions. But it does nothing to suggest that district court review may proceed on an entirely new record or hold de novo proceedings, or that Congress intended to do anything more than permit evidence to be presented in district court that could not be presented before the Patent Office.

The APA contemplates that statutes providing for de novo proceedings will specifically use that language. Under 5 U.S.C. § 706(2)(F), a reviewing court may "set aside agency action, findings, and conclusions" if "unwarranted by the facts[,] to the extent that the facts are subject to *trial de novo* by the reviewing court." Other federal statutes that have been held to provide for de novo review provide for such review explicitly. *See, e.g.*, Food Stamp Act, 7 U.S.C. § 2023(a)(15) ("The suit in the United States district court or State court *shall be a trial de novo* by the court in which the court shall determine the validity of the questioned administrative action in issue . . . . ").[8] This distinction has been repeatedly recognized. For example, in *Ibrahim. v. U.S.*, 834 F.2d 52 (2d Cir. 1987), the court held that,

> [t]he Food Stamp Act's de novo review provision embodies a different and broader scope of review than that available under the APA . . . [Cases requiring

---

[8] *See also* 19 U.S.C. § 1592(e) (providing that, for review of customs penalties for negligence or fraud, "[n]otwithstanding any other provision of law, in any proceeding commenced by the United States in the Court of International Trade for the recovery of any monetary penalty claimed under this section . . . all issues, including the amount of the penalty, *shall be tried de novo*").

> review on the agency record are different because there,] no statute or regulation provided for de novo review. The APA therefore governed. Here, in contrast, the Food Stamp Act specifically provides that review of FNS determinations 'shall be a trial de novo.' 7 U.S.C. § 2023(a).[9]

Id. at 53-54.

As these statutes demonstrate, when Congress intends review by de novo trial, Congress explicitly authorizes de novo trial. In the absence of specific statutory authorization, "de novo review is generally not to be presumed." *Consolo v. Fed. Mar. Comm'n*, 383 U.S. 607, 619 n.17 (1966). Section 145 does not include language providing for "de novo" review or the equivalent.

The majority is unable to point to any Supreme Court authority that has construed a statute not providing explicitly for de novo review or the equivalent as providing for such review. To be sure, the majority claims that *Chandler v. Roudebush*, 425 U.S. 840 (1976), recognizes de novo review based solely on the provision for a district court "civil action." *See* Maj. op. at 31 ("Where the statute permits a 'civil action' in relation to agency actions, the Supreme Court has held that this amounts to a trial de novo."). That is not accurate.

The *Chandler* Court found that the plain language (and legislative history) of that particular statute did provide for de novo review. *Chandler*, 425 U.S. at

---

[9] *See United States v. Ford Motor Co.*, 463 F.3d 1286, 1298 (Fed. Cir. 2006) (finding that even the explicit language of § 1592(e) should interpreted narrowly as providing for de novo review only of certain aspects of the customs determination, not to "permit an importer to end run the protest provisions").

844-46. The Civil Rights Act of 1964 provided for "civil action[s]" in district courts to redress discrimination against government employees. *Id.* at 844. Significantly, the statute also provided that "the provisions of section 706(f) through (k) as applicable shall govern civil actions brought hereunder." *Id.* at 844 (quoting 42 U.S.C. § 2000e-16(d) (1970 ed., Supp. IV)). Those sections, dealing with civil actions involving private employees, had repeatedly been interpreted as providing for a trial de novo based on specific language in the private employee provision. *Id.* at 844-45. The Court held that the incorporation of the private employee standard for a de novo trial meant that there was to be a trial de novo in government employee cases by virtue of the plain language of the statute. *Id.* at 845-46. The Court reasoned that the "terminology employed by Congress" in providing for a "civil action" in section 706, relating to private sector employees, "indicates clearly that the 'civil action' to which private-sector employees are entitled . . . is to be a trial de novo." *Id.* "Since federal-sector employees are entitled by § 717(c) to 'file a civil action as provided in section 706 [for private-sector employees] . . . [and] the civil action provided in § 706 is a trial de novo, it would seem to follow syllogistically that federal employees are entitled to a trial de novo . . . . " *Id.* Thus, based on that plain language of the statute and its legislative history, it found the general presumption against de novo review inapplicable because "here . . . there is a 'specific statutory authorization' of a district court 'civil action,' which both the plain language of the statute and the legislative history reveal to be a trial de novo." *Id.* at 862. There is no support for reading "civil action" language, standing alone, as requiring a

trial de novo. The Supreme Court's decision in *Chandler* supports that well-established rule.

IV

Additionally, the legislative history of the predecessor of section 145, when enacted in 1927, provides no support for the majority's interpretation of the statutory text. The majority relies wholly on hearing testimony. As the Supreme Court stated in *Kelly v. Robinson*, 479 U.S. 36 (1986), the Court has declined "to accord any significance to . . . statements" made in hearings. 479 U.S. at 51 n.13. Earlier, in *McCaughn v. Hershey Chocolate Co.*, 283 U.S. 488 (1931), the Court noted, "such individual expressions [as statements made in committee hearings] are with out weight in the interpretation of a statute." *Id.* at 493-94. The majority's decision here flies in the teeth of this established principle.

Even if the statements in Committee hearings could be considered relevant legislative history, the materials cited by the majority would be entitled to little weight. The 1927 legislation was based initially on a proposal drafted by the American Bar Association. *To Amend Section 52 of the Judicial Code and Other Statutes Affecting Procedure in the Patent Office: Hearings on H.R. 6252 and H.R. 7087 Before the H. Comm. On Patents*, 69th Cong. 14 (February 1926) [hereinafter *To Amend Section 52*]. The purpose of the proposal was to simplify the appeals procedure both within the Patent Office and in the courts. *Id.* at 3. Under section 4915 (section 145's predecessor) as it then existed, an appeal could be taken from the Patent Office decision to the Supreme Court of the District of Columbia. Act of March 2, 1927, ch. 273, § 11, 44 Stat. 1335, 1336-37.

Thereafter a "bill in equity" proceeding could be brought to set aside the Patent Office decision in district court. *Id.* The bills initially proposed to eliminate the appeal to the Supreme Court of the District of Columbia and to rely entirely on the bill in equity as the form of judicial review. *To Amend Section 52*, at 9.

Hearings were initially held in February of 1926 in the 69th Congress, First Session, on two separate bills. *Id.* at 1-2; *see To Amend the Statutes of the United States as to Procedure in the Patent Office: Hearings on H.R. 7563 and H.R. 13487*, 69th Cong. 5 (Dec. 1926) (explaining the prior hearings) [hereinafter *Procedure in the Patent Office*]. The quotes from the majority are taken entirely from the February 1926 hearings on bills that were not enacted into law insofar as they concerned revisions to section 4915.[10] The Commissioner of Patents objected to various provisions of the bill, and new bills were drafted reflecting substantial changes, including the creation of two alternative avenues for review —an appeal to the Court of Appeals for the District of Columbia based on the Patent Office record and the "bill in equity" procedure that would receive the full Patent Office record but allow supplementation.[11] Those

---

[10] The only bill that was enacted (H.R. 6252) concerned amendments to the jurisdictional rules in Section 52 of the judicial code and allowed parties in a 4915 action, if they resided in different districts, all to bring suit in the Supreme Court of the District of Columbia. Act of March 3, 1927 ch. 364, 44 Stat. 1394.

[11] A.C. Paul, Chairman of the Legislation Committee of the Patent Section of the American Bar Association explained, "We had a hearing before the committee on February 4, 1926. At that time some provisions of the bill were objected to by the commissioner, and after a hearing, as chairman of the legislation committee of the patent section of the American Bar Association, I undertook to see if we could get

February 1926 hearings were unlikely to be considered by members of Congress voting on a new and quite different bill in the subsequent session.

New hearings were held in December 1926 on the bill that ultimately became law (S. 4812 and H.R. 13487). In those hearings, both proponents of section 4915 (from the bar) and opponents (from the Patent Office) described the motivation for the new legislation in identical terms. While the bill in equity was characterized by some as a "de novo" proceeding or as "starting all over,"[12] those statements did not suggest that the Patent Office could be bypassed in the presentation of evidence. Indeed, the proponents viewed section 145 proceedings as involving review of PTO decisions. A.C. Paul, the Chairman of the legislation committee of the patent section of the American Bar Association viewed it as "practically another appeal." *See, e.g., Procedure in the Patent Office*, at 8. Three features are significant. First, the statute, unlike the existing provision, allowed the Patent Office record to be received in section 4915 interference proceedings, and the hearings noted the benefits of using the Patent Office record in the bill of equity proceeding. For instance, Otto Barnett explained that the bill "for the first time . . . provided that in [the bill of equity proceeding] you may use the testimony taken in the Patent Office" and that the new law

---

together and reconcile the views of the commissioner and the members of the committee, and we had negotiations extending over a number of months." *Procedure in the Patent Office*, at 5.

[12] Procedure in the Patent Office, at 11 (statement of Hon. Thomas E. Robertson, Comm'r of Patents); Amending the Statutes of the United States as to Procedure in the Patent Office: Hearings on S. 4812, 69th Cong. 10 (December 1926) (statement of Thomas E. Robertson, Comm'r of Patents) [hereinafter Senate Hearings].

was preferable because "under the present law it is all lost, and you have to start a new record." *Senate Hearings*, at 13 (Statement of Otto R. Barnett).

Second, even more significantly, the purpose of the bill was described as permitting the presentation of live testimony in the bill in equity proceeding because it could not be submitted before the Patent Office.[13] For example, Edward S. Rogers explained,

> There was a faction . . . who were in favor of doing away with section 4915 [the predecessor of section 145] . . . . It was thought inadvisable to do so, because the court, in hearing cases, will see the witnesses. *The testimony in the Patent Office hearings is all taken by deposition, and you cannot take the bearing of a man in a deposition, and frequently there are clashes in the testimony and lapses of memory, if not actual perjury. So it seems quite necessary to have the men who are to testify put on the stand in court.*

Senate Hearings, at 15 (statement of Edward S. Rogers) (emphasis added). Similarly, Commissioner of Patents Robertson noted,

> My own preference would be to repeal entirely section 4915 . . . but the bar unquestionably wants that section 4915 to continue, because *it does permit*

---

[13] The prevailing situation had been described in the earlier hearing as follows: "[E]ach applicant [in interference proceedings] is allowed to put in as much testimony as he wishes, but they do not have the same cross-examination privileges that they have in open court . . . . In ex parte cases, there is no testimony except affidavits." *To Amend Section 52*, at 37 (statements of Alexander J. Wedderburn, Patent Att'y & Karl Fenning, former Assistant Comm'r of Patents).

> *bringing the witnesses in open court which we can not have under the present procedure in the Patent Office* and so we have all agreed . . . .

Procedure in the Patent Office, at 11 (statement of Thomas E. Robertson, Comm'r of Patents) (emphasis added).[14] The purpose of the new legislation would be entirely served by allowing in the trial court only evidence that could not have been submitted to the Patent Office, such as live testimony.

Third, there was no suggestion in the December 1926 hearings, as there was in the February 1926 hearing, that applicants in the bill in equity could "bring[] in evidence that they could have brought in before [the Patent Office] but did not." To *Amend Section 52*, at 81 (statement of Thomas E. Robertson, Comm'r of Patents). That latter statement was made by the Commissioner of Patents only in February 1926 in his opposition to the bill. The omission of such statements in later hearings could well be explained by the Commissioner's receiving assurances in negotiations over the bill that it did not go that far. In any event, the earlier statement cannot be afforded any weight. As the Supreme Court noted in *Bryan v. United States*, 524 U.S. 184 (1998), "the fears and doubts of the opposition are no authoritative guide to the construction of legislation. In their zeal to defeat a bill, they understandably tend to overstate its reach."

---

[14] Commissioner Robertson also stated that "[t]he judges who decide these cases have never seen the witnesses [but if you] want a trial de novo under section 4915 you can force your opponent to come under section 4915 so that the *witnesses can be seen in court and have the testimony decided by the judges who actually see the witnesses as they testify*." *Procedure in the Patent Office*, at 14 (statement of Thomas E. Robertson, Comm'r of Patents) (emphasis added).

524 U.S. at 196 (citations, brackets, and quotation marks omitted).

Far more pertinent than the committee hearings in connection with the 1927 Act is the history of the 1952 codification. As I discuss below, at the time of the 1952 codification the courts had uniformly rejected a de novo standard in interpreting section 4915. It is fair to assume that Congress approved that interpretation in codifying the section. Congress explicitly stated that codification of section 145 made "no fundamental change in the various appeals and other review of Patent Office action . . . . " S. Rep. No. 82-1979 (1952), *reprinted in* 1952 U.S.C.C.A.N. 2394, 2400. The Supreme Court has recognized that the "evaluation of congressional action . . . must take into account its contemporary legal context," *Cannon v. Univ. of Chi.*, 441 U.S. 677, 698-99 (1979), and that "Congress is presumed to be aware of an administrative or judicial interpretation of a statute and to adopt that interpretation when it re-enacts a statute without change," *Lorillard v. Pons*, 434 U.S. 575, 580 (1978).

V

The earlier Supreme Court cases relied on by the majority do not suggest a different construction. None of the cases cited by the majority held that any and all evidence could be admitted without regard to whether it was submitted to the Patent Office. *Hoover Co. v. Coe*, 325 U.S. 79 (1945), merely states that section 145 allows for an action "on proof which *may* include evidence not presented in the Patent Office." 325 U.S. at 83 (emphasis added). Similarly, *Gandy v. Marble*, 122 U.S. 432 (1887), merely noted that section 4915 was "not a techni-

cal appeal from the patent-office, nor confined to the case as made in the record of that office" and did not explicitly state there were no limits on the evidence introduced. 122 U.S. at 439.

The majority, however, places emphasis on language in *Butterworth v. Hoe*, 112 U.S. 50 (1884), stating that in an action under section 4915 of the Revised Statutes (section 145's predecessor):

> Further provision, covering such and also all other cases in which an application for a patent has been refused, either by the commissioner of patents or by the supreme court of the district, is found in Revised Statutes, § 4915. It is thereby provided that the applicant may have remedy by bill in equity. This means a proceeding in a court of the United States having original equity jurisdiction under the patent laws, according to the ordinary course of equity practice and procedure. *It is not a technical appeal from the patent-office, like that authorized in section 4911, confined to the case as made in the record of that office, but is prepared and heard upon all competent evidence adduced, and upon the whole merits.* Such has been the uniform and correct practice in the circuit courts. *Whipple v. Miner*, 15 Fed. Rep. 117; *Ex parte Squire*, 3 Ban. & A. 133; *Butler v. Shaw*, 21 Fed. Rep. 321.

Butterworth, 112 U.S. at 61 (emphasis added).

In fact, *Butterworth* is no help to the majority for several reasons. First, *Butterworth* and the cases that it cited were all interference cases. Pre-1927 decisions of the Supreme Court and other courts in interference proceedings concerning the ability and necessity of cre-

ating a new record in bill in equity proceedings are of no value in interpreting the 1927 legislation. That legislation worked a major change on interference proceedings. The 1927 law explicitly provided that, for the first time, the PTO record would be received in the bill in equity interference proceedings and that "when admitted shall have the same force and effect as if originally taken and produced in the suit." Act of March 2, 1927, ch. 273, § 11, 44 Stat. 1335, 1337 (1927). Previously in the bill in equity proceedings, the Patent Office record, because of the informal procedures followed in the Patent Office, was viewed as having secondary value, and it was necessary to create a new *duplicate* record in the trial court.[15] This was recognized both in the hearings on the 1927 legislation (as noted above) and in subsequent court cases. As the Third Circuit explained,

> [T]he evidence given in the interference proceedings could be introduced only as secondary evidence, after proper foundation laid. The competency of such evidence had to be determined according to the principles of equity jurisprudence. In other words, the witnesses who had testified in the interference proceedings had to testify anew in the suit in the district court. If they did not so testify their absence had to be accounted for in the usual way if the testimony taken in the interference was to be received as secondary evidence. The [1927] amendment was passed to avoid this arduous and expensive means of reproducing the evidence of the interference proceedings in the suit.

---

[15] To be sure, in some cases the case did proceed based on the PTO record. *See, e.g., Morgan v. Daniels*, 153 U.S. 120, 124 (1894).

Gen. Talking Pictures Corp. v. Am. Tri-Ergon Corp., 96 F.2d 800, 812 (3d Cir. 1938) (citations omitted). Under these circumstances, pre-1927 court cases naturally referred to the creation of a new record in the bill in equity proceedings. Under the 1927 legislation the legislation of a new record in interferences became unnecessary. The legislation provided that the Patent Office record would be received and left it to the trial court to determine what additional cross examination and new testimony could appropriately be received.[16]

Second, *Butterworth* did not address the question whether evidence was required to be submitted to the Patent Office in the first instance if it was later to be used in bill in equity proceedings. The sole issue decided in *Butterworth* was whether the Secretary of the Interior could override the Patent Office decision approved by the court in a proceeding under section 4915.

---

[16] Although sections 145 and 146 stem from the same root, namely, R.S. § 4915, they are distinct because they have different content and contain different procedures for admitting evidence. In section 145 ex parte proceedings, the Patent Office is a direct party to the action whereas in section 146 interferences, the two private parties to the interference are the parties in interest. Section 146 explicitly addresses the optional procedure for admitting the entire administrative record, and such language is absent from section 145 because the administrative record is automatically admitted in judicial review proceedings. Thus, it is inaccurate to conflate sections 145 and 146 with regard to admissibility. Section 145 could be construed as a "mongrel" cause of action in the same sense that claim construction is "a mongrel practice," as Justice Souter noted in *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 378 (1996). Once again, as in *Zurko*, the majority is attempting to develop a distinction between patent administrative law and the traditional administrative agency procedure. In doing so, it fails to focus on the core of the matter, namely the discretion of a district court regarding the admissibility of evidence in a section 145 case.

112 U.S. at 54, 62, 68-69. The language of *Butterworth* is at best ambiguous. Like the other Supreme Court cases, it recognizes that new evidence may be received and considered in the trial court proceedings, *id.* at 61, but it says nothing about whether that evidence had to be submitted to the Patent Office in the first instance if such a submission were possible.

The three cases cited in *Butterworth* are no more illuminating. *Whipple* simply held that the trial court proceeding was an "original proceeding" and that the trial court could generally not enjoin issuance of a patent pending its outcome. 15 F. at 117-18. *Butler* held that for interference cases the 4915 proceeding could be invoked without first appealing to the Supreme Court of the District of Columbia, and noted that "the court may receive new evidence and has the same powers as in other cases in equity." 21 F. at 326-27. Again, what new evidence could be heard remained unclear. In the third case the court rejected the contention that the court was confined entirely to the record before the Patent Office, holding that in addition to the Patent Office records "new and additional testimony" could be received in the equity proceedings. *In re Squire*, 22 F. Cas. at 1016. But again, the court was considering only a proposed blanket bar on new evidence; it did not consider whether the substance of testimony could be withheld from the Patent Office in the agency proceeding if the Patent Office could receive and consider it.[17]

---

[17] The language quoted by the majority is not in fact from *Squire* itself but from the earlier case of *Atkinson v. Boardman* quoted in *Squire* as part of the background description. *See Atkinson v. Boardman*, 2 F. Cas. 97 (C.C.N.Y. 1851).

Third, *Butterworth*'s reference to "the ordinary course of equity practice and procedure" and "competent evidence" suggests meaningful limits on the admissibility of new evidence in section 4915 proceedings. *See* 112 U.S. at 61. As the Supreme Court explained in *Morgan v. Daniels*, a bill in equity[18] in the context of section 4915 was

> *an application to the court to set aside the action of one of the executive departments of the government.* The one charged with the administration of the patent system had finished its investigations and made its determination with respect to the question of priority of invention. That determination gave to the defendant the exclusive rights of a patentee. A new proceeding is instituted in the courts—a proceeding to set aside the conclusions reached by the administrative department, and to give to the plaintiff the rights there awarded to the defendant. *It is something in the nature of a suit to set aside judgment*, and such, is not to be sustained by a mere preponderance of evidence.

---

[18] A "bill in equity," also termed a "bill of complaint," was the initial pleading that invoked the jurisdiction of the courts of equity. *See* Federal Equity Rule 25 (1913). Equity courts recognized various species of bills, depending on the nature of the relief sought. The "bill of review" was a type of bill in equity seeking a reversal or modification of a prior decree or judgment. *See, e.g., Kingsbury v. Buckner*, 134 U.S. 650, 671-72 (1890); *Thompson v. Maxwell*, 95 U.S. 391, 395-96 (1877) ("It is manifest that the object of this bill, especially after being amended, was to set aside the decree made in the original cause, and to substitute therefor a new decree supposed to be more advantageous to the complainants, upon the same matters which were before the court and under its consideration in the said cause. Under the guise of a bill for quieting title it was in reality a bill of review.").

153 U.S. 120, 124 (1894) (emphases added); *see also Fregeau v. Mossinghoff*, 776 F.2d 1034, 1037 (Fed. Cir. 1985) (applying *Morgan* to section 145 and noting that "an action under § 145 is . . . in essence a suit to set aside the final decision of the board, like the bill in equity from which it was derived"). Under settled principles of federal equity practice, a court presented with a bill to set aside a prior judgment would not rehear arguments or evidence that had been adjudicated in the prior proceeding, nor would it consider evidence that could have been produced during that proceeding in the exercise of reasonable diligence. Rather, the court would limit its review to (1) legal errors apparent on the face of the decree and (2) new evidence of such compelling character as to call into doubt the outcome of the prior proceeding. *See, e.g., Beard v. Burts*, 95 U.S. 434, 436 (1877); *Scotten v. Littlefield*, 235 U.S. 407, 411 (1914).

In *Beard*, the Court explained:

> To sustain a bill of review, there must be errors of law apparent on the face of the decree, or some *new matters of fact material in themselves, and discovered after the rendition of the decree.* This is the general rule in equity . . . . The facts are not open for a re-trial, unless the bill asserts that new evidence has been discovered, not obtainable before the first trial by the exercise of reasonable diligence.

Beard, 95 U.S. at 436 (emphasis added).[19] Thus, federal courts in equity rejected attempts to litigate, through a bill of review, factual questions that could have been raised in the prior proceeding. *See id.* at 436; *Purcell*, 71 U.S. (4 Wall.) at 521 (rejecting petitioner's bill in equity because the complainant "offers no new evidence, but what he might as well have produced before"). These basic principles of equity practice would have been familiar to Congress in 1836, when it first authorized a "remedy by bill in equity" for applicants aggrieved by the final determination of the Commissioner of Patents. *See* Act of July 4, 1836, ch. 357, § 17, 5 Stat. 117, 124. Thus, the ordinary rules of equity practice tolerated nothing like the de novo relitigaation that the majority adopts.

Finally, and most significantly, none of the cases subsequent to *Butterworth* has interpreted it, or the cases that it cited, to require de novo review under the 1927 legislation. The Supreme Court has never directly addressed the de novo review issue. The only Supreme Court case to address the scope of section 145 after passage of the 1927 Act, *Dickinson v. Zurko*, 527 U.S. 150 (1990), does not address the issue of the scope of section

---

[19] *See also Scotten*, 235 U.S. at 411 (explaining that a bill of review encompassed only manifest legal errors and "new facts discovered since the decree, which should materially affect the decree and probably induce a different result"); *Purcell v. Miner*, 71 U.S. (4 Wall.) 519, 521 (1866) ("By Lord Chancellor Bacon's rules, it was declared: 'No bill of review shall be admitted except it contain either error in law appearing in the body of the decree without further examination of matters in fact, or some new matter which hath arisen in time after the decree; and not on any new proof which might have been used when the decree was made."); *Whiting v. Bank of United States*, 38 U.S. (13. Pet.) 6, 13-14 (1839).

145 with regard to new evidence. *Zurko* involved the question of what was the proper standard of review on direct appeal to the Federal Circuit under 35 U.S.C. § 141. *Id.* at 152-53. Although the Supreme Court noted that a section 145 claimant can "present to the court evidence that the applicant did not present to the PTO," the Court said nothing about when or under what circumstances such evidence could be introduced. *See id.* at 164. The decision in *Zurko* in fact undermines the majority's holding both by recognizing the importance of applying traditional administrative law principles to the PTO and in recognizing that the "PTO is an expert body" that "can better deal with the technically complex subject matter" of patent applications than the federal courts. *Id.* at 160. As will be seen in the next section, *Butterworth* has never been seen by other courts of appeals as barring limitations on new evidence that could have been presented to the Patent Office under the 1927 Act.

VI

The majority opinion is, in fact, contrary to decades of circuit authority under the 1927 legislation, after *Butterworth*, recognizing limits on the admissibility of new evidence in section 145 and section 146 proceedings. One of the more influential cases on the admissibility of evidence is *Barrett Co. v. Koppers Co.*, 22 F.2d 395 (3d Cir. 1927), decided several months after the passage of the 1927 legislation. There, during interference proceedings in the Patent Office, the Barrett Company instructed its employees not to answer questions about certain of its "commercial practices." *Id.* at 396. The Barrett Company lost the interference, and then filed a bill in equity under Revised Statutes § 4915 and sought to introduce

before the district court the exact testimony it had instructed its employees not to provide during the interference. *Id.* The Third Circuit found that the district court properly exclude this evidence, saying:

> The law gave the plaintiffs a day in court on the issue of priority. That was the day the interference was heard and if they chose not to avail themselves of their full rights but to gamble on the decision by giving only a part, and the weaker part, of the evidence they had in hand, they did it at their own risk. After losing on such evidence in what otherwise would be a train of futile appeals in the patent tribunals and Court of Appeals of the District of Columbia they cannot come into a District Court and say, now for the first time we shall tell the true story of reduction to practice and demand a patent.
>
> . . . When, as in this case, a party has refused to produce evidence for consideration by the Court of Appeals of the District of Columbia and then in the statutory action under section 4915, R.S., *produces that very evidence to overcome the effect of that court's decision, he comes very close to trifling with the courts' processes.* If in this case the Court of Appeals of the District of Columbia was wrong it was because the plaintiffs purposely kept it in the dark. If now this court were in effect to reverse the decision of that court on evidence brought to light for the first time, we should be assisting the plaintiffs to profit by their own technical wrong doing.
>
> . . . Particularly are we anxious that no one should think that we hold that any evidence not before the Court of Appeals of the District of Columbia is inadmissible in an action under section 4915, R.S. Such

> a notion would destroy the action given by section 4915, R.S. and throw overboard the whole doctrine of *Morgan v. Daniels*. Specifically our decision is that the plaintiffs in this action under section 4915, R.S., are *estopped to offer evidence which was wholly within their possession and control at the interference proceeding* and which they withheld from that proceeding and, therefore, withheld from the other patent tribunals and the Court of Appeals of the District of Columbia, and thereby made it impossible for those tribunals and that court to render what they, the plaintiffs, now maintain is the right decision.

Id. at 397 (formatting altered; emphasis added).

Subsequent to *Barrett*, three circuits—the District of Columbia, the Seventh, and the Eighth—have essentially followed the *Barrett* rule. The District of Columbia Circuit in *Cal. Research Corp. v. Ladd*, 356 F.2d 813 (D.C. Cir. 1966), adopted a negligence standard to limit the introduction of new evidence in a section 145 proceeding and explained that a section 145 action "may not be conducted in disregard of the general policy of encouraging full disclosure to administrative tribunals." *Id.* at 821. The Seventh Circuit adopted a "reasonably diligent" standard for determining whether evidence is admissible in a section 146 interference proceeding. In *Velsicol Chem. Corp. v. Monsanto Co.*, 579 F.2d 1038 (7th Cir. 1978), it held "that absent special circumstances, the proper question for the district court was whether the failure of the proponent of the additional evidence to uncover its existence earlier or to procure it for the interference proceeding occurred in spite of the proponent's diligence in preparing his case before the Board." *Id.* at 1046. The court cited the "policy of encouraging

full disclosure" to the administrative tribunal as the reason for this limitation. *Id.*; *see also Globe-Union v. Chi. Tel. Supply Co.*, 103 F.2d 722, 728 (7th Cir. 1939) ("We do not dispute the soundness of the proposition that all pertinent evidence, actually available, should be submitted in the first instance. To permit partial presentation before the Patent Office is to sanction *the destruction of administrative justice.*" (emphasis added)).

The Eighth Circuit adopted the rule that "deliberate, intentional, or willful withholding or suppression of pertinent and available evidence from the Patent Office, whether attended by reprehensible motives or not, whether it be for tactical or other reasons, justifies exclusion of such evidence in a section 146 proceeding." *Kirschke v. Lamar*, 426 F.2d 870, 874 (8th Cir. 1970). The court reasoned that a section 146 proceeding was not a "full trial de novo; rather, allowance of evidence in addition to the Patent Office record must be tempered and circumscribed to some degree to effectuate the policy favoring full disclosure to administrative tribunals." *Id.*

Although subsequent to *Barrett* the Third and Second Circuits limited the exclusion to testimony intentionally suppressed, their holdings too are inconsistent with the majority's approach here. The Third Circuit continued to hold that intentionally suppressed evidence must be excluded.[20] The Second Circuit, which origi-

---

[20] *See Minn. Mining & Mfg. Co. v. Carborundum*, 155 F.2d 746, 748 (3d Cir. 1946) (distinguishing *Barrett* and allowing expert testimony that was not intentionally suppressed at the time of the Patent Office proceedings). Although another later Third Circuit case, *Standard Oil Co. v. Montedison, S.P.A.*, 664 F.2d 356, 376 (3d Cir. 1981), stated that "new expert testimony is clearly admissible in a section 146 proceeding

nally approved of *Barrett*, *see Greene v. Beidler*, 58 F.2d 207, 208-09 (2d Cir. 1932), later suggested an exclusion might be limited to evidence "suppressed," not "merely neglected through the plaintiffs slackness in preparation," *Dowling v. Jones*, 67 F.2d 537, 538 (2d Cir. 1933).

Not a single court of appeals case has interpreted section 145 as permitting the submission of any and all new evidence. Although the cases suggest varying standards for the admission of new evidence, they all acknowledge the necessity of establishing significant limitations on the admission of new evidence, and recognize that to provide otherwise would undermine the requirement of administrative exhaustion. Today's decision represents an anomalous and unjustified departure from prevailing circuit authority.

VII

The majority suggests that one should not be too concerned about its special rule for patent cases because general evidentiary principles will somehow allow the district court to discount evidence not submitted to the PTO and thus reach the same result at least in some cases. *See* Maj. op. at 30-31. This approach is remarkably similar to the argument rejected in *Zurko* where it was suggested that there was no meaningful difference between the APA substantial evidence standard and the clearly erroneous standard for review of PTO decisions. The Supreme Court concluded that while the differences

---

without [showing special circumstances explaining why the testimony was not presented first to the Board] to the extent that it aids the court in understanding issues presented to the Board," the court was apparently responding to an attempt by the objecting party to place the burden of justifying the evidence on the party offering it.

were "subtle" and might not affect many cases, the differences were nonetheless important. *Zurko*, 527 U.S. at 161-65. Even if here the majority were right as to the consequences, this would not support application of the wrong law, as *Zurko* makes clear.

But the majority is not right as to the consequences, and there is nothing subtle about the difference between excluding evidence and admitting it. The evidentiary cases cited by the majority offer no support for discounting evidence not submitted to the PTO on grounds that it would be too costly to do so, and the majority offers applicants a ready made excuse—the costs of making a full record before the PTO—for the withholding of evidence under such circumstances.[21] The rules of evidence do not remotely offer a different path to the same result.

In conclusion, I note the quite arresting policy argument made by the majority for permitting applicants to bypass the PTO—that the applicant would bypass the PTO in favor of a de novo district court proceeding only

---

[21] The majority suggests that two cases from the turn of the last century recognize that "courts have considered an applicant's failure to introduce evidence before the Patent Office in determining what weight to afford to the evidence." Maj. op. at 30. The limited holdings of these cases impose no meaningful limits. The first simply recognizes that a witness' new explanation, not offered in his Patent Office declaration, was not credible. *W. Elec. Co. v. Fowler*, 177 F. 224, 228-29 (7th Cir. 1910). The second recognizes that prior consistent declarations of a witness in the PTO proceeding, only introduced in district court after the witness had died, would be given little weight in evaluating the witness' earlier testimony. *Standard Cartridge Co. v. Peters Cartridge Co.*, 77 F. 630, 638 (6th Cir. 1896). These cases impose no limit on new evidence presented by new witnesses whose declarations were not supplied to the PTO.

in cases where the patent is commercially significant and the costs of a separate proceeding can be justified. *See* Maj. op. at 30-31. But those are exactly the cases in which PTO review is most important. In such cases, contrary to the majority, it is not somehow fantastic to imagine that applicants will elect to bypass the PTO in favor of a second bite at the apple in the district court. They will do so exactly in those circumstances where an expert agency would reject the evidence but a non-expert district court might be convinced to accept it. A more pernicious approach is difficult to imagine.

APPENDIX B

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

No. 2007-1066

GILBERT P. HYATT, PLAINTIFF-APPELLEE

v.

JOHN J. DOLL, ACTING DIRECTOR, PATENT AND TRADEMARK OFFICE, DEFENDANT-APPELLEE

[Filed: Aug. 11, 2009]

Before: MICHEL, Chief Judge, DYK and MOORE, Circuit Judges.

Opinion for the court filed by Chief Judge MICHEL. Dissenting opinion filed by Circuit Judge MOORE.

MICHEL, Chief Judge.

Plaintiff-Appellant Gilbert P. Hyatt appeals from the grant of summary judgment in favor of Jon Dudas, in his official capacity as the Director of the United States Patent and Trademark Office ("PTO"),[1] sustaining the decision of the Board of Patent Appeals and Interferences ("Board") to uphold the examiner's rejection of 79 of the 117 claims of Hyatt's U.S. Patent Application Serial No. 08/471,702 ("the '702 application") as not sup-

---

[1] Pursuant to Federal Rule of Appellate Procedure 43(c)(2), John Doll was substituted for Dudas upon Dudas's resignation as Director.

ported by adequate written description. The appeal was argued on April 7, 2008. It is clear from the record that under our caselaw Hyatt had an affirmative and specific duty to disclose to the PTO the evidence excluded by the district court, and was so notified by the PTO, but willfully refused to cooperate in the examination process. On the facts of this case, we uphold the district court's exclusion of Hyatt's evidence. We therefore hold that the district court correctly granted summary judgment sustaining the Board decision because Hyatt offered no other evidence and the Board's decision was based on findings of fact and factual conclusions, all of which are supported by substantial evidence, and thus we affirm.

I.

A. Proceedings Before the Examiner

Hyatt is the sole listed inventor on the '702 application. Hyatt has been registered as a patent agent since 1975 and prosecuted the application wholly on his own.[2]

The '702 application relates to computer and software technology and is entitled "Improved Memory Architecture Having a Multiple Buffer Output Arrange-

---

[2] Hyatt is also familiar with this court. *See Hyatt v. Dudas*, 551 F.3d 1307 (Fed. Cir. 2008); *Hyatt v. Dudas*, 267 Fed. Appx. 944 (Fed. Cir. 2008); *Hyatt v. Dudas*, 492 F.3d 1365 (Fed. Cir. 2007); *in re Hyatt*, 243 F.3d 554 (Table) (Fed. Cir. 2000); *In re Hyatt*, 211 F.3d 1367 (Fed. Cir. 2000); *Hyatt v. Boone*, 146 F.3d 1348 (Fed. Cir. 1998); *In re Hyatt*, 108 F.3d 1393 (Table) (Fed. Cir. 1997); *In re Hyatt*, 106 F.3d 424 (Table) (Fed. Cir. 1996); *In re Hyatt*, 925 F.2d 1478 (Table) (Fed. Cir. 1991); *In re Hyatt*, 852 F.2d 1292 (Table) (Fed. Cir. 1988); *In re Hyatt*, 770 F.2d 182 (Table) (Fed. Cir. 1985); *In re Hyatt*, 770 F.2d 181 (Table) (Fed. Cir. 1985); *In re Hyatt*, 770 F.2d 178 (Table) (Fed. Cir. 1985); *In re Hyatt*, 714 F.2d 160 (Table) (Fed. Cir. 1983); *In re Hyatt*, 708 F.2d 712 (Fed. Cir. 1983); *In re Hyatt*, 714 F.2d 160 (Table) (Fed. Cir. 1983).

ment." Hyatt filed the '702 application on June 6, 1995. J.A. 10001. The '702 application is a continuation or continuation-in-part of several earlier applications, some of which were themselves continuations or continuations-in-part. J.A. 10004. When first filed, the '702 application claimed priority back to 1984; Hyatt later amended the application to claim priority back to 1975. J.A. 10756-57.

The '702 application as originally filed had 15 claims, a 238-page specification, and 40 pages of drawings. J.A. 10000-293. It also incorporated by reference multiple publications (such as the "Texas Instruments, ALS/AS Logic Circuits Data Book, 1983"), J.A. 10173-74, and a "disclosure document ha[ving] copies of many of" a list of referenced documents; on the list were manuals and specification sheets of products such as the "Viewpoint/3A Plus" and the "Siemens OEM Floppy Disk Drive FDD 100-8". J.A. 10239-40. After several rounds of amendments to the specification and the claims, Hyatt ultimately cancelled all 15 original claims and added 117 new claims. J.A. 4. New claim 107 is not atypical:

A process of operating a memory system comprising the acts of:

generating input image information;

storing a two dimensional array of blocks of pixel image information by a two dimensional pixel block memory, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information, wherein the blocks of pixel image information have boundaries there between;

generating write addresses and generating read addresses;

writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory in response to the input image information and in response to the write addresses;

generating a first clock signal having a first clock rate;

accessing blocks of pixel image information in response to the read addresses, wherein the accessing of blocks of pixel image information from the two dimensional pixel block memory is at a first information rate in response to the first clock signal;

generating block boundary smoothing information to smooth the pixel image information at boundaries between blocks of pixel image information;

storing weight information by a weight memory;

generating accessed weight information by accessing the weight information stored by the weight memory;

generating smoothed weighted image information by weighting the pixel image information contained in the accessed blocks of pixel image information in response to the accessed weight information and in response to the block boundary smoothing information;

generating a second clock signal having a second clock rate that is different than the first clock rate of the first clock signal; and

> generating output smoothed weighted image information in response to the smoothed weighted image information, wherein the generation of the output smoothed weighted image information is at a different information rate than the first information rate in response to the second clock signal.

J.A. 10472-73.

In a January 7, 1997 office action, the examiner described Hyatt's final amendment as incomplete, stating:

> Applicant also has failed to point out where in the specification support may be found for the amended and added claims. MPEP 714.02 states "Applicant should also specifically point out the support for any amendments made to the disclosure." The disclosure includes the claims.
>
> Since the response appears to be *bona fide*, but through an apparent oversight or inadvertence failed to provide a complete response, applicant is required to complete the response within a TIME LIMIT of ONE MONTH from the date of this letter or within the time remaining in the response period of the last Office action, whichever is longer.

J.A. 10493. Hyatt responded a month later with further amendments to the specification and drawings J.A. 10498-503. and the following indication of where support for the 117 new claims and amendments to the specification could be found:

> Representative antecedent basis includes page 23:2-19 for data compression; page 50:6-9 for the frame buffer; the section entitled "LOGIC BOARD" "Address Generators" at pages 117-127 for the ad-

dress generator; the section entitled "MEMORY ARCHITECTURE" at pages 25-62 and the section entitled "MEMORY BOARDS" at pages 128-135 for the block memory having accessing, writing, and processing circuits; the section entitled "GRAPHICS PROCESSOR" at pages 9-14, the program listing at pages 214-30, and pages 29-31, 41, 42, 45, and 50 for the vector generator and processor; the section entitled "SPATIAL FILTERING" pages 15-24 and the program listing at pages 231-236 for the spatial processor; and pages 33:15-24:11 for the transform processor.

The Examiner is further referred to the Table of Contents (see the Preliminary Amendments) for additional antecedent basis.

J.A. 10504-05.

In October 1997, the examiner issued a final office action rejecting all 117 of Hyatt's claims for lack of adequate written description, lack of enablement, double patenting, anticipation, or obviousness. J.A. 10634-64. The examiner rejected groups of claims for lack of written description and enablement based on the following thirteen limitations and groups of limitations:

- "a data decompressed video image input circuit generating data decompressed image information"
- "a writing circuit and an accessing circuit for writing and reading a block of video pixel image data into the block memory" and "the process of writing and reading a block of video pixel image data into the block memory"

- "a vector processor responsive to an accessed block of video pixel image information and to vector information"
- "a processor responsive to an accessed block of video pixel image information"
- "a spatial processor responsive to an accessed block of video pixel image information and to vector information and generating data compressed video"
- "a frequency domain processor," "generating frequency domain image information," and "frequency domain information"
- "a block processor responsive to an accessed block of pixel image information and to vector information"
- "[a]n input weight circuit generating input weight information," "an address generator which will generate weight addresses," "an address generator which will apply the weight addresses to the inputs of RAMS U5E and U6E at the same time the intensity bits are being applied to RAMS U3E and U4E," and "an address generator which will generate weight addresses for selecting weight values from the weight table to perform the desired weighting function at the spatial filter" (collectively, "the 'weight' limitations")
- "block boundary smoothing"
- "that the memory system is a video image data compression system"
- "a quantization weighting processor"

- "generating data compressed video image information"
- "the act of making a product in response to image information"

J.A. 10638-56. In some of his written description rejections, the examiner indicated the closest match he could find between the claim language and the disclosure of the specification. For example, the examiner stated "Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, 95-112, 117, and 188 claim a writing circuit and an accessing circuit for writing and reading a block of video pixel image data into the block memory. These claims cover *simultaneous* writing and reading of a block of graphic image data . . . . The specification describes a sequential write to and read from the block memory." J.A. 10641. For the majority of the written description rejections, however, the examiner merely stated a claim limitation—such as "a quantization weighting processor," "a video image data compression system," and "a spatial processor responsive to an accessed block of video pixel image information and to vector information and generating data compressed video"—was "not enabled" or "not described in the specification." *See, e.g.*, A10645, 10652-53.

B. Proceedings Before the Board

In September 1998, Hyatt—continuing to represent himself—appealed the examiner's final rejection to the Board. J.A. 10936. Hyatt's brief presented such arguments as "The '112-1 rejections are *prima facie* erroneous because the disclosure is presumptively valid and correct," J.A. 10824, "The disclosure is significant

. . . , comprising over 200 pages of description **with detailed schematic diagrams** showing actual commercially available electrical **components** in well known schematic symbol form and even showing component **pin** designations and **wire** connections," J.A. 10827, and "With the extensive memory disclosure (*e.g.*, Spec. at 99-135) and processor disclosure (e.g., Spec. at 87-98, 214-36) in the instant application, it is unbelievable that the Examiner would object to the disclosure of memory and processor features," J.A. 10831. In addition, he included a document entitled "Table-1" (reproduced below), which he had not provided to the examiner, purporting to give examples of support:

TABLE-1

REPRESENTATIVE TERMINOLOGY	*NOTES* [22]	*OCCURRENCES*	*REPRESENTATIVE CITES PAGE(S)*
access	A	>100	25-83, 128-164
address	A	>500	25-83, 128-164
block	A	>80	25-83, 128-164
boundary		=3	14, 41
compress		=4	23
data compressed		=1	23
decompressed		=1	23
frequency (FFT)	C	=7	33-34
graphic	D	>20	9-14, 214-230
image		>50	50-55
information		>100	THROUGHOUT
input		>200	THROUGHOUT
memory	A	>400	25-83, 128-164
pixel		>300	THROUGHOUT
processor		>50	85-98
quantization	E	>100	231-236

read	A	>50	25-83, 128-164
simultaneous		>8	36, 45, 46, 50
smoothing		=1	232
spatial	B	>20	15-24, 231-236
vector	D	>50	9-14, 214-230
video		=8	77, 166, 168-171
weight	F	>100	162-164
write	A	>100	25-83, 128-164

J.A. 10832-34. In accompanying notes, Hyatt asserted that certain broad categories of "terminology" were disclosed in certain textual sections of the specification and in raw source code appearing in the specification. J.A. 10833-34. For example, in note "A" (associated with the terms "access," "address," "block," "memory," "read," and "write"), Hyatt stated that

> Memory terminology; including memory access, memory read, memory write, and memory block terminology; is disclosed, for example, in **two whole sections** entitled "MEMORY ARCHITECTURE" and "MEMORY BOARDS" (Spec. at 25-62 and 128-35 and Figs. 6E-6N) and in **two additional whole sections** entitled "BUFFER MEMORY" and "BUFFER BOARD" (Spec. at 63-83 and 136-58 and Figs. 6W-6AF).

J.A. 10833. Although Hyatt presented thirty-six pages of general argument that the written description and enablement rejections should be reversed, J.A. 10823-58, Hyatt did not separately address—and did not indicate where in the specification support could be found for—any of the claim limitations the examiner determined lacked support, except for the limitation "making a product," J.A. 10836-40, and the group of "weight" limita-

tions. J.A. 10835. Hyatt made general statements that Table-1 and the table of contents of his specification indicated that support for the relevant limitations existed in his specification. J.A. 10827, 10831. Hyatt also argued that lists of twenty-nine publications had been incorporated by reference into the specification and provided enabling disclosure. J.A. 10848-51. Aside from the "making a product" and the "weight" limitations, Hyatt did not correlate Table-1, his table of contents, or any of the incorporated-by-reference publications with particular limitations.

Although reversing some of the examiner's written description and enablement rejections, the Board sustained the written description and enablement rejections for seventy-nine claims in a July 2002 decision. J.A. 11638. The Board addressed each of the claim limitations relied on by the examiner. The Board rejected Table-1 as unhelpful in identifying written description support:

> We agree with the examiner that merely pointing to isolated words scattered throughout the specification does not describe the invention claimed as a combination of elements, functions, and interconnections, anymore than a dictionary provides written description support for a book where words are used in combination to provide a certain meaning.

J.A. 11594. The Board even considered Table-1 "misleading" in that it indicated that the word "quantization" appeared in the specification, while the specification actually contained the "%" symbol and the arithmetic functions "FIX(exp)" and "INT(exp)." J.A. 11617.

The Board nevertheless reversed the examiner's rejections of thirty-eight of the claims. J.A. 11638. The Board reviewed the entire specification, looking for support for each of the claim limitations at issue and found support for three of the limitations (such as one for "a data decompressed video image input circuit generating data decompressed video image information"). *See, e.g.*, J.A. 11599-601. The Board also reversed one rejection because it was based on language not appearing in the claims (the "weight" limitations). J.A. 11602-03. For the other eight groups of claim limitations at issue, however, the Board agreed with the examiner that these limitations (such as "generating two dimensional processed image information in response to the accessed blocks of pixel image information and in response to the two dimensional vector information") were not supported by adequate written description, and explained its reasoning in detail. *See, e.g.*, J.A. 11604-06. The Board also reversed the rejections on the grounds of obviousness, anticipation, and double patenting, which are not at issue in this appeal. J.A. 11638.

Hyatt filed a request for rehearing with the Board on September 30, 2002. J.A. 11642. In the brief supporting his request, he provided extensive new arguments and citations to the specification purportedly detailing where disputed limitations of each still-rejected claim derive written description support and are enabled. J.A. 11642-792. The Board denied his request for rehearing, holding that these new arguments and citations could and should have been presented during the original appeal briefing. J.A. 11805-07.

C. The § 145 Action

On April 16, 2003, Hyatt, now acting through counsel, filed a district court action under 35 U.S.C. § 145 against the Director. The Director filed a motion for summary judgment, arguing principally that the Board's decision to reject all of the relevant claims of the '702 application for lack of written description and enablement was supported by substantial evidence. Hyatt opposed the motion, proffering his own declaration as well as his briefing from his request for rehearing before the Board (collectively, "Hyatt declaration") as purported evidence supporting his opposition and precluding summary judgment in favor of the Director. The Director objected to the Hyatt declaration on the ground that Hyatt failed to timely submit it before the Board. *Hyatt v. Dudas*, 2005 WL 5569663, at **4, 6 n.11 (D.D.C. Sept. 30, 2005) ("*Hyatt II*"). Hyatt submitted no other evidence.

The district court excluded the Hyatt declaration because it found Hyatt had been "negligent" in failing to submit it to the PTO during examination or in a timely manner to the Board on appeal. *Id.* at *4-7. The district court then proceeded to analyze the record before the Board and concluded that the Board's decision to uphold the written description rejections was supported by substantial evidence. *Id.* at *7-10. As the court found that no genuine issues of material fact had been raised, it granted summary judgment to the Director that Hyatt's claims were invalid for failure to meet the written description requirement (and considered the enablement issue moot). *Id.* at *10. The district court denied Hyatt's subsequent motion for reconsideration. *Hyatt v. Dudas*, 2006 WL 4606037 (D.D.C. Sept. 30, 2006).

Hyatt then timely appealed the district court's judgment to this court. We stayed this appeal pending the decision in a related appeal, *Hyatt v. Dudas*, 492 F.3d 1365 (Fed. Cir. 2007) ("*Hyatt I*"). We have jurisdiction under 28 U.S.C. § 1295(a)(4)(C).

II.

The central issue in this appeal is whether the district court properly excluded the Hyatt declaration. The parties argue whether, in light of over a century of precedent and practice involving trial court actions to overturn Patent Office decisions, the district court properly excluded Hyatt's declaration. The parties are correct that this court has never squarely addressed the issue of exactly what standard governs district courts in ruling on the admissibility of evidence withheld during examination in the PTO. Hyatt argues that a plaintiff in a § 145 action is " 'entitled' to submit additional evidence" subject to no limitations other than those imposed by the Federal Rules of Evidence. [Blue br. at 11-12]. The Director counters that Congress could not have intended district courts in § 145 actions to disregard the proceedings before the PTO altogether. The Director urges that § 145 actions are at least partly a form of appeal of PTO decisions, and that evidence not submitted to the PTO through the negligence, or at least the gross negligence, of the applicant is properly excluded in a § 145 action.

Section 145 is silent regarding what evidence—or whether any new evidence—can be admitted in such an action. Nor does the statute expressly indicate what, if any, deference the district court must give to the findings of the Board, or our court to the rulings of the district court. As background, we will trace the origins of

§ 145[3] and summarize the historical practice of excluding certain evidence an applicant did not present to the Patent Office. We will also discuss one issue the parties did not, the Administrative Procedure Act ("APA").

A.

1.

Shortly after the founding of the United States, Congress, pursuant to its constitutional power to "promote the Progress of Science and useful Arts," U.S. Const. art. I, § 8, cl. 8, passed its first patent act. Act of Apr. 10, 1790, ch. 7, 1 Stat. 109-12. Under this statute, a majority of "the Secretary of State, the Secretary for the department of war, and the Attorney General" had the power to allow a patent application. *Id.* § 1. Congress did not provide for judicial review of the decision to reject a patent application. Three years later, Congress abolished the examination of patents, and for the next three decades, the United States operated under a regime of patent registration. *See* Act of Feb. 21, 1793, ch. 1, § 1, 1 Stat. 318; P.J. Federico, *Evolution of Patent Office Appeals* (pts. 1 & 2), 22 J. Pat. Off. Soc'y 838 (1940), 22 J. Pat. Off. Soc'y 920 (1940), at 838.

In 1836, Congress created the Patent Office and the post of Commissioner of Patents. Act of July 4, 1836, ch. 357, § 1, 5 Stat. 117. The Commissioner and his staff of seven were responsible for determining if patent applications disclosed sufficiently useful, important, and novel alleged inventions to warrant a patent. See *id.* §§ 2, 7. An applicant dissatisfied with the Commis-

---

[3] Which, according to the Supreme Court, "cannot be stated briefly." *Hoover Co. v. Coe*, 325 U.S. 79, 84, 65 S. Ct. 955, 89 L. Ed. 1488 (1945) (discussing origins of R.S. § 4915).

sioner's decision could appeal to a "board of examiners" appointed by the Secretary of State; at least one board member was "to be selected, if practicable and convenient, for his knowledge and skill in the particular art, manufacture, or branch of science to which the alleged invention appertains." *Id.* § 7. Congress also created a process whereby an applicant could challenge the decision of the board of examiners in court, although this was limited to situations involving overlap between patents or between a patent and a patent application:

> *[W]henever there shall be two interfering patents, or whenever a patent on application shall have been refused on an adverse decision of a board of examiners, on the ground that the patent applied for would interfere with an unexpired patent previously granted*, any person interested in any such patent, either by assignment or otherwise, in the one case, and any such applicant in the other case, *may have remedy by bill in equity*; and the court having cognizance thereof, on notice to adverse parties and other due proceedings had, may adjudge and declare either the patents void in the whole or in part, or inoperative and invalid in any particular part or portion of the United States, according to the interest which the parties to such suit may possess in the patent or the inventions patented, and may also adjudge that such applicant is entitled, according to the principles and provisions of this act, to have and receive a patent for his invention, as specified in his claim, or for any part thereof, as the fact of priority of right or invention shall in any such case be made to appear. And such adjudication, if it be in favor of the right of such applicant, shall authorize the Commissioner to issue such patent, on his filing a copy of the adjudication,

> and otherwise complying with the requisitions of this act. Provided, however, That no such judgment or adjudication shall affect the rights of any person except the parties to the action and those deriving title from or under them subsequent to the rendition of such judgment.

Id. § 17 (emphasis added and removed). Congress additionally provided for federal jurisdiction over such actions with no restrictions on venue: "[A]ll actions, suits, controversies, and cases arising under any law of the United States, granting or confirming to inventors the exclusive right to their inventions or discoveries, shall be originally cognizable, as well in equity as at law, by the circuit courts of the United States, or any district court having the powers and jurisdiction of a circuit court." *Id.* § 18.

Over the next several decades, minor changes were made to the process of contesting an adverse decision of the Commissioner. In 1839, Congress specified that instead of to a board of examiners, appeals from a decision of the Commissioner would be taken "to the chief justice of the district court of the United States for the District of Columbia." Act of Mar. 3, 1839, ch. 88, § 11, 5 Stat 355. Several years later, Congress instead directed appeals to any one of the judges of "the Circuit Court of the District of Columbia."[4] Act of Aug. 30, 1852, ch. 107, § 1, 10 Stat. 75. During the Civil War, Congress abolished the District of Columbia district and circuit courts and assigned all their functions to the newly-created "supreme court for the District of Columbia." Act of

---

[4] The District of Columbia district and circuit courts were both staffed by the same three judges. Federico at 850-52.

Mar. 3, 1863, ch. 91, §§ 1, 3, 12 Stat 762-63. None of these changes affected the procedure of the 1836 act for a bill in equity, which remained available after some court of the District of Columbia had reviewed the Commissioner's decision. *See Potter v. Dixon*, 19 F. Cas. 1145, 1146 (C.C.S.D.N.Y. 1863) (No. 11, 325).

Congress substantially revised the patent laws in 1870. See Act of July 8, 1870, ch. 230, 16 Stat. 198-217. Primary responsibility for examining an application was vested in a "primary examiner;" Congress also authorized a single "examiner in charge of interferences." *Id.* §§ 4, 46. The decision of either could be appealed "to the board of examiners-in-chief," and from there to the Commissioner.[5] *Id.* §§ 46-47. Further appeal could be taken "to the supreme court of the District of Columbia, sitting in banc;" the appeal was to be decided "on the evidence produced before the commissioner." *Id.* §§ 48-50. The decision of the District of Columbia supreme court could be challenged via a bill in equity:

> *[W]henever a patent on application is refused, for any reason whatever, either by the commissioner or by the supreme court of the District of Columbia upon appeal from the commissioner, the applicant may have remedy by bill in equity;* and the court having cognizance thereof, on notice to adverse parties and other due proceedings had, may adjudge that such applicant is entitled, according to law, to receive a patent for his invention, as specified in his claim, or for any part thereof, as the facts in the case may appear. And such adjudication, if it be in favor of the right of the applicant, shall authorize the com-

---

[5] These statutory changes merely formalized the practice that had developed over time within the Patent Office. Federico at 853-56.

> missioner to issue such patent, on the applicant filing in the patent office a copy of the adjudication, and otherwise complying with the requisitions of law. And *in all cases where there is no opposing party a copy of the bill shall be served on the commissioner, and all the expenses of the proceeding shall be paid by the applicant, whether the final decision is in his favor or not.*

Id. § 52 (later codified as R.S. § 4915) (emphasis added).[6] Unlike the procedure under the 1836 act, the 1870 act allowed a bill in equity for any refusal to allow a patent application, not just a refusal based on an interfering patent.[7]

In 1893, Congress created "the court of appeals of the District of Columbia," which had general appellate supervision of the supreme court of the District of Columbia. Act of Feb. 9, 1893, ch. 74, §§ 1, 7, 27 Stat. 434-35. To this new court were also assigned appeals from decisions of the Commissioner. *Id.* § 9. While appeals from "final judgments" of the court of appeals of the District of Columbia could be taken to the Supreme Court, *id.* § 8, the Supreme Court held that it lacked jurisdiction to review a decision of the Court of Appeals of the District of Columbia affirming the Commis-

---

[6] Although the statute provided a bill in equity could be filed after an adverse decision "either by the commissioner or by the supreme court of the District of Columbia upon appeal from the commissioner," the statute was nonetheless interpreted as allowing a bill in equity to be filed only after an adverse decision of the supreme court of the District of Columbia. *See Kirk v. Comm'r of Pats.*, 5 Mackey 229, 1886 WL 15875, *2 (D.C.Sup. 1886).

[7] The rules of equity practice applied to suits under Revised Statutes § 4915. *See Appleton v. Ecaubert*, 45 F. 281, 282 (C.C.E.D.N.Y. 1891).

sioner's rejection of an application because "the decision of that court may be challenged generally and a refusal of patent may be reviewed and contested by bill as provided" for by Revised Statutes § 4915. *Frasch v. Moore*, 211 U.S. 1, 9, 29 S. Ct. 6, 53 L. Ed. 65 (1908).

Although this created an appellate path from the Patent Office that may seem highly unusual to us today, such a path was used. *See Uihlein v. Gen. Elec. Co.*, 47 F.2d 997, 998 (7th Cir. 1931) (appeal from examiner of interferences, to board of examiners-in-chief, to Commissioner, to D.C. Cir., to E.D. Wis., to 7th Cir.); *Courson v. O'Connor*, 227 F. 890, 890, 892 (7th Cir. 1915) (appeal from examiner of interferences, to board of examiners-in-chief, to Commissioner, to D.C. Cir., to N.D. Ill., to 7th Cir.). It also seemed unusual to many at the time; in Congressional hearings and reports leading up to the 1927 amendments to the Patent Act, the fact that in no other area of law were "five appeals" possible was often mentioned. *See, e.g., Procedure in the Patent Office: Hearing on H.R. 7563 and H.R. 13487 before the H. Comm. on Pats.* ("H.R. 7563 Hearing"), 69th Cong. 8 (Dec. 10, 1926) (statement of A.C. Paul, Chairman of Legislation Comm., Pat. Section, of the Am. Bar Ass'n); *Procedure in the Patent Office: Hearing on S. 4812 before the S. Comm. on Pats.* ("*S. 4812 Hearing*"), 69th Cong. 8 (Dec. 20, 1926) (statement of Thomas E. Robertson, Comm'r of Pats.); H.R.Rep. No. 69-1889, at 1, 2, 7 (Jan. 28, 1927).[8]

---

[8] While Revised Statutes § 4915 did not on its face limit the venues in which a dissatisfied applicant could file a bill in equity, the practice of the Commissioner sometimes did. *See S. 4812 Hearing* at 8 (Robertson) ("If it is an ex parte case, the statute requires that service must be made on the Commissioner of Patents, and the Commissioner of Patents will not accept service in these suits all over the Untied States.

In 1927, Congress significantly altered the process of reviewing rejections. A substantial motivation for doing so was the unusual and lengthy process involving "five appeals" for patent applicants. *See id.* To streamline the appeal process, various groups suggested eliminating the bill in equity or the direct appeal from the Patent Office; Congress settled on retaining both procedures but forcing applicants to elect one or the other. *Hoover Co. v. Coe*, 325 U.S. 79, 83, 65 S. Ct. 955, 89 L. Ed. 1488 (1945); *S. 4812 Hearing* at 10 (Paul). Defenders of the bill in equity primarily argued for it by pointing out that it was the only method for supporting a patent application with live testimony. *See, e.g., H.R. 7563 Hearing* at 11, 15 (Robertson); *S. 4812 Hearing* at 15 (statement of Edward S. Rogers). Congress additionally simplified the appeal process by combining the two appeals within the Patent Office (to the board of examiners-in-chief and then to the Commissioner) into one (to a three-member "board of appeals" constituted from "the Commissioner of Patents, the first assistant commissioner, the assistant commissioner, and the examiners in chief"). Act of Mar. 2, 1927, ch. 273, §§ 3-9, 44 Stat. 1335-36.

Because of a backlog in the Court of Appeals of the District of Columbia, in 1929, Congress renamed the "Court of Customs Appeals" the "Court of Customs and Patent Appeals," and redirected appeals from the Patent Office to the renamed court. Act of Mar. 2, 1929, ch. 488, 23 Stat. 1475-76; *S. 4812 Hearing* at 25-27 (state-

---

The Department of Justice has not thought it proper to do that, so the commissioner will accept service only in the District of Columbia, or in Baltimore, nearby . . . . When I came in as commissioner five years ago we had one in Texas, and, of course, it makes it very difficult for the department to handle.").

ment of Karl Fenning, Chairman, Comm. on Laws & Rules of the Am. Pat. Law Ass'n).[9]

Congress significantly reworked the Patent Act in 1952. Revised Statutes § 4915 was bifurcated into separate provisions: 35 U.S.C. § 145 for ex parte proceedings, and 35 U.S.C. § 146 for interference proceedings. Congress made clear that this was not meant to change the substantive application of Revised Statutes § 4915. *See* S. Rep. No. 82-1979 (1952), as *reprinted in* 1952 U.S.C.C.A.N. 2394, 2400. ("This group of sections makes no fundamental change in the various appeals and other review of Patent Office action, but has made a few changes in the procedure in various instances to correct some of the problems which have arisen, particularly in section 146. These details are mainly procedural."). Subsequent changes to § 145 have been mainly cosmetic; § 145 currently reads (much as it did in 1952):

> An applicant dissatisfied with the decision of the Board of Patent Appeals and Interferences in an appeal under [35 U.S.C. § 134(a)] may, unless appeal has been taken to the United States Court of Appeals for the Federal Circuit [under 35 U.S.C. § 141], have remedy by civil action against the Director in the United States District Court for the District of Columbia if commenced within such time after such decision, not less than sixty days, as the Director appoints. The court may adjudge that such applicant is entitled to receive a patent for his invention, as specified in any of his claims involved in the decision of

---

[9] Prior to this change, Chief Justice William Howard Taft had been regularly reassigning judges from the Court of Customs Appeals to the Court of Appeals of the District of Columbia to help relieve the latter court's congestion. *S. 4812 Hearing* at 25-27.

the Board of Patent Appeals and Interferences, as the facts in the case may appear and such adjudication shall authorize the Director to issue such patent on compliance with the requirements of law. All the expenses of the proceedings shall be paid by the applicant.

2.

Under Revised Statutes § 4915 as it existed from 1927 to 1952, differences existed between the procedure for bills in equity based on ex parte proceedings and those based on interferences; as enacted in 1927, the last three sentences read:

> *In all cases where there is no opposing party a copy of the bill shall be served on the commissioner; and all the expenses of the proceedings shall be paid by the applicant, whether the final decision is in his favor or not. In all suits brought hereunder where there are adverse parties the record in the Patent Office shall be admitted in whole or in part, on motion of either party, subject to such terms and conditions as to costs, expenses, and further cross-examination of the witnesses as the court may impose, without prejudice, however, to the right of the parties to take further testimony. The testimony and exhibits, or parts thereof, of the record in the Patent Office when admitted shall have the same force and effect as if originally taken and produced in the suit.*

(emphasis added). The first of these sentences is the basis for the last sentence of the current version of § 145: "All the expenses of the proceedings shall be paid by the applicant." The last two sentences of Revised

Statutes § 4915 appear in revised form in the current version of § 146:

> In such suits the record in the Patent and Trademark Office shall be admitted on motion of either party upon the terms and conditions as to costs, expenses, and the *further cross-examination of the witnesses as the court imposes, without prejudice to the right of the parties to take further testimony. The testimony and exhibits of the record in the Patent and Trademark Office when admitted shall have the same effect as if originally taken and produced in the suit.*

(emphasis added). Congress added these last two sentences to Revised Statutes § 4915 in 1927 to eliminate an inefficient practice that had previously been required in interferences. As the Third Circuit explained, under Revised States § 4915 prior to the 1927 amendment,

> the evidence given in the interference proceedings could be introduced only as secondary evidence, after proper foundation laid. The competency of such evidence had to be determined according to the principles of equity jurisprudence. In other words, the witnesses who had testified in the interference proceedings had to testify anew in the suit in the district court. If they did not so testify their absence had to be accounted for in the usual way if the testimony taken in the interference was to be received as secondary evidence. The [1927] amendment was passed to avoid this arduous and expensive means of reproducing the evidence of the interference proceedings in the suit.

Gen. Talking Pictures Corp. v. Am. Tri-Ergon Corp., 96 F.2d 800, 812 (3d Cir.1938).

To the extent that pre-1927 interferences cases could be read to support a de novo review standard, these cases are based on the prior practice of affording the Patent Office record little weight. For example, in *Ex parte Squire* (which was cited in *Hoe*, 112 U.S. at 61, 5 S. Ct. 25) the court explained that "[t]he evidence before the commissioner is not evidence here, except by consent of parties. It is taken, generally, without much regard to formality, and is ex parte, and, even if permitted to be used here, not entitled to the credit of proof taken in the usual way." 22 F. Cas. at 1016-17. In amending Revised Statutes § 4915 in 1927, Congress clearly rejected this approach.

Because both § 145 and § 146 are derived from Revised Statutes § 4915, and we have previously described them as "parallel provisions," *Winner Int'l Royalty Corp. v. Wang*, 202 F.3d 1340, 1345 (Fed. Cir. 2000), our precedent from § 146 cases can be used for guidance in interpreting § 145. We have noted that while § 146 prescribes a method for introducing the PTO record in a § 146 action, "section 145 is completely silent about evidence." *Winner*, 202 F.3d at 1345.

However, as explained in *General Talking Pictures*, Congress provided in § 146 this method of admitting the Patent Office record and required that it "shall have the same effect as if originally taken and produced in the suit" to overcome a specific problem that existed only in bills in equity based on interferences, not those based on ex parte prosecution. The absence of similar language in § 145 does not suggest that the PTO record should be given less weight in a § 145 action. But *see Fregeau v.*

Mossinghoff, 776 F.2d 1034, 1041-42 (Fed. Cir. 1985) (Newman, J., concurring in part) (asserting § 145's silence about evidence means that § 145 proceedings should be conducted without regard to PTO record). Indeed, as we discuss below, it was well established by the Supreme Court that review of agency decisions was generally on the agency record. It should also be kept in mind that there are differences between ex parte prosecution and interference practice before the PTO, such as that live testimony may in certain circumstances be taken in interferences but not ex parte prosecution, see Trial Division of the Board of Patent Appeals and Interferences Standing Order at 1, http://www.uspto.gov/go/dcom/bpai/Standing-Order.pdf; *Ginter v. Benson*, 81 U.S.P.Q. 2d 1342, 1349 (B.P.A.I. 2005).

3.

While the Federal Circuit has not delineated a standard under which evidence may be excluded in § 145 actions,[10] various other courts have. Issues specific to § 145 actions are a matter of Federal Circuit, rather than regional circuit, law. *Titanium Metals Corp. of Am. v. Banner*, 778 F.2d 775, 779 (Fed. Cir. 1985). So far, we have left open the extent to which we should adopt the § 145 precedents from other circuits. *Id.* We

---

[10] The dissent presents several of cases in which this court has considered new evidence in § 145 and § 146 cases without analyzing whether that evidence should have been presented to the PTO. Dissent at 1284-85. In none of the cases the dissent cites, however, did any party object to the evidence. This court does not engage in sua sponte review of evidentiary rulings; objections not raised before the district court are ordinarily considered waived. *Caterpillar Inc. v. Sturman Indus.*, 387 F.3d 1358, 1368 (Fed. Cir. 2004).

thus undertake a review of past decisions of other courts.

Under the pre-1927 version of the statute, the Supreme Court made clear that a bill in equity under Revised Statutes § 4915 was not independent of proceedings in the Patent Office. Instead, the Court described this bill in equity as

> something more than a mere appeal. It is an application to the court to set aside the action of one of the executive departments of the government. The one charged with the administration of the patent system had finished its investigations and made its determination with respect to the question of priority of invention. That determination gave to the defendant the exclusive rights of a patentee. A new proceedings is instituted in the courts,—a proceeding to set aside the conclusions reached by the administrative department, and to give to the plaintiff the rights there awarded to the defendant. *It is something in the nature of a suit to set aside a judgment, and, as such, is not to be sustained by a mere preponderance of evidence.*

Morgan v. Daniels, 153 U.S. 120, 124, 14 S. Ct. 772, 38 L. Ed. 657 (1894) (emphasis added). Although dealing with the burden of proof and not admissibility of evidence, Morgan makes clear that the proceedings before the Patent Office could not be disregarded in court proceedings. The Supreme Court had also explained that under Revised Statutes § 4915, an applicant could file a

> bill in equity. This mean[t] a proceeding in a court of the United States having original equity jurisdiction under the patent laws, according to the ordinary

> course of equity practice and procedure. It [wa]s not a technical appeal from the patent-office, like that authorized in section 4911, confined to the case as made in the record of that office, but [wa]s prepared and heard upon all competent evidence adduced, and upon the whole merits.

Butterworth v. United States ex rel Hoe, 112 U.S. 50, 61, 5 S. Ct. 25, 28 L. Ed. 656 (1884);[11] *see also Hoover Co. v. Coe*, 325 U.S. 79, 83, 65 S. Ct. 955, 89 L. Ed. 1488 (1945) (Under R.S. § 4915, "a formal trial is afforded on proof which may include evidence not presented in the Patent Office."); *In re Hien*, 166 U.S. 432, 439, 17 S. Ct. 624, 41 L. Ed. 1066 (1897) ("The bill in equity provided for by section 4915 is wholly different from the proceeding by appeal from the decision of the commissioner . . . . The one is in the exercise of original, the other of appellate, jurisdiction."). More recently, the Court has also, "in passing, noted the settled law that in a section 145 action a disappointed applicant may present evidence that it did not present to the Board, and that the 'presence of such *new* or *different* evidence makes a factfinder of the district judge.'" Winner, 202 F.3d at 1345-46 (quoting *Dickinson v. Zurko*, 527 U.S. 150, 164, 119 S. Ct. 1816, 144 L. Ed.2d 143 (1999)) (emphasis added in *Winner*).

The dissent states that our holding is "in conflict with Supreme Court jurisprudence on this point." Dissent at 1282. In fact, the Supreme Court has never decided the issue of what kind of evidence or when evidence could be introduced in § 145 or Revised Statutes § 4915 actions, and there is no clear guidance to be gleaned from Su-

---

[11] The dissent misrepresents the import of an isolated phrase from this quotation. *See Dissent* at 1283.

preme Court jurisprudence. The dissent fails to recognize that Hoe involved not a bill in equity under Revised Statutes § 4915 but rather a writ of mandamus; the issue was "whether the secretary of the interior had power by law to revise and reverse the action of the commissioner of patents" in an interference. 112 U.S. at 54, 5 S. Ct. 25. As quoted above, the Court in *Hoe* noted that a suit under Revised Statutes § 4915 was "prepared and heard upon all competent evidence adduced," but remained silent as to what was "competent evidence" under Revised Statutes § 4915.[12] The dissent erroneously presents these phrases from *Hoe* as a holding. Dissent at 9. The dissent's reading of *Hoe*, however, is contrary to the Supreme Court's:

> Although, as was said by this court in [*Hoe*], the proceeding by bill in equity, under section 4915, on the refusal to grant an application for a patent, intends a suit according to the ordinary course of equity practice and procedure, and is not a technical appeal from the patent-office, nor confined to the case as made in the record of that office, but is prepared and heard upon all competent evidence adduced, and upon the whole merits, *yet the proceeding is, in fact and necessarily, a part of the application for the patent.*

Gandy v. Marble, 122 U.S. 432, 439, 7 S. Ct. 1290, 30 L. Ed. 1223 (1887) (emphasis added; citations omitted); *see also Hien*, 166 U.S. at 434, 17 S. Ct. at 626 (in explaining *Gandy*, noting that "the bill in equity was sub modo a branch of the application for the patent").

---

[12] Competent evidence is a synonym for admissible evidence. Bryan A. Garner, *A Dictionary of Modern Legal Usage* 186 (1995 2d ed.).

None of the other Supreme Court cases the dissent relies upon addressed this question either, or even involved suits under § 145 or Revised Statutes § 4915. The issue in *Zurko* (which involved an appeal under § 141 rather than an action under § 145) was whether the standard of review set forth in the APA "applies when the Federal Circuit reviews findings of fact made by the Patent and Trademark Office."[13] 527 U.S. at 152, 119 S. Ct. 1816. In *Hien*, which involved an appeal under Revised Statutes § 4911 rather than a bill in equity under Revised Statutes § 4915, the Court decided whether the two-year time limit for an applicant to respond to actions of the Patent Office required that an applicant be allowed two years to file a notice of appeal with the court of appeals for the District of Columbia. 166 U.S. at 436, 17 S. Ct. 624.

To be sure, the Supreme Court cases establish that in some circumstances new evidence may be submitted. But merely because new evidence may be submitted does not necessarily mean this right is unfettered;[14]

---

[13] It is ironic that the dissent downplays the importance of the holding of *Zurko* (and criticizes the fact that we even discuss the APA), *see* Dissent at 12 n. 4, and instead fixates on the statement that § 145 "permits the disappointed applicant to present to the court evidence that the applicant did not present to the PTO" (which was part of a rejection of the Federal Circuit's rationale for holding that the APA did not apply to appeals under § 141). *See Zurko*, 527 U.S. at 164, 119 S. Ct. 1816. Of course new evidence is "permit[ted]", but this does not mandate the admission of all evidence whatsoever. If this statement were as absolute as the dissent believes, it would seemingly trump the Federal Rules of Evidence.

[14] The dissent overlooks this distinction. *See* Dissent at 1281-85. Neither *Ex parte Squire*, 22 F. Cas. 1015, 1017 (C.C.E.D. Mo. 1877) (No. 13,269), nor *Butler v. Shaw*, 21 F. 321, 326 (C.C.D. Mass. 1884), support the dissent's argument that the right to admit new evidence is

there still may be situations in which new evidence may be excluded. Over the last century, lower federal courts have found circumstances in which the actions of a party before the Patent Office justify excluding evidence offered by that party from a suit to obtain a patent.

In an opinion from 1896, the Sixth Circuit, although not excluding evidence outright, stated "that its evidential weight is much impaired from the fact that, though accessible, it was not introduced during the interference proceedings." *Standard Cartridge Co. v. Peters Cartridge* Co., 77 F. 630, 638 (6th Cir. 1896).

In *Western Electric Co. v. Fowler*, a party to an interference, Fowler, argued for and submitted evidence supporting a June 1901 date of reduction to practice, and, after the examiner of interferences awarded priority to his opponent in the interference, Fowler attempted to submit new evidence supporting a March 1901 reduction to practice. 177 F. 224, 226 (7th Cir. 1910). This new evidence was admitted, but the examiner of interferences held Fowler to his original argument. *Id.* Fowler appealed successively to the examiner in chief, the Commissioner, and the Court of Appeals for the District of Columbia, but the decision of the examiner of interferences was affirmed each time. *Id.* Fowler filed a bill in equity to obtain a patent, and the Circuit Court for the Northern District of Illinois found for Fowler. *Id.* at 224. On appeal, the Seventh Circuit discounted the evidence Fowler produced tardily in the Patent Office, and on that basis, reversed the district court. *Id.* at 228-29; *see also Courson v. O'Connor*, 227

---

wholly unconstrained; each merely recites the unremarkable proposition that new evidence may have been submitted in a suit under Revised Statutes § 4915.

F. 890, 892-93 (7th Cir. 1915) (allowing new testimony in the circumstance of that case).

The court in *General Electric Co. v. Steinberger* took a limited view of what new evidence could be disregarded:

> In some instances the new testimony is offered as to matters which were not thought relevant or necessary for presentation to the Patent Office in the previous hearing.
>
> In general it must be held that all such testimony is competent and must be considered by the court in the action under section 4915, but in so far as the conclusions of the Patent Office, as sustained on appeal, are treated as a fair determination, upon similar testimony, and hence as being valid unless plainly erroneous, and in so far as the parties to the interference proceeding may have been estopped from asserting things inconsistent with their claims before the Patent Office, this court will not use the additional proofs in reaching a conclusion on the right to the patent, until it has determined whether the defeated party is in a position to contest further, or to give additional testimony about, the matters thus previously determined.

208 F. 699, 701 (E.D.N.Y. 1913).

After the 1927 amendments to the Patent Act, no circuit court allowed a de novo trial in an action under Revised Statutes § 4915. One of the more influential cases on the admissibility of evidence is *Barrett Co. v. Koppers Co.*, 22 F.2d 395 (3d Cir. 1927). There, during interference proceedings in the Patent Office, the Barrett Company instructed its employees not to answer questions

about certain of its "commercial practices." *Id.* at 396. The Barrett Company lost the interference, and then filed a bill in equity under Revised Statutes § 4915 and sought to introduce before the district court the exact testimony it had instructed its employees not to provide during the interference. *Id.* The Third Circuit found that the district court properly excluded this evidence, saying:

> The law gave the plaintiffs a day in court on the issue of priority. That was the day the interference was heard and if they chose not to avail themselves of their full rights but to gamble on the decision by giving only a part, and the weaker part, of the evidence they had in hand, they did it at their own risk. After losing on such evidence in what otherwise would be a train of futile appeals in the patent tribunals and Court of Appeals of the District of Columbia they cannot come into a District Court and say, now for the first time we shall tell the true story of reduction to practice and demand a patent.
>
> . . . . *When, as in this case, a party has refused to produce evidence for consideration by the Court of Appeals of the District of produces that very evidence to overcome the effect of that court's decision, he comes very close to trifling with the courts' processes.* If in this case the Court of Appeals of the District of Columbia was wrong it was because the plaintiffs purposely kept it in the dark. If now this court were in effect to reverse the decision of that court on evidence brought to light for the first time, we should be assisting the plaintiffs to profit by their own technical wrong doing.

> . . . . Particularly are we anxious that no one should think that we hold that any evidence not before the Court of Appeals of the District of Columbia is inadmissible in an action under section 4915, R.S. Such a notion would destroy the action given by section 4915, R.S. and throw overboard the whole doctrine of *Morgan v. Daniels*. Specifically our decision is that the plaintiffs in this action under section 4915, R.S., are *estopped to offer evidence which was wholly within their possession and control at the interference proceeding* and which they withheld from that proceeding and, therefore, withheld from the other patent tribunals and the Court of Appeals of the District of Columbia, and thereby made it impossible for those tribunals and that court to render what they, the plaintiffs, now maintain is the right decision.

Id. at 397 (formatting altered; emphasis added); *see also Standard Oil Co. v. Montedison, S.p.A.*, 540 F.2d 611, 616 (3d Cir. 1976) ("An action brought under § 146" is "limited to the review of a decision of the Board of Patent Interferences.").

While the Third Circuit gave *Barrett* a fairly limited reading in a subsequent case,[15] other courts have inter-

---

[15] *See Minn. Mining & Mfg. Co. v. Carborundum*, 155 F.2d 746, 748 (3d Cir. 1946) (distinguishing *Barrett* and affirming district court's denial of motion to exclude expert testimony which was allegedly "available to the plaintiffs at the time of the proceedings in the Patent Office" because the evidence was not *intentionally suppressed*). In a subsequent, related appeal of *Standard Oil*, the Third Circuit rejected the argument that the district court should have required a party to explain why it was only offering evidence for the first time before the district court. *Standard Oil Co. (Ind.) v. Montedison, S.P.A.*, 664 F.2d 356, 376 (3d Cir. 1981) ("[N]ew expert testimony is clearly admissible in a section 146 action without such justification to the extent that it aids the

preted *Barrett* more broadly. The Eighth Circuit cited *Barrett* when affirming a district court's exclusion of evidence that could have been presented to the Patent Office but was not. *Kirschke v. Lamar*, 426 F.2d 870, 872-75 (8th Cir. 1970). The District of Massachusetts followed *Barrett* in *O'Donnell v. United Shoe Machinery Corp.*, 2 F. Supp. 178, 181 (1933). There, the plaintiff presented witnesses to the Patent Office, but they did not testify about an experiment the plaintiff had allegedly performed. *Id.* After losing the interference, the plaintiff instituted a suit under Revised Statutes § 4915, and sought to have the same witnesses testify about the alleged experiment. *Id.* The defendant objected to this new evidence, and the court disallowed it, saying:

> All of the additional testimony was available when the question of priority was before the Patent Office. . . .
>
> I am not inclined to sanction the practice of submitting issues of fact to an administrative department, competent to decide the issue, upon a partial presentation of the available evidence, reserving the full presentation for a trial in the courts to set aside the order of the administrative authority. This practice was justly condemned in *Barrett Co. v. Koppers Co.* . . .

Id.

The Eastern District of New York promulgated a novel formulation of the rule of *Barrett*, namely that

---

court in understanding issues already presented to the Board."). It is not clear from the opinion, however, that the objecting party did anything other than attempt to place the burden of justifying the evidence on the party offering it.

evidence available to but not presented by the party who lost before the Patent Office would be given "no weight" because the losing party gave "no sufficient reason" why the evidence was not presented to the Patent Office. *Perkins v. Lawrence Sperry Aircraft Co.*, 57 F.2d 719, 720-21 (E.D.N.Y. 1932). Conversely, the court also ruled that the party successful before the patent office was "not bound by" this rule. *Id.* However, Judge Learned Hand, writing for the Second Circuit, hinted his disapproval of such a stringent exclusion standard the following year:

> In *Barrett Co. v. Koppers*, the Third Circuit refused to consider evidence which the inventor had deliberately suppressed in the interference, and used broader language than the exact situation required, which we quoted with approval in *Greene v. Beidler*, 58 F.2d 207, 209-10 (2d Cir. 1932). However, it does not follow that it would have extended the doctrine to evidence not suppressed, but merely neglected through the plaintiff's slackness in preparation. *Perkins v. Lawrence Sperry Aircraft Co.* did so extend it, but we need not approve. The question is doubtful and we prefer to leave it open, for it is not necessary to answer it here.

Dowling v. Jones, 67 F.2d 537, 538 (2d Cir. 1933) (citations altered and omitted; formatting altered; emphasis added).[16]

---

[16] The Second Circuit had earlier approved of *Barrett*. *See Greene v. Butler*, 58 F.2d 207, 209-10 (2d Cir. 1932) (quoting *Barrett* for the proposition that parties "cannot come into a District Court and say, now for the first time we shall tell the true story of reduction to practice and demand a patent" and stating "this is substantially the position which the appellees here have taken. It cannot prevail.").

The Seventh Circuit likewise accepted that evidence could be excluded from a case brought under Revised Statutes § 4915 because of the actions of a patent applicant:

> In the *Barrett* case, *the additional evidence was at all times "wholly within (the) possession and control" of plaintiff, but he had "withheld" the evidence from the Patent Office.* Under such circumstances, it is *reasonable that the withholding person be estopped to present that evidence later.* Such a principle of estoppel works properly in many instances, e.g., when evidence has been deliberately withheld or secreted, and when a story is completely changed on coming to court. *We do not dispute the soundness of the proposition that all pertinent evidence, actually available, should be submitted in the first instance.* To permit partial presentation before the Patent Office is to sanction the destruction of administrative justice.
>
> But we are satisfied that the estoppel principle has its limitations. It should not be used to penalize an innocent party. *Nor should it exclude the presentation of evidence, which previously had not been procurable or which had become known after the interference proceedings.* Coming now to the instant case, we find that Stoekle did *not intentionally withhold* the evidence which he later produced in court. . . . It seems undisputable that evidence may be available and existent at a given time, and yet not be within the knowledge or "possession and control" of the person desiring to make use of it. We are not prepared to say that Stoekle did not exercise *due diligence* in procuring the evidence sooner than he did.

Globe-Union v. Chicago Tel. Supply Co., 103 F.2d 722, 728 (7th Cir. 1939) (formatting altered; emphasis added).

By the time of *Velsicol Chemical Corp. v. Monsanto Co.*, at least in the Seventh Circuit, the rule based on *Barrett* had developed into the following:

> [A]bsent special circumstances,[17] the proper question for the district court was whether the failure of the proponent of the additional evidence to uncover its existence earlier or to procure it for the interference proceeding occurred *in spite of the proponent's diligence in preparing his case before the Board.* We agree with the court in *Kirschke* that it makes no difference whether the failure to produce the evidence was "attended by reprehensible motives or not (or) whether it be for tactical or other reasons." 426 F.2d at 874. Moreover, we find that in terms of the policy of encouraging full disclosure it is not necessary that there have been an affirmative action or *decision to suppress the evidence; it is enough that a reasonably diligent preparation of the proponent's case before the Board would have led to the discovery of the existence of the evidence and its production.* Nor is it necessary that the evidence have been in the exclusive control and possession of the proponent, as long as it was procurable by him. Conversely, *a litigant who has been reasonably diligent in identifying and procuring evidence for the interfer-*

---

[17] Examples of special circumstances might include an intervening change in the law, the presence of a new issue, or the admission of other new evidence deserving of a response or further elaboration. *See e.g., Douglas Aircraft Co. v. Mueller*, 107 U.S. App. D.C. 321, 277 F.2d 351 (1960).

> *ence proceeding will not be precluded* from strengthening his presentation in the district court if new evidence should become available to him in the interim.

Velsicol, 579 F.2d 1038, 1046 & n. 10 (7th Cir. 1978) (footnote renumbered; emphasis added).

The D.C. Circuit has stated that "the plaintiff may not submit for the first time evidence which he was negligent in failing to submit to the Patent Office." *Cal. Research Corp. v. Ladd*, 356 F.2d 813, 820 n. 18 (D.C. Cir. 1966). The D.C. Circuit has also prohibited an applicant from raising new issues in a § 145 action, and justified that rule as a necessary extension of the requirement that one exhaust administrative remedies before resorting to court, *DeSeversky v. Brenner*, 424 F.2d 857, 859-60 (D.C. Cir. 1970) (per curiam), or, as the D.C. Circuit has also explained it, a § 145 action "may not be conducted in disregard of the general policy of encouraging full disclosure to administrative tribunals," *Cal. Research*, 356 F.2d at 820 n. 18; see also *Knutson v. Gallsworthy*, 164 F.2d 497, 508-09 (D.C. Cir. 1947). The D.C. Circuit has noted that "surprise should not materially affect the result in" § 145 cases. *Cal. Research*, 356 F.2d at 821.[18]

---

[18] Although the D.C. Circuit did not expressly adopt *Barrett*, it cited the case to support a statement in dicta that evidence which was important and "readily available" yet not presented to the PTO should not be admitted in a suit under R.S. § 4915. *Boucher Inventions v. Sola Elec. Co.*, 131 F.2d 225, 227 & n. 5 (D.C. Cir. 1942). *See also* Emerson Stringham, Patent Interference Equity Suits 83-84 (1930) ("*Barrett v. Koppers* takes the rather extreme position that a party who withholds, during the office interference, evidence then in his possession and control, is thereafter estopped to present that evidence in an equity suit. . . . Probably such a ruling would be made only if the court considered that

Under § 145, the District of Columbia district court is the exclusive forum for actions under that statute. Since 2002, there appear to have been approximately thirty § 145 actions filed in the District of Columbia district court.[19] Many are terminated before the district court must rule on the admissibility of evidence not before the PTO. *See, e.g., Novo Nordisk A/S v. Dudas*, No. 06-cv-01896, slip op. at 2-3 (July 3, 2007) (dismissing case by consent of parties).

There is no uniform practice in the District of Columbia district court regarding the standard governing exclusion from § 145 actions of evidence that was not submitted during PTO proceedings. *See Hyatt II*, 2005 WL 5569663, at *4-7 (after Director's objection, excluding evidence because failure to submit it to PTO was "negli-

---

the withholding during the office proceeding *constituted bad faith, amounting to, or approximating, 'unclean hands.'*") (emphasis added).

[19] *SD3, LLC v. Doll*, 08-cv-01242-RWR; *Aldor Solutions Corp. v. Dudas*, 08-cv-00897-ESH; *Dome Patent L.P. v. Doll*, 07-cv-01695-PLF; *Hitachi Koki Co. v. Doll*, 07-cv-01504-ESH; *Novo Nordisk A/S v. Dudas*, 06-cv-01896-CKK; *Takeda Pharm. Co. v. Dudas*, 06-cv-01640-TFH; *Fullerene Int'l Corp. v. Dudas*, 06-cv-01451-RMU; *Innovatit Seafood Sys. v. Comm'r of Pats.*, 06-cv-00825-JR; *Innovatit Seafood Sys. v. Comm'r of Pats.*, 06-cv-00822-JR; *Hickman v. Dudas*, 05-cv-02426-RBW; *Hyatt v. Dudas*, 05-cv-02310-HHK; *Dieterich Stnd. Inc. v. Dudas*, 05-cv-02296-RBW; *Putman v. Dudas*, 05-cv-01796-LFO; *Hyatt v. Dudas*, 05-cv-00834-EGS; *Hyatt v. Dudas*, 05-cv-00310-HHK; *Hyatt v. Dudas*, 05-cv-00309-EGS; *Galbreath v. Dudas*, 04-cv-02222-JR; *Hyatt v. Dudas*, 04-cv-01802-HHK; *Hyatt v. Dudas*, 04-cv-01496-EGS; *Hyatt v. Dudas*, 04-cv-01222-EGS; *Hyatt v. Dudas*, 04-cv-01139-HHK; *Hyatt v. Dudas*, 04-cv-01138-HHK; *Hyatt v. Rogan*, 03-cv-01375-EGS; *Hyatt v. Rogan*, 03-cv-01283-EGS; *Hyatt v. Rogan*, 03-cv-01280-EGS; *Regents of Univ. of Cal. v. Rogan*, 03-cv-01133-RWR; *Hyatt v. Dudas*, 03-cv-00901-HHK; *Hyatt v. Dudas*, 03-cv-00108-EGS; *Protechna, SA. v. Godici*, 02-cv-02524-RBW; *Galbreath v. Dudas*, 02-cv-02354-JR.

gent"); *Hitachi Koki Co. v. Dudas*, 556 F. Supp. 2d 41, 47 (D.D.C. 2008) (flatly rejecting negligence standard of *Hyatt II* and admitting evidence over Director's objection because failure to present it was not due to "*fraud, bad faith, or gross negligence*" (emphasis added)); *Takeda Pharm. Co. v. Dudas*, 511 F. Supp. 2d 81, 87 (D.D.C. 2007) (admitting new evidence over Director's objection because failure to submit it to PTO was "not *negligent*" (emphasis added)); *Killian v. Watson*, 121 U.S.P.Q. 507, 509 (D.D.C. 1958) (after Commissioner's objection, excluding new evidence on alternate grounds that failure to submit it to Patent Office was "*grossly negligent*" and that applicant gave no explanation for the failure (emphasis added)); *see also Shell Dev. Co. v. Pure Oil Co.*, 111 F. Supp. 197, 199 (D.D.C. 1953) (in § 146 case, admitting evidence over objection because failure to submit it during interference was not *due to* "*any bad faith, suppression, or gross negligence*" (emphasis added)). However, as the preceding cases show, the District of Columbia district court will always exclude evidence that was not presented to the PTO due to bad faith or gross negligence and sometimes if the failure to present it was negligent.

In sum, it has been the general practice of federal courts for over eighty years in certain circumstances to exclude evidence which a party could and should have introduced before the Patent Office but did not despite an obligation to do so. Our own cases likewise have not adopted a de novo standard for trial. We have said that "[c]learly, the applicant does not start over to prosecute his application before the district court unfettered by what happened in the PTO." *Fregeau*, 776 F.2d at 1038. On the other hand, it is beyond question that in appropriate circumstances new evidence may be submitted to

the district court in a § 145 action (subject, at least, to the Federal Rules of Evidence). *See Gould v. Quigg*, 822 F.2d 1074, 1079 (Fed. Cir. 1987) ("[A]dditional evidence is permitted in a civil action under section 145, allowing the district court to make *de novo* fact findings."); *Newman v. Quigg*, 877 F.2d 1575, 1579 (Fed. Cir. 1989) ("A district court action under 35 U.S.C. § 145 is a de novo determination of patentability. It is not limited to the record before the PTO."); Emerson Stringham, Patent Interference Equity Suits 5 (1930) ("The equity suit offers distinctive advantages in way of a fresh hearing and the presentation of testimony direct to the tribunal.").

B.

As the Supreme Court has noted, "[o]ne purpose" of Congress in enacting the APA "was to introduce greater uniformity of procedure and standardization of administrative practice among the diverse agencies whose customs had departed widely from each other." *Wong Yang Sung v. McGrath*, 339 U.S. 33, 41, 70 S. Ct. 445, 94 L. Ed. 616 (1950), *superseded by statute*, Supplemental Appropriation Act of 1951, 64 Stat. 1048, as *recognized in Marcello v. Bonds* 349 U.S. 302, 311, 75 S. Ct. 757, 99 L. Ed. 1107 (1955). The Court explained that lightly finding exceptions to the APA would defeat its purpose. *Id.*

Court review (whether by a district court or a court of appeals) of an administrative agency decision is presumptively deferential under the APA. *See* 5 U.S.C. §§ 701-06. The usual rule is that judicial review of agency action should be on the agency record, regardless of whether the action is in the court of appeals or in district

court. *See Marsh v. Or. Natural Res. Council*, 490 U.S. 360, 375-78, 109 S.Ct. 1851, 104 L. Ed. 2d 377 (1989); *Chandler v. Roudebush*, 425 U.S. 840, 862, 96 S. Ct. 1949, 48 L. Ed. 2d 416 (1976) ("[I]n the absence of specific statutory authorization, a de novo review is generally not to be presumed."); *Camp v. Pitts*, 411 U.S. 138, 141-42, 93 S. Ct. 1241, 36 L. Ed. 2d 106 (1973) (per curiam) ("[T]he focal point for judicial review [by the district court] should be the administrative record already in existence, not some new record made initially in the reviewing court."); *see generally* Jacob Stein, et al., *Administrative Law* § 51.04 (2006).

While the APA specifically states that "the reviewing court shall decide all relevant questions of law," 5 U.S.C. § 706, court review of agency fact-finding is generally deferential. Under 5 U.S.C. § 706(2)(F), a reviewing court may "set aside agency action, findings, and conclusions" if "unwarranted by the facts[,] to the extent that the facts are subject to trial de novo by the reviewing court." As the Supreme Court stated in *Citizens to Preserve Overton Park, Inc. v. Volpe*, such de novo review is authorized in two situations: first, "when the action is adjudicatory in nature and the agency factfinding procedures are inadequate," or, second, "when issues that were not before the agency are raised in a proceeding to enforce nonadjudicatory agency action." 401 U.S. 402, 415, 91 S. Ct. 814, 28 L. Ed. 2d 136 (1971) (citing H.R. Rep. No. 1980 (May 3, 1946)). These exceptions do not apply to § 145 cases; the patent application process is not adjudicatory and new issues cannot be raised in a § 145 action. *See Newman*, 877 F.2d at 1579 (citing *DeSeversky*, 424 F.2d at 858). A third (and final) exception to the limited review under the APA exists: where another statute explicitly provides for de novo review. *See*

United States v. Carlo Bianchi & Co., 373 U.S. 709, 714-15, 83 S. Ct. 1409, 10 L. Ed. 2d 652 (1963).

Even before the 1946 enactment of the APA, see Act of June 11, 1946, 60 Stat. 243, the Supreme Court had held that provisions for district court review—even in a suit in equity—would not be read to imply the power to go outside the agency record. For example, in *Tagg Bros & Moorhead v. United States*, the Court discussed that although the Packers and Stockyards Act of 1921, 7 U.S.C. §§ 181-231, provided for suits to be brought in federal district court to enjoin the enforcement of agency orders, this did not imply trial de novo. 280 U.S. 420, 444-45 & n.4, 50 S. Ct. 220, 74 L. Ed. 524 (1930). Judicial review of orders of the Secretary was "restricted" by the following statutory language: "If, after hearing, that court determines that the order was regularly and duly served, and that the carrier is in disobedience of the same, the court shall enforce obedience." *Tagg Bros.*, 280 U.S. at 444 n.4, 50 S. Ct. 220 (quoting 49 U.S.C. § 16(12)). The Court explained:

> A proceeding under section 316 of the Packers and Stockyards Act is a judicial review, not a trial de novo. The validity of an order of the Secretary, like that of an order of the Interstate Commerce Commission, must be determined upon the record of the proceedings before him [except with regard to certain constitutional claims]. . . . On all other issues his findings must be accepted by the court as conclusive, if the evidence before him was legally sufficient to sustain them and there was no irregularity in the proceeding. *To allow his findings to be attacked or supported in court by new evidence would substitute the court for the administrative tribunal as the*

> *rate-making body.* Where it is believed that the Secretary erred in his findings because important evidence was not brought to his attention, the appropriate remedy is to apply for a rehearing before him or to institute new proceedings.

280 U.S. 420, 443-45, 50 S. Ct. 220, 74 L. Ed. 524 (1930) (emphasis added; footnote omitted).

The Court disposed of similar arguments in the context of district court actions authorized by the judicial review provision of the Communications Act of 1934, 47 U.S.C. § 402(a).[20] *Nat'l Broadcasting Co. v. United States*, 319 U.S. 190, 227, 63 S.Ct. 997, 87 L. Ed. 1344 (1943). The Court held that such suits were not de novo, and the review was limited to the agency record: "The court below correctly held that its inquiry was limited to review of the evidence before the Commission. *Trial de novo of the matters heard by the Commission and dealt with in its Report would have been improper.*" *Id.* at 227, 63 S. Ct. 997.

Similarly, in *Bianchi* the Court held that suits brought in the Court of Claims under the Wunderlich Act were not trials de novo, but were limited to the agency record. 373 U.S. at 713-15, 83 S.Ct. 1409. The Court noted that "the standards of review adopted in the Wunderlich Act—'arbitrary,' 'capricious,' and 'not supported by substantial evidence'—have frequently been used by Congress and have consistently been associated with a review limited to the administrative record." *Id.*

---

[20] The Court had previously characterized an action based on this statute as "a plenary suit in equity." *Columbia Broadcasting Sys. v. United States*, 316 U.S. 407, 415, 62 S. Ct. 1194, 86 L. Ed. 1563 (1942).

at 715, 83 S. Ct. 1409. The Court gave the following general rule:

> [T]he reviewing function is ordinarily limited to consideration of the decision of the agency or court below *and of the evidence on which it was based. Indeed, in cases where Congress has simply provided for review, without setting forth the standards to be used or the procedures to be followed, this Court has held that consideration is to be confined to the administrative record* and that no de novo proceeding may be held.

Id. at 714, 83 S.Ct. 1409.

Previously, this court rejected the notion that the APA applied to fact-finding by the PTO when reviewed on direct appeal here. *In re Zurko*, 142 F.3d 1447 (Fed. Cir. 1998) (en banc). The Supreme Court reversed, holding that the Federal Circuit must review fact-finding by the PTO using the framework set forth in the APA. *Dickinson v. Zurko*, 527 U.S. 150, 165, 119 S. Ct. 1816, 144 L. Ed. 2d 143 (1999). The Court noted that for a statute to create exceptions to the APA, it must do so clearly. *Id.* at 155, 119 S. Ct. 1816. And the circumstances under which the APA provides for de novo review of factual issues are "narrow." *Overton Park*, 401 U.S. at 414, 91 S. Ct. 814.

Where the statute, as here, provides for district court review, a de novo trial is generally not appropriate unless the statute specifically provides for it. Section 145 does not. Section 145 merely states that "[a]n applicant dissatisfied with the decision of the Board" may "have remedy by civil action against the Director in the United States District Court for the District of Columbia." This

is in contrast to other statutes that do provide explicitly for de novo review in the district courts. Such statutes are very clear; when Congress intends review by de novo trial, Congress explicitly authorizes de novo trial.[21]

---

[21] *See, e.g., Food Stamp Act*, 7 U.S.C. § 2023(a)(15) ("The suit in the United States district court or State court *shall be a trial de novo* by the court in which the court shall determine the validity of the questioned administrative action in issue . . . . "); *Ibrahim v. United States*, 834 F.2d 52, 53-54 (2d Cir. 1987) ("The Food Stamp Act's de novo review provision embodies a different and broader scope of review than that available under the APA . . . [*Camp v. Pitts*] is not on point. That case involved review of a decision by the Comptroller of the Currency denying a national bank charter, and no statute or regulation provided for de novo review. The APA therefore governed. Here, in contrast, the Food Stamp Act specifically provides that review of FNS determinations 'shall be a trial de novo.' 7 U.S.C. § 2023(a)."); 7 U.S.C. § 499g(c) (providing that, for review of reparations orders by Department of Agriculture, "Either party adversely affected by the entry of a reparation order by the Secretary may . . . appeal therefrom to the district court. . . . Such suit in the district court *shall be a trial de novo and shall proceed in all respects like other civil suits for damages*, except that the findings of fact and order or orders of the Secretary shall be prima-facie evidence of the facts therein stated"); *see also* 19 U.S.C. § 1592(e) (providing that, for review of customs penalties for negligence or fraud, "Notwithstanding any other provision of law, in any proceeding commenced by the United States in the Court of International Trade for the recovery of any monetary penalty claimed under this section . . . all issues, including the amount of the penalty, *shall be tried de novo*"); *United States v. Ford Motor Co.*, 463 F.3d 1286, 1297 (Fed. Cir. 2006) (finding that even the explicit language of § 1592(e) should interpreted narrowly as providing for de novo review only of certain aspects of the customs determination, not to "permit an importer to end-run the protest provisions").

Only in very rare cases has the Supreme Court held that a new record may be made in the District Court in the absence of specific statutory authorization. *McDonnell Douglas Corp. v. Green*, 411 U.S. 792, 798-99, 93 S. Ct. 1817, 36 L. Ed. 2d 668 (finding that private-sector employees are entitled to trial de novo under Title VII); *accord Chandler*,

In light of *Zurko*, we determined that actions under § 145 are subject to the strictures of the APA. *See Mazzari v. Rogan*, 323 F.3d 1000, 1004 (Fed. Cir. 2003) ("[A] reviewing court, whether this court or the district court, applies the 'substantial evidence' standard of review to findings of fact made by the [B]oard."). Of course, in § 145 actions, review is not strictly confined to the agency record. *Zurko*, 527 U.S. at 164, 119 S. Ct. 1816. But neither are proceedings wholly de novo; the admission of new evidence is limited by the APA.[22] *Mazzari*, 323 F.3d at 1005. The Supreme Court in Zurko left open the question of how to apply the APA to our review of PTO decisions in various circumstances, including § 145 actions. *See* 527 U.S. at 164, 119 S. Ct. 1816.

In light of the hybrid nature of § 145 actions, we have held that in the absence of new evidence, a district court must review the decision of the Board for substantial evidence, but for factual questions where new evidence

---

425 U.S. at 845, 96 S. Ct. 1949 (for public employees under Title VII). However, the statutory scheme makes clear that "Title VII does not provide the [EEOC] with direct powers of enforcement. The [EEOC] cannot adjudicate claims or impose administrative sanctions. Rather, final responsibility for enforcement of Title VII is vested with federal courts." *Alexander v. Gardner-Denver Co.*, 415 U.S. 36, 44-45, 94 S. Ct. 1011, 39 L. Ed. 2d 147 (1974).

[22] A central flaw of the dissent is that it believes evidence in § 145 actions is limited only by the Federal Rules of Evidence. *See* Dissent at 1280. Contrary to the dissent's argument, however, it is not enough that § 145 is silent about evidence or that an appeal is available under § 141. *See* dissent at 1280-81. The Supreme Court has recently stated that patent law should not lightly depart from accepted legal principles of general applicability. *See eBay Inc. v. MercExchange, L.L.C.*, 547 U.S. 388, 390-94, 126 S. Ct. 1837, 164 L. Ed. 2d 641 (2006). The ambiguous silence of § 145 on the admissibility of evidence does not meet the high bar the Supreme Court has set for implying trial de novo.

is before the district court, the district court makes de novo findings. *Fregeau*, 776 F.2d 1034.[23] However, admitting new evidence without restriction would defeat the purpose of the APA, as applicants could then always submit new evidence whenever they desired de novo review; allowing new evidence unnecessarily will convert deferential review "into effectively de novo review." *Axiom Resource Mgmt. v. United States*, 564 F.3d 1374, 1380 (Fed. Cir. 2009).

Nothing in the language of § 145 requires a de novo trial. The dissent makes much of the phrase "a civil action" in the statute, arguing that it requires a de novo action despite the general rule that review is on the agency record. It should be noted, however, that the language of the predecessor statute referred to a "bill in equity." Even before the APA, the Supreme Court repeatedly held that general language authorizing judicial review does not create a trial de novo, and that much more specific language is required. *See, e.g., Nat'l Broadcasting*, 319 U.S. at 227, 63 S. Ct. 997; *Tagg Bros.*, 280 U.S. at 444-45 & n. 4, 50 S. Ct. 220.

Nor do the cases addressing § 145 support the dissent's de novo standard. As discussed above, the Supreme Court has never directly considered the scope of § 145 with regard to new evidence, and the one reference to § 145 in a Supreme Court decision sheds little light on the issue. *Zurko* involved the question of what was the proper standard of review on direct appeal to the Federal Circuit under § 141, and although the Su-

---

[23] In *Zurko*, the Supreme Court noted that we may need to adjust standards of review to prevent anomalous results under the APA, citing *Fregeau* with apparent approval. *See Zurko*, 527 U.S. at 164, 119 S. Ct. 1816.

preme Court noted that a § 145 claimant can "present to the court evidence that the applicant did not present to the PTO," the Court said nothing about when or under what circumstances such evidence could be introduced. *See Zurko*, 527 U.S. at 164, 119 S. Ct. 1816.

As the Supreme Court stated in *Overton Park*, where "agency factfinding procedures are inadequate," the APA allows a district court to take additional evidence. For example, the PTO does not take oral testimony in an examination of a patent application. In some cases credibility determinations will be very important to the resolution of the case, for example, where there is a question about the date of reduction to practice which will determine what is, or is not, prior art. In such circumstances, it makes sense to permit the district court to hear live testimony under *Overton Park* to resolve credibility issues because the PTO procedures are inadequate.

Some restrictions on the ability of an applicant to introduce new evidence in a § 145 action are therefore required under the APA, although there is certainly not a blanket exclusion of new evidence, either.[24]

---

[24] The dissent complains that we "blur[ ] the line between an appeal pursuant to § 141 and the civil action of § 145." Dissent at 1289. However, the availability of live direct testimony and cross-examination would make a section 145 action quite different from a section 141 appeal, regardless of whether some evidence available to the applicant but not submitted to the PTO would be excludable. Just because proceedings under the two sections are *different* does not mean they should be as *different as possible*; the dissent lacks convincing support to require the specific difference it wishes to create. In any event, de novo proceedings under § 145 are disallowed by the APA.

C.

Hyatt and the dissent argue that proceedings under § 145 are (or should be) entirely de novo if the plaintiff so wishes. However, the arguments in favor of de novo proceedings are unpersuasive. Hyatt focuses on isolated statements by this and other courts that a § 145 action is a "de novo" proceeding, but ignores the context of—and qualifications on—such statements. Although the Seventh Circuit acknowledged that evidence could be excluded because it was not presented to the Patent Office, the court still referred to a case brought under Revised Statutes § 4915 as "a de novo trial." *Globe-Union*, 103 F.2d at 728. As the district court from which Hyatt's appeal is taken has aptly noted, § 145 actions

> are sometimes denominated "trials de novo", but such use of this term is somewhat loose. . . . Additional evidence is admissible in support of contentions advanced by the parties in the Patent Office. It is this feature that has led to the inaccurate use of the appellation "trials de novo" in these actions. There is a limitation on the admissibility of supplementary evidence. Such evidence as was available to the parties, but was withheld from the Patent Office as a result of fraud, bad faith, or gross negligence, may be excluded at the trial.

Monsanto Co. v. Kamp, 269 F. Supp. 818, 822 (D.D.C. 1967); *see also Killian v. Watson*, 121 U.S.P.Q. 507, 507 (D.D.C. 1958) ("It is equally well settled that the proceedings of the District Courts under § 145, though de novo, are not wholly ignorant of what has gone before."); *MacKay v. Quigg*, 641 F. Supp. 567, 570 (D.D.C. 1986) ("For that reason, despite the 'de novo' label accorded judicial review under § 145, courts have limited the ad-

missibility of certain kinds of evidence."); cf. *Conservolite, Inc. v. Widmayer*, 21 F.3d 1098, 1102 (Fed. Cir. 1994) ("While the expression 'de novo' is often used to describe a § 146 action, the statute does not use this language or state that new issues can freely be raised. Section 146 authorizes the district court on review to accept new testimony, but normally only as to issues raised by the parties during the proceedings below or by the Board's decision.").

The dissent argues that testimony given before Congress in 1926 compels the conclusion that a de novo trial is available under § 145 in all circumstances. Dissent at 3-7. During 1926 hearings on proposed patent statute reforms similar to those enacted in 1927, Commissioner Thomas E. Robertson, in an attempt to persuade Congress to eliminate altogether bills in equity to obtain patents, stated that plaintiffs in such suits could

> file testimony bringing in evidence that they could have brought in before but did not bring in before, and after dragging a man through all this procedure which you have said is so complicated and burdensome, start de novo in court, and bring in testimony not taken the first time.

To Amend Section 52 of Judicial Code and Other Statutes Affecting Procedure in Patent Office: Hearings on H.R. 6252 and H.R. 7087 Before the House Committee on Patents, 69th Cong., 1st Sess. 81 ("*H.R. 6252 Hearing*") (emphasis added). However, characterizations by Patent Office officials are not necessarily indicative of the intent of Congress, particularly where the witnesses

opposed the legislation.[25] As the Supreme Court has noted in *Bryan v. United States*, the "the fears and doubts of the opposition are no authoritative guide to the construction of legislation. In their zeal to defeat a bill, they understandably tend to overstate its reach." 524 U.S. 184, 196, 118 S. Ct. 1939, 141 L. Ed. 2d 197 (1998) (citations, brackets, and quotation marks omitted). Stray comments by other witnesses supporting the legislation are also distinctly unpersuasive. The dissent quotes Representative Albert H. Vestal as saying a bill under Revised Statutes § 4915 "is not an appeal. It is the bringing of a new suit." Dissent at 1281 (quoting *H.R. 6252 Hearing* at 36). Even statements by members in floor debate are entitled to little weight. *Garcia v. United States*, 469 U.S. 70, 76, 105 S. Ct. 479, 83 L. Ed. 2d 472 (1984) ("In surveying legislative history we have repeatedly stated that the authoritative source for finding the Legislature's intent lies in the Committee Reports on the bill. . . . We have eschewed reliance on the passing comments of one Member and casual statements from the floor debates." (citations omitted)).

While not irrelevant to the extent that Congress enacted § 145 based on existing practice under Revised Statutes § 4915, this legislative history can hardly be said to be dispositive, or even particularly probative, of the issue in the present case, as the majority clearly concluded in *Fregeau*, 776 F.2d at 1037-38. And even to the extent this legislative history is considered, much of it only supports the undisputed general rule that applicants may submit certain evidence not previously before the PTO in a § 145 action. *See, e.g., H.R. 6252 Hearing*

---

[25] Commissioner Thomas's comments appear to be focused on interference cases rather than ex parte ones. *H.R. 6252 Hearing* at 78-82.

at 81 (Paul) ("If we go into a court of equity the parties may use the record that they have in the Patent Office and may supplement it by additional evidence."). But none of the cited Congressional testimony specifically addresses situations where an applicant sought to overcome *the consequences of his own refusal to adhere to the rules of prosecuting a patent application.* Indeed, absent from the legislative history is any discussion of the admissibility of evidence being proffered or objections to evidence.

Furthermore, the "evaluation of congressional action . . . must take into account its contemporary legal context." *Cannon v. Univ. of Chicago*, 441 U.S. 677, 698-99, 99 S. Ct. 1946, 60 L. Ed. 2d 560 (1979). "Congress is presumed to be aware of an administrative or judicial interpretation of a statute and to adopt that interpretation when it re-enacts a statute without change." *Lorillard v. Pons*, 434 U.S. 575, 580, 98 S. Ct. 866, 55 L. Ed. 2d 40 (1978).[26] Although issued several months after Congress' 1927 revisions to patent laws, *Barrett* predated the 1952 Patent Act by a quarter of a century, which, combined with Congress' statement that § 145 and § 146 made "no fundamental change in the various *appeals* and *other review* of Patent Office action,"[27] S. Rep. No. 82-1979 (1952) (emphasis added), suggests

---

[26] *But see Catron County Bd. of Comm'rs v. U.S. Fish & Wildlife Serv.*, 75 F.3d 1429, 1438 (10th Cir. 1996) ("Although a proponent of congressional acquiescence need not show that the acquiescence is 'specifically embodied in a statutory mandate,' he bears the burden of showing 'abundant evidence that Congress both contemplated and authorized' the previous noncongressional interpretation in which it now acquiesces.").

[27] This is not equivalent to making "no substantive changes to § 4915," as the dissent asserts. *See* Dissent at 1281.

that Congress approved of the cases holding that patent applicants could not present to a district court evidence they should have but did not present to the Patent Office. And this legislative history predated the 1946 enactment of the APA by two decades.[28]

Hyatt's argument for a de novo action is also inconsistent with our precedent that the district court must apply a deferential standard to PTO fact-finding. *See Mazzari*, 323 F.3d at 1004-05. "Clearly, the applicant does not start over to prosecute his application before the district court unfettered by what happened in the PTO." *Fregeau*, 776 F.2d at 1038. Indeed, the Supreme Court assumed there would be cases brought under § 145 in which "the district judge does no more than review PTO factfinding." *Zurko*, 527 U.S. at 164, 119 S. Ct. 1816. Therefore, in the absence of new evidence, the district court is obliged to accept the facts as found by the PTO unless not supported by substantial evidence. *Mazzari*, 323 F.3d at 1005; *see also Zurko*, 527 U.S. at 162-65, 119 S. Ct. 1816. When new evidence is admitted, the district court makes de novo factual findings, but only as to the new evidence. *See Mazzari*, 323 F.3d at 1004. In other words, the district court must defer to the PTO's fact-finding except where appropriately admitted new evidence conflicts with a fact found by the PTO or presents a new factual issue that the PTO did not consider. *See id.*

---

[28] The dissent's heavy reliance on the legislative history of the 1927 revisions to the Patent Act, *see* Dissent at 1280-82, is therefore anachronistic.

III.

A.

If the district court's ruling had been a conventional evidentiary ruling, we would apply the standard of review of the appropriate regional circuit. *See Advanced Cardiovascular Sys. v. Medtronic, Inc.*, 265 F.3d 1294, 1308 (Fed. Cir. 2001). However, the challenged evidentiary ruling here is partly tied to issues of interpretation of the patent law. To this extent, we apply Federal Circuit law and review these issues of legal interpretation de novo. *Sulzer Textil A.G. v. Picanol N.V.*, 358 F.3d 1356, 1363 (Fed. Cir. 2004). To the extent that district court evidentiary rulings apply the correct legal standard, we review them for abuse of discretion. *Gen. Elec. Co. v. Joiner*, 522 U.S. 136, 141, 118 S. Ct. 512, 139 L. Ed. 2d 508 (1997) ("[A]buse of discretion is the proper standard of review of a district court's evidentiary rulings."); *see also Conservolite*, 21 F.3d at 1102 (noting district court's discretion to admit testimony on new issues in certain circumstances in action under § 146).

Congress created this court to promote a uniform interpretation of the patent laws. *C.R. Bard, Inc. v. Schwartz*, 716 F.2d 874, 878 (Fed. Cir. 1983). The cases show that the regional circuits repeatedly excluded, in some circumstances, evidence that an applicant had not presented to the Patent Office. In making discretionary decisions, courts should not lightly disregard historical practice. *See eBay Inc. v. MercExchange, L.L.C.*, 547 U.S. 388, 395, 126 S. Ct. 1837, 164 L. Ed. 2d 641 (2006) (Roberts, C.J., concurring). And the Supreme Court has warned us that "courts must be cautious before adopting changes that disrupt the settled expectations of the inventing community," even if this means rejecting a

"bright-line rule." *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 535 U.S. 722, 739, 122 S. Ct. 1831, 152 L. Ed. 2d 944 (2002).

There is long history of excluding evidence not submitted to the PTO, and of a consensus that evidence may be excluded if it was not submitted to the PTO *at least* due to fraud, gross negligence, bad faith, or intentional suppression. *See, e.g., Cal. Research*, 356 F.2d at 820 n.18 (excluding evidence not submitted to Patent Office merely due to "negligence"); *Velsicol*, 579 F.2d at 1046 (excluding evidence not submitted to Patent Office merely due to lack of "diligence"); *Killian v. Watson*, 121 U.S.P.Q. at 509 (excluding new evidence because failure to submit it to Patent Office was "grossly negligent"). The Director argues in favor of a negligence standard, although he also argues that Hyatt's conduct amounts to gross negligence. *See* Appellee's Br. at 28-53. Hyatt himself argues that the "prevailing law in the District of Columbia" is that evidence not submitted to the PTO can be excluded only if the failure was due to "gross negligence." Appellant's Br. at 27. Hyatt also states that if we exclude some evidence in § 145 actions, gross negligence should be the applicable standard. *Id.* at 28.

We note, however, that the terminology of negligence (and gross negligence) is somewhat inapposite to the issue of admissibility. Negligence (which is roughly the absence of diligence) implies a duty. While patent applicants do have certain duties to the PTO, including duties of disclosure,[29] beyond a certain point, how much more

---

[29] Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information

evidence to submit is in large part a determination for which a patentee and his agents must use good judgment.[30] While there are certainly many factors which could go into such a decision, a duty to the PTO may not necessarily be one of them. We believe a semantic shift away from negligence will help focus attention on the factors that are pertinent to whether an applicant should be allowed to introduce evidence before the district court over an objection by the Director.

Hyatt was obligated to respond to the examiner's written description rejection by *In re Alton*, 76 F.3d 1168, 1175 (Fed. Cir. 1996), by explaining where in the specification support for each of these limitations could be found. We held in *Alton* that after studying the specification, an examiner can make out a prima facie case of lack of adequate written description, thus shifting the burden of production to the applicant, simply by identifying specific claim limitations and stating that despite reviewing the specification, he could not find support for those limitations. 76 F.3d at 1175; *see also In re Wertheim*, 541 F.2d 257, 263-64 (CCPA 1976) ("[T]he PTO has the initial burden of presenting evidence or reasons why persons skilled in the art would not recognize in the disclosure a description of the invention defined by the claims;" if the PTO does so, the applicant bears the burden of rebutting this showing.); Manual of Patent Examining Procedure ("MPEP") § 2163.04(I)(B) (reiterating holding of *Alton*).

---

known to that individual to be material to patentability as defined in this section." 37 C.F.R. § 1.56(a).

[30] Information "cumulative to information already of record" is not "material to patentability." 37 C.F.R. § 1.56(b).

Any time from the January 7, 1997 office action rejecting Hyatt's new claims for Hyatt's failure to "specifically point out the support for" the claims pursuant to the examiner's reading of MPEP § 714.02 up through when Hyatt filed his initial appeal brief before the Board on September 2, 1998, Hyatt could have declared where in his specification the written description support for each of the disputed limitations resided. After the examiner stated that he had read through the specification and could find no support for certain claim limitations, all Hyatt needed to do was show the examiner where in the specification support existed—something that should have been simple for him, the person most familiar with the specification. The Board noted, "It is far easier for appellant to describe where the limitation he wrote is disclosed than for the Office to prove that the limitation is not disclosed." J.A. 11600-01. Rejection as per *Alton* was in essence the examiner telling Hyatt to point to written description support in the specification for his claims. Hyatt, however, refused to cooperate, even though he necessarily possessed the information the examiner sought by the time he filed his application.

On these facts, the district court's exclusion of Hyatt's new evidence must be affirmed. The district court found that Hyatt was "negligent" in failing to submit the evidence disclosed in the Hyatt declaration to the PTO because he was obligated to do so, he had a fair opportunity to do so, and he failed to give an adequate explanation for his failure to submit it. *Hyatt II*, 2005 WL 5569663 at *3, 5-7. However, it is clear from the record that Hyatt willfully refused to provide evidence in his possession in response to a valid action by the examiner. Such a refusal to provide evidence which one possessed was grounds in *Barrett* to exclude the with-

held evidence. Similarly, we hold that in light of Hyatt's willful non-cooperation here, the district court did not abuse its discretion by excluding the Hyatt declaration.[31]

Instead of rebutting the examiner's prima facie case that the claims were not supported by adequate written description, Hyatt argued that the burden of digging through the 238-page specification remained on the examiner, even though many limitations clearly do not appear verbatim in the specification. Before the Board, Hyatt submitted a table showing where some, but not all, of the substituent words of these limitations could be found, but this table was for many limitations of no help whatsoever in locating support for the claim limitations at issue.[32] If the Board was wrong, it was because Hyatt purposefully kept it in the dark by not presenting evidence within his possession to overcome the examiner's rejections for lack of written description. This blatant non-cooperation was willful. Allowing Hyatt to escape the consequences of his refusal to timely submit his own information to the PTO that he was required by law and

---

[31] We leave to future cases consideration of whether evidence may be excluded on grounds other than the type of refusal at issue here and in *Barrett*.

[32] For example, the examiner could find no support in Hyatt's specification for "block boundary smoothing" claim language. J.A. 20-21. According to Table-1, "block" appears on pages 25 through 83 and 128 through 164; "boundary" on pages 14 and 41; and "smoothing" once, on page 232. J.A. 10832. The words "boundary" and "smoothing" are separated by almost two hundred pages. Similarly, the examiner stated he could find no support in the specification for the claimed "quantization weighting processor." According to Table-1, "quantization" appears on pages 231 through 236, "weight" appears on pages 162 through 164, and "processor" on pages 85 through 98. To suggest Table-1 is helpful in determining where in the specification support for these limitations may be found borders on insolent.

requested by the examiner to submit would hardly be consonant with the APA or the legislative purpose of § 145.[33]

B.

Hyatt makes four arguments as to why his refusal to present responsive evidence to the PTO should not bar him from presenting his declaration in district court: (1) the Board's decision presented new grounds of rejection beyond those of the examiner and thus he was not on notice that such evidence was required; (2) he was unaware prior to this court's decision in *Hyatt I* that he bore the burden of producing evidence or explanation to rebut the examiner's written description rejections; (3) since the Board reversed the examiner's rejections for 38 of the 117 rejected claims, his efforts at providing evidence to the Board must also have been reasonable as to the remaining 79 claims; and (4) he relied on the expertise of the PTO and thus reasonably believed that the PTO did not require this evidence. We address each argument in turn.

First, we agree with the district court that the Board decision did not include any new ground of rejection. *See Hyatt II*, 2005 WL 5569663, at *6. The district court

---

[33] The instant case is distinguishable from *Burlington Industries v. Quigg*, where we upheld a district court's reversal in a § 145 action of claim rejections by the PTO. 822 F.2d 1581, 1582, 1584 (1987). We noted that the district court's decision was based largely on live testimony (which was unavailable during proceedings before the PTO) and if, under such circumstances the district court reached a conclusion different from that of the PTO, "that is not contrary to the legislative purpose of section 145 de novo review. Indeed, it is in fulfillment of that purpose." *Id.* at 1584.

correctly noted that an applicant must have an opportunity to respond to new grounds of rejection relied on by the Board. *See In re Kronig*, 539 F.2d 1300, 1302-03 (CCPA 1976). But whether a ground of rejection is "new" depends on whether the applicant had a "fair opportunity to react to the thrust of the rejection." *Id.* Here, after reviewing the Board decision and the rejections of the examiner, we agree with the district court that the Board did not rely on any new ground of rejection. For fifty-nine of the seventy-nine claims still at issue, both the Board and the examiner relied on the same rationale, namely that one or more claim limitations—which they expressly identified—are not disclosed or adequately supported in the written description. While the Board's explanations were often, though not always, more detailed, the "thrust" of these rejections was identical to that of the examiner's corresponding rejections. The Board cannot be said to have presented a new ground of rejection simply by elaborating on the examiner's rejection or by using different words. *See In re Oetiker*, 977 F.2d 1443, 1445-46 (Fed. Cir. 1992).

For the remaining twenty claims, claims 153 through 172, the district court noted that the Board may have gone beyond the scope of the examiner's rejections with regard to the claim limitation "making a product in response to image information." *See Hyatt II*, 2005 WL 5569663, at *6. However, as the district court correctly ruled, the Board's rationale as to these claims was not a new ground for rejection because it was simply a response to arguments raised by Hyatt in his briefing to the Board. See *id.* at *5-6. Thus, he had the opportunity to, and did, make arguments as to this ground. Hyatt argued for the first time to the Board that written de-

scription support existed in the specification because a "signal" could be a "product," and the Board rejected that view. Therefore, we reject Hyatt's argument that the Hyatt declaration must be admitted to afford him the opportunity to respond to the Board's new grounds for rejection because we hold that the Board did not present any new grounds.

Second, we reject Hyatt's argument that the timing of our decision in *Hyatt I* in 2007 excuses his failure to provide the Hyatt declaration to the PTO. In *Hyatt I*, we held that an examiner can shift the burden of proof of showing adequate written description by identifying specific claim limitations and clearly stating that despite reviewing the specification, he could not find support for those limitations. 492 F.3d at 1370-71. We relied directly on our 1996 decision in *Alton*, which stated the very same rule a decade earlier. *See* 76 F.3d at 1175. We then compared the *Alton* rule to MPEP § 2163.04(I)(B), which we held was a lawful articulation of the *Alton* rule. *Hyatt I*, 492 F.3d at 1370-71. Both *Alton* and MPEP § 2163.04(I)(B) were in effect at all times the '702 application was pending before the PTO. Thus, Hyatt was clearly on notice of his obligation to provide evidence or explanation to the examiner to rebut the written description rejections. His failure to do so from 1997 to 2002 thus cannot be attributed to the fact that *Hyatt I* had not yet been decided.

Third, we agree with the district court that the Board's reversal of thirty-eight of the examiner's written description rejections does not establish Hyatt acted reasonably with regard to the seventy-nine rejections not reversed. *See Hyatt II*, 2005 WL 5569663 at *6. As the district court correctly observed, the Board's rever-

sals were based solely on its own independent analysis of the claims and written description. *Id.* The Board expressly stated that it did not, and could not, rely on anything provided by Hyatt, specifically noting that Table-1 did not provide any helpful information. J.A. 11594, 11600-01. We agree with the assessments of the Board and the district court; neither Table-1 nor its accompanying notes indicate where written description support can be found for any of the claim limitations at issue. The fact that the substituent words of a claim limitation are individually used in the specification does not explain how the specification discloses the claim limitation itself, and Table-1 does not even purport to address all of the claim limitations the examiner identified as lacking written description support. Thus, neither the Board's laudable efforts to thoroughly analyze the specification even in the absence of assistance from Hyatt, nor the limited information that Hyatt did provide to the Board, indicates that Hyatt provided the PTO with the information it needed to properly assess the patentability of his claims. In fact, if anything, the Board's consideration of Table-1 demonstrates that Hyatt had the opportunity to properly provide helpful information to the Board but, for reasons we need not identify, did not.

Lastly, Hyatt's alleged reliance on the expertise of the PTO also fails to support his case. The examiner clearly indicated that, *despite his expertise*, he could not identify written description support for numerous claim limitations. It was then incumbent on Hyatt to either cite to where support could be found in the written description or amend it to add the required support. *Hyatt I*, 492 F.3d at 1371.

In sum, Hyatt presents no acceptable excuse for his failure to properly present his declaration to the PTO.

That Hyatt willfully refused to respond to the examiner's written description rejections by pointing out where in the specification support for his claims could be found is the primary reason we affirm the district court's exclusion of the Hyatt declaration. This failure of Hyatt, who at the time had been a patent agent for over twenty years, to perform a simple task that it was his burden to perform is inexcusable in the circumstances of this case. However, consideration of all the facts of this case—including the absence of an adequate explanation for Hyatt's failure to present the evidence earlier, the form of the evidence (documentary instead of testimonial), the Director's objection to the Hyatt declaration and his rehearing brief before the district court, and Hyatt's perverse unhelpfulness—only reinforces this conclusion. We hold that the district court did not commit any legal error or abuse its discretion in excluding Hyatt's declaration because of Hyatt's failure to present this evidence earlier.

C.

The dissent incorrectly describes our decision as promulgating a "sweeping exclusionary rule." *See* Dissent at 1279. We have not adopted a "sweeping" or "*per se* rule." *See id.* at 1279-80, 1287. We express no opinion as to admissibility of evidence in the multitude of variegated factual scenarios that may arise in the future which the dissent claims are decided today. The dissent also characterizes the majority opinion as standing for something that it does not: that evidence must be excluded simply because it could have been presented to

the PTO. *See* Dissent at 1284. Instead, we have merely reached the unremarkable conclusion that it is unreasonable to believe Congress intended to allow a patent applicant in a § 145 action to introduce new evidence with no regard whatsoever as to his conduct before the PTO, and that, specifically, Congress did not intend that evidence owed,[34] requested and willfully withheld from the PTO must nevertheless be admitted in a § 145 action.

The dissent also appears to misapprehend the import of *Alton*. There is, under *Alton*, only one acceptable response to a written description rejection: showing the examiner where by column and line number in the specification he may find written description support for each disputed claim limitation.[35] Here, not only was Hyatt's response to the written description rejections completely and wholly inadequate, it was willfully so. He simply refused to respond as required by *Alton* to the requests of the examiner for citations to the specification, and he clearly did so deliberately, thus impeding the examination the PTO is legally required to conduct. Here, not only was Hyatt's response to the written description rejections completely and wholly inadequate, it was willfully so. He simply refused to respond as required by *Alton* to the requests of the examiner for citations to the

---

[34] The dissent's claim that we hold that Hyatt "'owed' the PTO *all evidence he possesses* that is responsive to a rejection," Dissent at 1279-80 (emphasis added, citation omitted), is overbroad and illustrates the dissent's misunderstanding of our holding.

[35] The dissent complains about Hyatt's burden of responding to, as the dissent calculates it, "2546 separate rejections." Dissent at 1288. The dissent does not acknowledge that this is proportional to Hyatt's prosecution of an application containing 117 pending claims spanning 79 pages. *See* J.A. 10411-89.

specification, and he clearly did so deliberately, thus impeding the examination the PTO is legally required to conduct.

IV.

Since Hyatt did not offer any other evidence in his § 145 action, the district court correctly reviewed the Board's decision solely on the record before the Board. We review a district court's grant of summary judgment de novo, applying the same standards as the district court. *Ethicon Endo-Surgery v. U.S. Surgical Corp.*, 149 F.3d 1309, 1315 (Fed. Cir. 1998). In the § 145 context, in the absence of new evidence, the district court must enter judgment for the Director if the Board's findings regarding the lack of adequate written description are supported by substantial evidence. *See In re Curtis*, 354 F.3d 1347, 1352 (Fed. Cir. 2004) (whether written description adequately supports claims is issue of fact); *Mazzari*, 323 F.3d at 1004-05 (absent new evidence, PTO fact-finding reviewed under substantial evidence standard in § 145 actions).

Hyatt argues that the Board's decision was not supported by substantial evidence because the record before the Board cited and contained adequate written description for all the claims rejected by the Board. When examined more closely, however, Hyatt's arguments rely almost entirely on Table-1. As noted earlier, Table-1 simply lists certain individual words used within various multi-word limitations, the number of times each such word appears in the specification, and "representative" pages in the specification where each word appears (or, in many cases, simply states that the word appears "throughout" the specification). For example, certain

claims were rejected for lacking written description support for a "processor responsive to an accessed block of video pixel image information." J.A. 10643 ¶ 15. Table-1 indicates that "block" was used over 80 times on at least pages 25-83 and 128-164 of the specification; "information" was used over 100 times "throughout" the specification; "video" was used exactly eight times on at least pages 77, 166, and 168-71; etc. J.A. 10832. Table-1 does not, however, explainhow any of these individual occurrences of these substituent words discloses a "processor responsive to an accessed block of video pixel image information." The same defect exists in each of Hyatt's arguments relying on Table-1 and so we are not persuaded by them.

In addition, Hyatt repeatedly points to raw source code printed in the specification as disclosing various features of his claims. Aside from self-serving attorney arguments, Hyatt points to no evidence that would enable the district court or this court to determine whether the source code actually does disclose these features. Moreover, he made the same unsupported arguments to the PTO, and despite its expertise the PTO found them to be unhelpful in determining whether the written description adequately supported the claims at issue. We therefore agree with the district court that the Board's decision was supported by substantial evidence. There was no error in the district court's grant of summary judgment.

CONCLUSION

For the reasons stated above, the district court's grant of summary judgment is

AFFIRMED.

MOORE, Circuit Judge, dissenting.

The majority takes away this patent applicant's fundamental right to a "civil action to obtain [a] patent" as granted by Congress in 35 U.S.C. § 145. Today the majority decides that a patent applicant may not introduce the inventor's declaration in a § 145 proceeding before the district court because the inventor had an "affirmative duty" or "obligation" to disclose this evidence to the PTO. His failure to fulfill his affirmative duty, by not disclosing evidence he could have disclosed to the PTO, results in such evidence being excluded from the district court § 145 proceeding. The district court made no fact findings indicating willful withholding or intentional suppression; in fact, the district court did not even conclude that Mr. Hyatt's conduct amounted to gross negligence, but rather excluded the evidence under a negligence "could have" standard. Nor did the PTO even argue, at any stage of these proceedings, that Mr. Hyatt's conduct in this case was willful or intentional. Nonetheless, the majority concludes that the applicant "owed," Maj. Op. at 1278, the PTO all evidence he possesses that is responsive to a rejection and that failure to fulfill this newly created "affirmative duty" amounts to willful withholding as a matter of law. There are only two possible ways to interpret the majority's willful withholding determination. Either the majority is engaging in appellate fact finding or it is determining that breach of its newly created affirmative duty is willful withholding as a matter of law. The latter leaves no room for fact finding in individual cases and takes the discretion completely away from the trial court. Ultimately, the majority's sweeping exclusionary rule is far broader than anything argued by the parties.

While the Supreme Court has characterized the § 145 action as a proceeding that is "in fact, and necessarily, a part of the application for the patent," the hallmark of the § 145 proceeding in the district court is that "all competent evidence" shall be heard subject only to "the ordinary course of equity practice and procedure." *Gandy v. Marble*, 122 U.S. 432, 439, 7 S. Ct. 1290, 30 L. Ed. 1223 (1887); *see also Butterworth v. United States ex rel. Hoe*, 112 U.S. 50, 61, 5 S. Ct. 25, 28 L. Ed. 656 (1884). To be clear, Mr. Hyatt does not argue that § 145 actions are de novo trials that are entirely separate from PTO proceedings. Mr. Hyatt argues only that new evidence may be admitted in a § 145 action. He acknowledges that deferential review (substantial evidence) is given to Board fact findings absent new evidence in § 145 proceedings and also that evidence pertaining to new issues cannot be introduced. *See* Appellant's Br. 1, 5, 8, 10-11, 14-15; *see also Conservolite, Inc. v. Widmayer*, 21 F.3d 1098 (Fed. Cir. 1994) (holding that in a § 146 action, evidence pertaining to new issues that were not raised before the PTO may be excluded).

The majority's decision to affirm the district court's exclusion of the inventor's own declaration in a § 145 civil action severely restricts the rights that Congress afforded patent applicants, making this proceeding more of an appeal than the new civil action contemplated and enacted by Congress. Moreover, by concluding that an inventor has an "affirmative duty" to submit his own declaration in response to a rejection by the PTO, lest he be prevented from admitting the material in any subsequent district court proceeding, the majority makes it impossible for inventors to ever testify in a § 145 action unless their testimony had first been proffered to the PTO. I cannot agree that this was what Congress con-

templated when it enacted § 145, and therefore I dissent.

I. Mr. Hyatt's Declaration Should Not Be Excluded

Congress enacted a statute that permitted a "civil action" and gave patent applicants the right to present new evidence in a trial in the district court despite that this right would allow the applicant to introduce "evidence that they could have brought in before" the PTO, potentially resulting in "dragging an opponent through a second time." *To Amend Section 52 of Judicial Code and Other Statutes Affecting Procedure in Patent Office: Hearings on H.R. 6252 and H.R. 7087 Before the H. Comm. on Patents*, 69th Cong., 1st Sess. 80-81 (1926) (statement of Hon. Thomas E. Robertson, Commissioner of Patents) [hereinafter *To Amend Section 52*]. Congress granted patent applicants the right to a civil action in the district court distinct from their right of appeal. It is our obligation to protect the distinction Congress codified in § 145, not to reweigh the virtues of that decision. The § 145 proceeding is a civil action and ought to be governed by the same Federal Rules of Evidence that govern other civil actions. Patent cases do not need, nor should they have, special rules of evidence.

Section 145, titled "Civil action to obtain a patent," provides:

> An applicant dissatisfied with the decision of the Board of Patent Appeals and Interferences in an appeal under section 134(a) of this title may, unless appeal has been taken to the United States Court of Appeals for the Federal Circuit, *have remedy by civil action* against the Director in the United States District Court for the District of Columbia if com-

> menced within such time after such decision, not less than sixty days, as the Director appoints. *The court may adjudge* that such applicant is entitled to receive a patent for his invention, as specified in any of his claims involved in the decision of the Board of Patent Appeals and Interferences, *as the facts in the case may appear* and such adjudication shall authorize the Director to issue such patent on compliance with the requirements of law. All the expenses of the proceedings shall be paid by the applicant.

35 U.S.C. § 145 (emphasis added).

The statute itself distinguishes the appeal that may be brought pursuant to 35 U.S.C. § 141 because a § 145 action is not an appeal; it is a "civil action." The statute obligates the district court to adjudicate the facts in this civil action. Because the statute affords no limitations on the type of evidence that ought to be admissible in a civil action brought under § 145, the standard Federal Rules of Evidence that govern all civil actions ought to govern. The legislative histories of § 145 and its predecessor statute, section 4915 of the Revised Statutes, repeatedly *and without contradiction* indicate that the intent of Congress was to permit a patent applicant to bring a new suit built upon a new record. In testimony leading to the Patent Act of 1927, the Commissioner of Patents referred to a section 4915 suit as one where an applicant would proceed "*de novo*" in district court, with the right "to build up a new record" and bring in "further evidence that I might have put in before and drag you through another trail [sic] court." *To Amend Section 52*, at 79-80. The Commissioner of Patents was testifying in opposition to this statute, to this civil action in the district court. He testified that this statute that per-

mits this "new record" results in "dragging an opponent through a second time." *Id.* at 80. In fact, he articulated these concerns a second time, noting that the statute allowed a patent applicant to "file testimony bringing in evidence that they could have brought in before [the PTO] but did not bring in before, and after dragging a man through all this procedure which you have just said is so complicated and burdensome, start *de novo* in court, and bring in testimony not taken the first time." *Id.* at 81; *see also id.* at 76 (statement of Karl Fenning, Former Assistant Commissioner of Patents) (arguing that "the best thing to do would be to cut out 4915 entirely for ex parte applications" to encourage the applicant to "put in all the testimony pertinent to his case" before the PTO).

Despite being presented with the policy reasons for not permitting a civil action, which allows the applicant to bring in evidence *he could have brought before the PTO*, Congress decided to adopt this approach. Mr. A.C. Paul, Chairman of the Patent Section of the Legislation Committee of the American Bar Association, made clear that he too understood section 4915 to permit the introduction of new evidence:

> While our committee would have the case start *de novo* after the decision of the board . . . and the difference would be then if we went to the court of appeals by an appeal the decision must be based upon the same record. If we go into a court of equity the parties may use the record that they have in the Patent Office and may supplement it by additional evidence.

Id. at 81. Similarly, Congressman Albert H. Vestal stated that "if a party feels aggrieved, he can bring his suit

in the equity court, but it is not an appeal. It is the bringing of a new suit." *Id.* at 36.[1] Charles E. Howson, Chairman of the Committee on Patent Law Revision for the American Bar Association, who was the "chairman of the committee that drew these bills" explained:

> The advantage of section 4915 is that it enables the party in interest, desiring to obtain a patent, to take evidence in a court or tribunal whose business it is to try issues of facts *and make up a record in addition to that he has been enabled to furnish the examiners in the Patent Office*, and therefore get before a court of competent jurisdiction everything connected with his rights and every fact connected with his patent; in other words, *have before him everything that courts in the country have before them in infringement cases.*

Id. at 21 (emphasis added); *see also To Amend the Statutes of the United States as to Procedure in the Patent Office and the Courts: Hearing Before the S. Comm. on Patents*, 69th Cong., 2d Sess. 13-14 (1926) (statement of Otto R. Barnett) (Pursuant to section 4915, you may file an action in the district court if "you want a new record to bring out new things developed in your patent, in lieu of that you may file a new suit. . . . Now, when it came to ex parte cases, it was comparatively simple to say that

---

[1] *See also* Albert H. Walker, *The Law of Patents for Inventions* § 134 (5th ed. 1917) ("In order to decide the issues of such a bill in equity as is treated in this section, the court, where the bill is pending, will take testimony, and any other admissible evidence, according to the course of courts of equity; and will also consider whatever was before the Patent Office in the proceedings which resulted in the refusal to grant a patent . . . . The proceeding, however, is not revisory of the Patent Office proceeding, but is an original suit in equity . . . . ").

the individual inventor may appeal, or he may start his new suit. . . . 'Well, somebody may want to start a new suit and bring out other and new things.' So we said, 'All right, take your choice; go on with a new suit, or appeal.'").

These numerous statements confirm that when Congress enacted this statute, which does not limit the evidence that may be introduced in this "new suit" or "civil action," Congress did so with this purpose and intent. The majority attempts to sweep away all of the legislative history (as "anachronistic") claiming that the mere existence of *Barrett* "suggests that Congress approved of the cases holding that patent applicants could not present to a district court evidence they should have but did not present to the Patent Office." Maj. Op. at 1271-73. There are several problems with this theory. First, the parties agree and Congress clearly stated that the 1952 patent act made no substantive changes to § 4915. *See* Appellant's Br. 16; Appellee's Br. 45; S. Rep. No. 82-1979 (1952), *as reprinted in* 1952 U.S.C.C.A.N. 2394, 2400. Second, even the few courts that excluded evidence prior to the 1952 patent act did so under a hodgepodge of different standards (diligence, intentional suppression or bad faith). Congress could not have implicitly adopted all of these differing standards. Indeed, Congress did not limit the type of evidence that the patent applicant may introduce precisely because it intended for a civil action under § 4915, now § 145, to be based upon a new record and new evidence, even if that new evidence could have been brought before the PTO. Congress intended that the district court in a § 145 action have everything that a court would have in an infringement suit. Under this standard, Congress cer-

tainly intended for an inventor, such as Mr. Hyatt, to be permitted to introduce his own declaration in a § 145 action.[2]

Moreover, to deter applicants from exactly the type of procedural gaming that concerns the majority, § 145 imposes on the applicant the heavy economic burden of paying "[a]ll the expenses of the proceedings." 35 U.S.C. § 145. This burden encourages applicants to present their best case to the PTO to avoid responsibility for all expenses in a § 145 proceeding. To allow this type of evidence in these civil actions was a policy decision committed solely to the discretion of Congress, which it duly made.

Not only does the majority decision conflict with the proper interpretation of § 145, but it is also in conflict with Supreme Court jurisprudence on this point. The Supreme Court has repeatedly and without limitation spoken to an applicant's right to "present to the court evidence that the applicant did not present to the PTO. The presence of such new or different evidence makes a factfinder of the district judge." *Dickinson v. Zurko*, 527 U.S. 150, 164, 119 S. Ct. 1816, 144 L. Ed. 2d 143 (1999). Supreme Court jurisprudence reflects a strong distinction between a § 141 appeal, in which new evidence is not permitted, and a § 145 action and its precursors, in which new evidence is freely admitted. A civil

---

[2] The Federal Rules of Evidence do not support the majority's exclusion of inventor statements. Inventor testimony is regularly admitted in infringement cases for various reasons: *Wang Labs., Inc. v. Toshiba Corp.*, 993 F.2d 858, 866 (Fed. Cir. 1993) (written description); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1317 (Fed. Cir. 2005) (en banc) (claim construction); *Cooper v. Goldfarb*, 154 F.3d 1321, 1330 (Fed. Cir. 1998) (reduction to practice); *Symantec Corp. v. Computer Assocs. Int'l, Inc.*, 522 F.3d 1279, 1295 (Fed. Cir. 2008) (conception).

action under § 145—like the bill in equity before it and unlike an appeal—is "the exercise of original, the other of appellate, jurisdiction." *In re Hien*, 166 U.S. 432, 438, 17 S. Ct. 624, 41 L. Ed. 1066 (1897). A defining difference between an appeal and the bill in equity is the introduction of new evidence:

> It is evident that alternative rights of review are accorded an applicant,—one by appeal to the United States Court of Customs and Patent Appeals, the other by bill in equity filed in one of the federal district courts. In the first the hearing is summary and solely on the record made in the Patent Office; in the other a formal trial is afforded on proof *which may include evidence not presented in the Patent Office.*

Hoover Co. v. Coe, 325 U.S. 79, 83, 65 S. Ct. 955, 89 L. Ed. 1488 (1945) (citation omitted); *id.* at 87, 65 S. Ct. 955 (explaining that the legislative history makes clear that Congress intended to save to "litigants the option of producing new evidence in court, by retaining the equity procedure"); *see also Hill v. Wooster*, 132 U.S. 693, 697, 10 S. Ct. 228, 33 L.Ed. 502 (1890) ("The opinion of the circuit court discusses . . . and states that considerable evidence was produced before the court which was not before the patent-office."). And the Supreme Court has distinguished an appeal from the bill in equity under section 4915 (the precursor to § 145):

> It is thereby provided [in section 4915] that the applicant may have remedy by bill in equity. This means a proceeding in a court of the United States having original equity jurisdiction under the patent laws, *according to the ordinary course of equity practice and procedure.* It is not a technical appeal from the patent-office, like that authorized in section

> 4911, confined to the case as made in the record of that office, but is prepared and heard upon *all competent evidence* adduced, and upon the whole merits. Such has been the uniform and correct practice in the circuit courts. *Whipple v. Miner*, 15 F. 117 (C.C.D. Mass. 1883); *Ex parte Squire*, 3 Ban. & A. 133; *Butler v. Shaw*, 21 F. 321.

Butterworth, 112 U.S. at 61, 5 S.Ct. 25 (emphasis added).

In *Butterworth*, the Supreme Court held that a section 4915 action should be heard on "all competent evidence," which is governed "according to the ordinary course of equity practice and procedure." *Id.* The majority explains that competent evidence is synonymous with admissible evidence, *see* Maj. Op. at 1260 n.12, but suggests that the Supreme Court was silent on what evidence was competent (admissible). In fact, the preceding sentence in *Butterworth* explained that the admissibility or competence is determined "according to the ordinary course of equity practice and procedure" (i.e. the Federal Rules of Evidence and Civil Procedure). *Butterworth*, 112 U.S. at 61, 5 S. Ct. 25. Evidence is admissible in a § 145 civil action limited only by the ordinary rules of evidence and procedure that apply to all civil actions. The majority claims that reading *Butterworth* as holding that evidence is admissible in a § 145 civil action limited only by the ordinary rules of evidence and procedure that apply to all civil actions is contrary to the Supreme Court's decision in *Gandy*. However, the very quote in *Gandy* that the majority cites for this proposition, Maj. Op. at 1260, reaffirms this holding of *Butterworth*. The fact that the "proceeding, is, in fact and necessarily, a part of the application for the patent,"

is not to the contrary. The cases endorsed by the Supreme Court in *Butterworth*, like the Supreme Court itself, hold that the section 4915 action is one in which any *evidence* may be admitted:

> It would seem, therefore, that the course of proceeding in either case is clear-viz., "according to the course of equity." Even in the absence of these explicit terms it would be apparent that a suit in equity would have to be governed in its proceedings by equity rules. . . . The provisions of the acts of congress, already referred to, allowing the party failing in his application, to file a bill, do not restrict the hearing, in this court, to the testimony used before the commissioner. *Either party, therefore, is at liberty to introduce additional evidence, or rather, to speak more accurately, the hearing is altogether independent of that before the commissioner, and takes place on such testimony as the parties may see fit to produce agreeably to the rules and practice of a court of equity.*

Ex parte Squire, 22 F. Cas. 1015, 1017 (C.C.E.D. Mo. 1877) (No. 13,269) (emphasis added).[3] This case, which on this very point the Supreme Court held was "cor-

---

[3] *See also Butler v. Shaw*, 21 F. 321, 326 (C.C.D. Mass. 1884) (distinguishing between the patent applicant's right to appeal where "that court acts strictly as a court of appeal in the matter . . . the hearing is summary, and is confined to the specific reasons of appeal, and to the evidence produced before the commissioner" and the patent applicant's right to file a "bill in equity" under section 4915, which is "a suit within the ordinary jurisdiction in equity of the courts . . . the statute contains no provision requiring the case to be heard upon the evidence produced before the commissioner . . . as has been held in this and other circuits, the court may receive new evidence, and has the same powers as in other cases in equity").

rect," holds that the only limitations on evidence that may be introduced in these proceedings are those limitations that arise under the normal rules—in this case the Federal Rules of Evidence. *See id.*

The majority discusses the importance of preserving settled expectations. Our own precedent is replete with examples of § 145 actions in which district courts considered new evidence that could have been presented to the PTO but was only first presented to the district court. *See, e.g., Fregeau v. Mossinghoff*, 776 F.2d 1034, 1036 (Fed. Cir. 1985) (applicant submitted a new expert declaration setting forth additional data and a new theory to the district court); *Titanium Metals Corp. of Am. v. Banner*, 778 F.2d 775 (Fed. Cir. 1985) (new expert testified in district court); *Gould v. Quigg*, 822 F.2d 1074 (Fed. Cir. 1987) (both the PTO and the patent applicant offered new expert testimony); *Mazzari v. Rogan*, 323 F.3d 1000, 1004-05 (Fed. Cir. 2003) (allowing a large volume of new evidence offered by the applicants and the PTO including new experts and prior art references); *see also Winner Int'l Royalty Corp. v. Wang*, 202 F.3d 1340, 1346-48 (Fed. Cir. 2000) (allowing new evidence of commercial success to be introduced in the district court proceedings); *Genentech, Inc. v. Chiron Corp.*, 220 F.3d 1345, 1351 (Fed. Cir. 2000) (permitting four new experts to testify despite the fact that none of them had offered any testimony by declaration, affidavit, or otherwise during proceedings at the PTO). We have repeatedly held that a § 145 applicant is "entitled" to and may "choose" to introduce additional evidence. *See Mazzari*, 323 F.3d at 1004-05 ("A section 145 review . . . affords the applicant an opportunity to present additional evidence or argue the previous evidence afresh," and "[i]f

the parties choose to present additional evidence to the district court . . . the district court would make *de novo* factual findings."). In *Newman v. Quigg*, 877 F.2d 1575 (Fed. Cir. 1989), we held that the PTO could introduce several new reports, declarations, and affidavits not submitted during the PTO proceedings explaining:

> A district court action under 35 U.S.C. § 145 is a *de novo* determination of patentability. It is not limited to the record before the PTO. Unless a party is prejudiced thereby or due process is denied, expeditious justice is better served by avoiding artificial restrictions on the district court's authority to resolve all issues reasonably raised in the proceeding.

Id. at 1579 (citation omitted). These cases illustrate the great magnitude of the majority's departure from decades of practice in which both parties believed such evidence admissible. The majority's decision to start excluding evidence in § 145 actions is contrary to the statute, legislative history, Supreme Court precedent, and the long-standing practice of considering such evidence in our cases.[4]

---

[4] Although not considered below or raised or argued by the parties on appeal, the majority contends that the APA requires "[s]ome restrictions on the ability of an applicant to introduce new evidence in a § 145 action." Maj. Op. at 1270. There is little doubt that, as a general matter, the APA applies to PTO actions. *Zurko*, 527 U.S. at 165, 119 S. Ct. 1816. But *Zurko* acknowledged that § 145 allows applicants to "present to the court evidence that the applicant did not present to the PTO. The presence of such new or different evidence makes a factfinder of the district judge." *Id.* at 164, 119 S. Ct. 1816. And in a case considering the applicability of *Zurko* to § 145, we stated that "[a] section 145 review is distinct from a section 141 appeal in that it affords the applicant an opportunity to present additional evidence or argue the previous evidence afresh." *Mazzari*, 323 F.3d at 1004. While *Zurko* and

II. The New *Alton* Rule for Excluding Evidence

After a lengthy discussion of the hodgepodge of standards that were applied in the few regional circuits that had excluded evidence from district court proceedings, the majority affirms the district court's exclusion of evidence.[5] The authority, according to the majority, is

---

Mazzari concerned the standard of review, both cases considered the APA and both cases proceeded on the uncontroversial premise that the applicant can "choose" to present "new or different evidence" in a § 145 action. Further, as explained in detail *supra*, the language and legislative history of § 145 resoundingly support the admissibility of new evidence in § 145 actions. *Cf. Chandler v. Roudebush*, 425 U.S. 840, 862, 96 S. Ct. 1949, 48 L. Ed. 2d 416 (1976) ("Here, by contrast, there is a 'specific statutory authorization' of a district court 'civil action,' which both the plain language of the statute and the legislative history reveal to be a trial de novo."). The APA does not limit new evidence in a § 145 proceeding to live testimony to resolve credibility issues as the majority asserts. Maj. Op. at 1270-71.

[5] To the extent that regional circuits or lower courts excluded evidence in § 145 actions, there is considerable disagreement as to the standard that ought to govern the exclusion of such evidence (gross negligence, intentional suppression, bad faith, or negligence/diligence). *See, e.g., Case v. CPC Int'l, Inc.*, 730 F.2d 745, 752 (Fed. Cir. 1984) ("We are aware that this provision *has received varying interpretations in the circuits*. In our view, since an action under 35 U.S.C. § 146 has the hybrid nature of an appeal and a trial de novo, the statute authorizes the district court to accept all proffered testimony on issues raised by the parties during the proceedings below or by the board's decision." (emphasis added)). In fact, the negligence/diligence standard applied in this case was recently rejected by the very court from which this appeal comes:

> As a threshold matter, the Court must determine whether plaintiff may, under Section 145, offer the four new declarations not previously submitted to the Board . . . . Defendant contends that the Court should not consider these new declarations because they were not previously submitted to the Board . . . . There is no indication

In re Alton, 76 F.3d 1168, 1175 (Fed. Cir. 1996). The majority holds that by failing to offer his testimony to the PTO, Hyatt has failed to satisfy "an affirmative and specific duty." Maj. Op. at 1248. In this way, this new affirmative duty for prosecution seems to resemble inequitable conduct, though here the applicant is penalized regardless of their intent. The majority explains: "Hyatt was obligated to respond to the examiner's written description rejection by *In re Alton*, 76 F.3d 1168, 1175 (Fed. Cir. 1996), by explaining where in the specification support for each of these limitations could be found." Maj. Op. at 1274.[6] The majority continues:

---

here that plaintiff's failure to introduce the four declarations rises to the level of fraud, bad faith, or gross negligence.

Defendant, however, points to a handful of cases in this Court, which have adopted an even more stringent standard for the consideration of new evidence. Defendant relies primarily on *Hyatt v. Dudas*, in which Judge Kennedy declined to consider new evidence "negligently submitted after the end of administrative proceedings." This articulation of the "new evidence" standard represents a significant departure from the PTO's guidelines and, as plaintiff argues, would "render an appeal under § 145 . . . nearly indistinguishable from a direct appeal to the Federal Circuit, and would render the purpose of the statute duplicative and meaningless." The Court therefore declines to adopt the *Hyatt* standard for considering new evidence in this case.

Hitachi Koki Co. v. Dudas, 556 F. Supp. 2d 41, 47 (D.D.C. 2008) (citations omitted).

[6] The majority suggests that there is only one way to respond to a written description rejection. Maj. Op. at 1278 ("There is, under *Alton* only one acceptable response to a written description rejection: showing the examiner where by column and line number in the specification he may find written description support for each disputed claim limitation."). With all due respect, this not correct. Written description rejections can be addressed by arguing, for example, that the examiner failed to set forth a prima facie case, by amendment, by adjusting a

"Hyatt was clearly on notice of his obligation to provide evidence or explanation to the examiner to rebut the written description rejections," Maj. Op. at 1276, and "he was required by law" to provide it. Maj. Op. at 1275. With all due respect to the majority, I do not believe a new "affirmative duty" to disclose is warranted, nor do I believe Hyatt was "required by law" or "obligated" to provide his declaration to the PTO. While Mr. Hyatt may have failed to overcome the rejections or to convince the Board based upon his submissions to the PTO, he did not fail to fulfill an "obligation" or "affirmative duty" as the majority alleges.

The majority uses *Alton* to create an "affirmative duty" with which patent applicants must comply. *Alton* does not justify this new duty. *Alton* stands for the proposition that when the examiner makes a prima facie case for his written description rejection, the burden of coming forward with evidence or argument (burden of production) shifts to the applicant. *Alton*, 76 F.3d at 1175. And, this is true whether the examiner is rejecting a claim on the basis of anticipation, obviousness, enablement, written description or any other reason. *See In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992) ("[T]he examiner bears the initial burden, on review of the prior art or *on any other ground*, of presenting a prima facie case of unpatentability. If that burden is met, the burden of coming forward with evidence or argument shifts to the applicant."); *see also Manual of Patent Examination Procedure* § 804 ¶ I.A (8th ed., rev.

---

priority claim, or by pointing out common alternative definitions for a claim term known to one of ordinary skill in the art. There is not simply one way an applicant can or must respond, and we should not micromanage prosecution.

2008); *id.* § 2106 (patentable subject matter), § 2107.02 (utility), § 2112 (inherent anticipation), § 2142 (obviousness), § 2163.04 (written description), § 2164.04 (enablement), § 2184 (equivalents). Once the examiner makes a prima facie case, the applicant then has the burden of coming forward with evidence to rebut that prima facie showing.

Because the same burden shifting occurs with regard to every type of rejection an examiner makes, this new affirmative duty is not limited to the written description issue reviewed in *Alton*. Hence if the burden shifting creates "an affirmative duty" then this affirmative duty comes into existence every time an examiner makes a prima facie case and rejects claims. I cannot agree with the per se rule that an applicant is deemed to have willfully withheld anything he possessed during prosecution that was responsive to a rejection regardless of the applicant's actual intent. Willfulness always requires intent and is simply not compatible with the majority's strict liability approach.

III. Mr. Hyatt's Evidence

In this case, the district court found that Mr. Hyatt's failure to proffer his declaration to the PTO was merely negligent. *Hyatt v. Dudas*, No. 03-0901, 2005 WL 5569663 (D.D.C. Sept. 30, 2005) ("*Hyatt II*") ("Hyatt's failure to explain why he didn't submit his declaration earlier is negligent, and the district court need not consider evidence negligently submitted after the end of administrative proceedings."). There has been no finding of bad faith, fraud, willful withholding, intentional suppression or even gross negligence in this case. The PTO did *not* argue to either the district court or this

court that the facts in this case would establish intentional suppression or willful withholding by Mr. Hyatt. Rather, the PTO argued that the facts established that Mr. Hyatt acted negligently or in the alternative grossly negligently. Appellee's Br. 51-53. In fact, the PTO argues that Mr. Hyatt's focus on "intentional or deliberate conduct misses the point." Appellee's Br. 51. Analogizing the present case to *Schering Corp. v. Marzall*, 101 F. Supp. 571 (D.D.C. 1951), the PTO distinguishes between suppression on the one hand and evidence withheld without sufficient excuse on the other. *Id.* at 34-35. If the majority would like the willful withholding standard to be applied and for fact findings to be made accordingly, it must vacate and remand for the district court to do so in the first instance. Because willful withholding was not argued by the parties or considered by the district court, we as an appellate court simply cannot know the volume of evidence that may exist on the issue nor are we in a position to judge Mr. Hyatt's credibility.

I find troubling the majority's characterizations of Mr. Hyatt. *See, e.g.*, Maj. Op. at 1275 (Mr. "Hyatt purposefully kept [the Board] in the dark"); *id.* (his "blatant noncooperation"); *id.* at 1275 (Mr. "Hyatt willfully refused to provide evidence in his possession"); *id.* (Hyatt "refused to cooperate"); *id.* ("Hyatt's willful noncooperation"); *id.* at 1277 ("Hyatt willfully refused"); *id.* at 1274 (providing his declaration "should have been simple for him"); *id.* at 1277 (that Hyatt's failure "to perform a simple task that it was his burden to perform is inexcusable"); *id.* at 1277 ("Hyatt's perverse unhelpfulness"). None of this appears in the district court proceedings, the PTO proceedings, or the record—these fact findings ought to be left to the district court which

is in the best position to weigh the contradictory evidence.

Contrary to the appellate finding of willful withholding, the record contains ample evidence of a lack of willful withholding. Here, the examiner rejected all of Mr. Hyatt's 117 claims for lack of written description, failure to enable, obviousness-type double patenting (over 8 separate references), and *Schneller*-type double patenting (over the same 8 references). The examiner also rejected 9 claims as anticipated (*Hill* reference) and 7 as obvious (over a combination of three references). Technically, Mr. Hyatt was appealing 45 separate issues totaling 2546 separate rejections of his 117 claims to the Board. He wrote a 129-page appeal brief addressing *all* of these different rejections.[7] And, to be clear, the Board reversed all the examiner's rejections for obviousness, anticipation, obviousness-type double patenting, Schneller-type double patenting, and many of the written description and enablement rejections. With regard to the written description rejections in particular, the Board reversed the rejections of 38 claims and sustained the rejections of 79 claims. Mr. Hyatt prevailed on 92% of all the examiner's rejections at the Board level. Despite Mr. Hyatt's success, the majority declares Mr. Hyatt's response to be "completely and wholly inadequate" and Mr. Hyatt to have been perversely unhelpful. Maj. Op. at 1277, 1278.

With respect to the written description issue, Mr. Hyatt responded to the rejections—as the majority explains—with thirty six pages of argument and Table-1.

---

[7] Mr. Hyatt prosecuted his patent application pro se. This is not to suggest that Mr. Hyatt is unsophisticated, as he is an inventor with several patents to his credit and a patent agent.

While the Board criticizes Table-1, the Board reversed thirty-eight of the examiner's rejections for lack of written description and in some cases relied upon exactly the information referenced in Table-1. For example, the Board found support for "a data decompressed video image input circuit generating data decompressed image information" (in thirty-three claims) on page 23 of the 236-page specification, the exact and only location where table-1 says the terms "data compressed" and "decompressed" appeared. *See, e.g., Ex Parte Hyatt*, No. 2000-2049 (B.P.A.I. July 30, 2002) at 19-20. Although Mr. Hyatt may have failed to overcome all of the written description rejections based upon his submissions to the PTO, he did not fail to fulfill an "obligation" or "affirmative duty," and he certainly was not "perversely unhelpful" as the majority alleges. With all of these facts, and no one arguing willful withholding, should we be finding it in the first instance? I believe the court is wrong to hold that breach of the newly created affirmative duty, i.e., not producing evidence to the PTO, is willful withholding as a matter of law.

It is helpful to compare these facts to one of the only examples of willful withholding, where a court excluded evidence of reduction to practice where the assignee corporation expressly refused to disclose and to allow their witnesses to answer questions before the PTO in order to maintain a commercial advantage. *Barrett*, 22 F.2d at 396 ("[T]he Barrett Company forbade them to answer."). *Barrett* represents an extreme and unwarranted position, and the majority chooses to go far beyond even that standard. Mr. Hyatt's conduct here hardly rises to the level of the Barrett Company. There is no evidence that Mr. Hyatt intentionally withheld information to retain some commercial advantage, as in

Barrett. Rather, the majority concludes that where an applicant fails to convince the PTO of his position, he is foreclosed from bringing in new evidence to further that position in a § 145 action, regardless of whether he believed he had submitted adequate evidence to the PTO—i.e., regardless of the applicant's intent.

In hindsight, perhaps Mr. Hyatt should have submitted his declaration or that of any other expert earlier in the prosecution process. But hindsight is misleadingly acute. Declarations and expert reports are time consuming and expensive to prepare. It is hardly reasonable or even desirable to require patent applicants to put massive declarations into the record at an early stage of prosecution, weighing the cost to both the applicant and the PTO. *See generally* Mark A. Lemley, *Rational Ignorance at the Patent Office*, 95 Nw. U. L. Rev. 1495 (2003) (arguing that it would be inefficient for the PTO to overinvest in examination because so few patents are enforced). In this case, for example, the examiner rejected the claims on many different bases (double patenting on 8 different references, obviousness, anticipation, enablement, written description, etc.), totaling 2546 separate rejections. The Board overturned nearly all of them. It is easy with the benefit of hindsight to say Mr. Hyatt should have introduced more evidence on written description to the Board. But Mr. Hyatt was not facing merely a written description rejection, he was facing 2546 separate rejections on many, many different bases. The majority implausibly asserts that 2546 separate rejections is "proportional to Hyatt's prosecution of an application containing 117 pending claims spanning 79 pages." Maj. Op. at 1278 n. 35. An average of 21 rejections per claim is hardly proportional. Mr. Hyatt was forced to appeal 45 independent issues to the Board

when the average is two. Dennis D. Crouch, *Understanding the Role of the Board of Patent Appeals in Ex Parte Appeals*, 4, available at http://papers.ssrn.com/sol3/papers.cfm?abstract_id=142392295. Despite this challenge, Mr. Hyatt was largely successful on appeal. Further, the length of Mr. Hyatt's application suggests that his efforts to pinpoint pages containing certain terms was helpful and in good faith. Mr. Hyatt's response may have been especially valuable in the time before searchable electronic applications.

To say that Mr. Hyatt had an affirmative duty to introduce all evidence to the Board or that he "owed" (Maj. Op. at 1278) all the evidence he possessed is to put an enormous and undesirable burden on the patentee, one that will foreclose patent protection for many small inventors. Congress foresaw exactly this problem and ameliorated it with § 145 by providing applicants a way to initiate a civil action and introduce new evidence after Board proceedings when the issues are much more succinct and consolidated. This is illustrated perfectly here, where the applicant was contending with 2546 rejections on many different bases before the Board. After the Board overturned nearly all of them, only a small number of rejections—based on written description/enablement—were maintained. Hence at the district court the applicant could proffer much more extensive evidence because the universe of issues was greatly narrowed. This is the sensible approach Congress enacted. The statute even places the cost of the proceeding on the party better positioned to know the value of the application—the applicant. The majority's new exclusionary rule based upon its new affirmative duty upsets this balance.

CONCLUSION

In this case, the majority blurs the line between an appeal pursuant to § 141 and the civil action of § 145. The admissibility of new evidence is exactly what distinguishes § 145 from § 141. "We must be vigilant to preserve to patent applicants the alternative procedures that the law provides, and to preserve the historical distinction between them." *Fregeau*, 776 F.2d at 1041 (Newman, J., concurring-in-part). The legislative history and Supreme Court precedent make clear that the hallmark distinction is the admissibility of "all competent evidence," "to build up a new record," "to start *de novo* in court," "and file testimony bringing in evidence that they could have brought in before [the PTO] but did not bring in before." This evidence, admissible in this civil action, should be governed as the Supreme Court indicated by "equity practice and procedure," i.e., the Federal Rules of Evidence and Civil Procedure.

Since only the presence of new evidence invokes the *de novo* standard of review (otherwise the district court will give the Board fact findings substantial evidence deference, *see Fregeau*, 776 F.2d at 1038), the majority's decision in this case makes the § 145 action virtually indistinguishable from an appeal under § 141. This version of a "civil action" under § 145 is contrary to Congressional intent and to the Supreme Court's rulings. While it is sound policy to encourage full disclosure to administrative tribunals such as the PTO, we are not the body that makes the decision of how best to do this. Congress held numerous hearings over this legislation, considered the concerns over permitting a civil action, and decided to enact the legislation despite these concerns.

Mr. Hyatt did not fail to fulfill an affirmative duty or obligation and he should not be penalized. I believe Congress gave Mr. Hyatt the right to have his own declaration considered as part of the evidence in the § 145 civil action at the district court, and therefore I must dissent from the majority's constriction of this patent applicant's rights.

APPENDIX C

UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF COLUMBIA

Civil Action 03-0901 (HHK)

GILBERT P. HYATT, PLAINTIFF

v.

JON W. DUDAS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE, DEFENDANT

[Filed: Sept. 30, 2005]

MEMORANDUM OPINION

Plaintiff, Gilbert P. Hyatt ("Hyatt"), brings this action against defendant, Jon W. Dudas,[1] in his official capacity as Director of the United States Patent and Trademark Office ("PTO"), seeking review of the decision of the Board of Patent Appeals and Interferences ("Board") to affirm the rejection of 79 of the 117 claims in Hyatt's patent application. Before the court are the

---

[1] Jon Dudas became the Director of the United States Patent and Trademark Office in 2004. When Hyatt initially filed his complaint on April 16, 2003, James Rogan held this position. Pursuant to FED. R. CIV. P. 25(d)(1), the court has substituted Dudas for Rogan as the defendant in this lawsuit.

parties' cross-motions for summary judgment [## 23, 24]. Upon consideration of the motions, the respective oppositions thereto, and the record of this case, the court concludes that the PTO's motion for summary judgment must be granted, and Hyatt's partial motion for summary judgment must be denied as moot.

I. BACKGROUND

A. Legal Background

1. Patent Applications

An inventor seeking to obtain a patent must file a specification of the purported invention with the PTO. 37 C.F.R. § 1.51 (b)(1). A specification must include, inter alia, both a written description of the invention and an enablement for a claimed invention which explains the "manner and process of making and using [the invention], in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains . . . to make and use the same. . . . " 35 U.S.C. § 112 para. 1; *see also* 37 C.F.R. § 1.71(a).

To fulfill the written description requirement, a patent applicant must "convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession *of the invention*." *Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555, 1563-64 (Fed. Cir. 1991). That is, a description need not describe exactly what that applicant claims as her invention, but it must convey to one with "ordinary skill in the art" that the applicant invented what is claimed. *See Union Oil Co. of Cal. v. ARCO*, 208 F.3d 989, 997 (Fed. Cir. 2000). A disclosure may meet this burden by providing either "express" or "inherent" support for a claimed limitation.

See Tronzo v. Biomet, Inc., 156 F.3d 1154, 1159 (Fed. Cir. 1998). In order for a disclosure to be inherent, the "missing descriptive matter must necessarily be present in the . . . application's specification such that one skilled in the art would recognize such a disclosure." *Id.*

To fulfill the enablement requirement, "a patent application must adequately disclose the claimed invention so as to enable a person skilled in the art to practice the invention at the time the application was filed without undue experimentation." *In re Swartz*, 232 F.3d 862, 863 (Fed. Cir. 2000) (internal citation omitted). "[A] 'reasonable' amount of routine experimentation," is allowed but "such experimentation must not be 'undue.'" *Enzo Biochem, Inc. v. Calgene, Inc.*, 188 F.3d 1362, 1371 (Fed. Cir. 1999). In addition, "[whether claims are sufficiently enabled by a disclosure in a specification is determined as of the date that the patent application was first filed." *Id.*

At the end of the written description and enablement, a proper specification should conclude with a list of "claims," which identify the specific innovations, components or sub-parts of invention, the applicant regards as hers. 35 U.S.C. § 112 para 2. A claim is a single sentence description, usually divided into several paragraphs, of what an applicant believes to be her invention, setting the boundaries of the invention the applicant wishes the PTO to examine. Specifically, a single claim can be composed of multiple elements and/or limitations. Elements are the previously known physical components that make up the claimed invention. Limitations, on the other hand, usually describe the claim's restrictions, the interaction between or features of the claim's elements. An application may contain several

claims, and each claim usually contains several limitations. In addition, several claims in a single application may share some of the same limitations. As a result, the PTO may reject several claims at once by rejecting a single, shared limitation.

2. Patent Process and Review

After an inventor files her application, which typically includes a specification, drawings, and sets of claims, to the PTO, the PTO submits the application to an Examiner with the necessary technical competence. *In re Berg*, 320 F.3d 1310, 1315 (Fed. Cir. 2003). After examining the application, the Examiner sends the applicant an "Office action" which may grant or reject the claims. 37 C.F.R § 1.104(a)(2). The applicant may respond by submitting, in writing, a reply that "distinctly and specifically points out the supposed errors in the examiner's action and must reply to every ground of objection and rejection in the prior Office action." *Id.* § 1.111(b). "A general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references does not comply with the requirements of this section." *Id.* If and when the Examiner and applicant finally cannot agree on the disposition of certain claims, the Examiner issues a Final Office Action. *Id.* § 1.113. The applicant then may appeal to the Board, made up of a panel of three administrative patent judges ("APJs"), which will either sustain or reverse the Examiner's rejections. 35 U.S.C. § 134(a). If the Board sustains the Examiner's rejections, the applicant may appeal to the Federal Circuit under 35 U.S.C. § 141, or she may bring a civil action to overturn the Board's decision in this court under 35 U.S.C. § 145.

B. Factual Background

Hyatt is an electrical engineer who holds various computer hardware and software patents. The application at issue is U.S. Patent Application Serial No. 08/471,702 ("'702 Application" or "'702"), entitled "Improved Memory Architecture Having A Multiple Buffer Output Arrangement," which relates to a computerized display system for processing images. R3, 1584.

On June 6, 1995, Hyatt filed the '702 Application, which included a 238-page specification, 40 pages of drawings, and 15 claimed inventions. R1-347. After several amendments, Hyatt presented 117 claims for examination. Hyatt's specification indicates that the '702 application is part of a continuation of ancestor patents dating back to 1984. R4. The specification lists certain computer components, including a graphics processor, a register interface, a buffer memory, and a post-processor. The specification describes certain techniques, such as spatial filtering for anti-aliasing, and some software programs. *See* R1599-1600.

The Examiner rejected all 117 claims on various grounds. *See* R638-63. The Board affirmed the Examiner's rejections of 79 of Hyatt's claims[2] and overturned other rejections, which are not part of the present action. *See* R1583-1640. The Board affirmed the rejection of each of the 79 claims for lack of written description and/or lack of enablement. R1639. On April 16, 2003, Hyatt filed a complaint in this court pursuant to 35 U.S.C. § 145.

---

[2] The Board upheld the rejection of claims 1-14, 17, 18, 20, 34, 36, 42-45, 81, 85, 98, 106-114, 116, 119-134, 136, 141, 143, 145-48, and 153-72 for lack of written description and lack of enablement. R1639.

II. ANALYSIS

A. Procedural issues

The PTO brings a motion for summary judgment, and Hyatt brings a motion for partial summary judgment, under FED. R. CIV. P. 56.[3] The parties, however, dispute several threshold issues of law which this court must resolve before turning to the merits of the motions. in this case. Specifically, the court must determine: (1) the deference, if any, owed to the decision of the Board in a district court review under Section 145; (2) the value of inventor testimony or declarations as evidence; and (3) the application of the administrative exhaustion requirement to certain arguments in this case. The court examines each in turn.

1. Standard of Review—Section 145

The parties disagree over the court's standard of review of the Board's decision to reject Hyatt's patent application. The PTO argues that in a case under 35 U.S.C. § 145, all of the Board's fact-findings are entitled to "substantial evidence" deference, whether or not the patent applicant introduces new evidence as Section 145 allows her to do. Hyatt, on the other hand, contends that the Board's fact-findings are reviewed *de novo* if additional evidence is submitted that rebuts those findings. Hyatt is correct.

---

[3] Under FED. R. CIV. P. 56, summary judgment shall be granted if the pleadings, depositions, answers to interrogatories, admissions on file and affidavits show that there is no genuine issue of material fact in dispute and that the moving party is entitled to judgment as a matter of law. Material facts are those "that might affect the outcome of the suit under the governing law." *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 248 (1986).

Section 145 provides that the district court "may adjudge that such applicant is entitled to receive a patent for an invention, as specified in any of his claims involved in the decision of the [Board]." 35 U.S.C. § 145. The Federal Circuit recognized that Section 145 is, in essence, a type of review of administrative action, and therefore the district court must employ a "standard of review for error in [an] agency decision." *Fregeau v. Mossinghoff*, 776 F.2d 1034, 1038 (Fed. Cir. 1985). As a result, a district court normally applies the deferential "substantial evidence" standard to the Board's fact-findings. *Mazzari v. Rogan*, 323 F.3d 1000, 1004-05 (Fed. Cir. 2003) (citing *Dickinson v. Zurko*, 527 U.S. 150 (1999)) (holding that the Administrative Procedure Act, 5 U.S.C. § 706, applies to a court's review of PTO decisions). However, section 145 is not merely a form of administrative review. The statute allows the parties to submit new evidence to be considered by the court in addition to the administrative record before the Examiner and the Board. *See Fregeau*, 776 F.2d at 1037 ("The proceeding [under Section 145], however, is not simply an appeal since the parties are entitled to submit additional evidence."); *Mazzari*, 323 F.3d at 1004 (holding that section 145 "affords the applicant an opportunity to present additional evidence or argue the previous evidence afresh, either by simply relying upon the record below or by reintroducing the same evidence through alternative means such as live testimony"). If new evidence is submitted, "the district court takes on the role of fact-finder and may need to make factual findings." *Id.* Proceedings under Section 145 have therefore been described as "a hybrid of an appeal and a trial de novo." *Winner Int'l Royalty Corp. v. Wang*, 202 F.3d 1340, 1345 (Fed. Cir. 2000) (citing *Estee Lauder Inc. v.*

L'Oreal, S.A., 129 F.3d 588, 592 (Fed. Cir. 1997)). This is because the district court "applies the 'substantial evidence' standard of review to findings of fact made by the board," but it makes "de novo factual findings" if the parties present additional conflicting evidence. *Mazzari*, 323 F.3d at 1005. Therefore, the court reviews the Board's fact-findings *de novo* to the extent that Hyatt presents new evidence that challenges particular findings; otherwise, when no such evidence is presented, the court employs a deferential "substantial evidence" standard.

2. Admissibility of Hyatt's Declaration

Hyatt presents a declaration which refutes the Board's various written description rejections. *See generally* R832. Such a declaration would entitle Hyatt to *de novo* review of every fact-finding of the Board he challenged. *Mazzari*, 323 F.3d at 1005. However, the PTO argues that despite Hyatt's apparent entitlement to submit new evidence under Section 145, the court should not consider Hyatt's declaration—causing the Board's fact-findings to be reviewed under a deferential standard—for two reasons. First, the PTO argues that the declaration of a patent applicant in his own case is not entitled to any weight. Second, the PTO contends that Hyatt's declaration should not be considered because he does not explain his failure to submit the declaration in previous proceedings before the Board. The court considers both arguments in turn and ultimately concludes that it cannot consider Hyatt's declaration.

a. Validity of Inventor Testimony

The PTO argues that the court should not consider Hyatt's declaration because "the bald declaration of an inventor is insufficient to overcome the Board's findings." Def.'s Reply to Pl.'s Opp'n to Def.'s Mot. for Summ. J. ("Def.'s Reply") at 11 (citing *Bell & Howell Document Mgmt. Prods. Co. v. Altek Sys.*, 132 F.3d 701, 706 (Fed. Cir. 1997); *Rotan Barrier, Inc. v. Stanley Works*, 79 F.3d 1112, 1126 (Fed. Cir. 1996)). The PTO is incorrect because it mis-reads the law.

A court may not consider an inventor's declaration in disputes involving claim construction, which by definition only takes place *after* a patent has been granted. *See Bell & Howell*, 132 F.3d at 706 (noting that, in claim construction, after-the-fact inventor declarations must be disregarded because "the claims, specification, and file history, rather than extrinsic evidence, constitute the public record of the patentee's claim, a record on which the public is entitled to rely") (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996)); *Rotan Barrier*, 79 F.3d at 1125-26 (disregarding inventor declaration in resolving dispute over claim construction in infringement case). By contrast, it is well-established that *before* a patent has been granted, an inventor's testimony may be used to determine whether claims meet the written description requirement. *See Solomon v. Kimberly-Clark Corp.*, 216 F.3d 1372, 1378 (Fed. Cir. 2000) ("[I]n the more fluid environment of patent examination, an inventor's statements are relevant to determining compliance with the statute."); *see also id.* ("It is not inappropriate for the PTO *or a reviewing tribunal* to consider such evidence extrinsic to the patent application in light of the goals of

the examination process and the fact that pending claims can be freely amended to comport with those goals.") (emphasis added) (citing *In re Zletz*, 893 F.2d 319, 321-22 (Fed. Cir. 1989)). The court, therefore, will not refuse to consider Hyatt's declaration simply because it is his own self-serving testimony.

b. Failure to Submit Declaration in Previous Proceedings

The PTO argues that the court should not consider Hyatt's declaration because he failed to present it in the proceedings before the Examiner and the Board. The merits of this argument in turn rests on the validity rests of two other assertions: first, that there are limitations to a party's entitlement to submit new evidence under Section 145 and, second, that under these limitations, Hyatt is not entitled to submit his declaration. The court agrees with the PTO on both counts.

First, while Hyatt argues that there are no restrictions to submitting new evidence under Section 145, courts in the District of Columbia have established a doctrine limiting this entitlement. The courts in such actions refuse to admit evidence submitted to support "new" arguments—that is, those not raised before the Examiner or the Board. *DeSeversky v. Brenner*, 424 F.2d 857, 858 (D.C. Cir. 1970) (stating that though an applicant may present new evidence, she is "precluded from presenting new issues, at least in the absence of some reason of justice put forward for failure to present the issue to the Patent Office"); *see also In re Watts*, 354 F.3d 1362, 1367 (Fed. Cir. 2004) ("[I]t is important that the applicant challenging a decision not be permitted to raise arguments on appeal that were not presented to

the Board."). In addition, courts have excluded new evidence in Section 145 actions if it was "available to the parties, but was withheld from the Patent Office as a result of fraud, bad faith, or gross negligence." *Monsanto Co. v. Kamp*, 269 F. Supp. 818, 822 (D.D.C. 1967); *accord Cal. Research Corp. v. Ladd*, 356 F.2d 813, 820-21 n.18 (D.C. Cir. 1966) ("Although each side 'may strengthen its case with additional material' the plaintiff may not submit for the first time evidence which he was negligent in failing to submit to the Patent Office. . . . "); *Holloway v. Quigg*, 9 U.S.P.Q. 2d 1751, 1752 (D.D.C. 1988) ("[E]vidence has been excluded if it was available to the plaintiff during the PTO proceeding but was either intentionally or negligently withheld."). Both doctrines support the "general policy of encouraging full disclosure to administrative tribunals." *Ladd*, 356 F.2d at 820-21 n.18 ("In short, the District Court proceeding may not be conducted in disregard of the general policy of encouraging full disclosure to administrative tribunals . . . ."). Consequently, these doctrines limit Hyatt's entitlement to submit new evidence under Section 145.[4]

---

[4] The Federal Circuit, which provides the controlling law in this case, has neither accepted nor repudiated cases, such as *DeSeversky* or *Kamp*, limiting the entitlement to submit new evidence in Section 145 actions. Nevertheless, the PTO has adopted these guidelines, citing explicitly to D.C. Circuit and D.C. district court cases:

> In an action under 35 U.S.C. [§] 145, the plaintiff may introduce evidence not previously presented to the U.S. Patent and Trademark Office. However, plaintiff will be precluded from presenting new issues, at least in the absence of some reason of justice put forward for failure to present the issue to the U.S. Patent and Trademark Office. [Citations to *DeSeversky*, 424 F.2d at 858; *MacKay*, 641 F. Supp. at 570]. Furthermore, new evidence is not admissible in district court where it was available to the parties but was withheld from the U.S. Patent and Trademark Office as a result of fraud, bad faith, or gross

Second, the PTO argues that under these doctrines, Hyatt should be barred from submitting his declaration. Specifically, the PTO contends that Hyatt is at least negligent in failing to provide the declaration in earlier proceedings. Def.'s Mot. for Summ. J. ("Def.'s Mot.") at 37. Hyatt, on the other hand, justifies submitting his declaration because he had no opportunity to respond to the Board's new grounds for upholding the Examiner's written description rejections. Pl.'s Opp'n to Def.'s Mot. for Summ. J. ("Pl.'s Opp'n") at 41-44. The PTO's position has merit and Hyatt's does not.

A patent applicant must have the opportunity to respond to new grounds for claim rejections put forth by the Board. *See In re Waymouth*, 486 F.2d 1058, 1061 (CCPA 1973) ("To attempt to deny appellants an opportunity to provide a different and appropriate response to the board's rejection . . . does not satisfy the administrative due process established by Rule 196(b) of the Patent Office."). If the Board provides a "wholly different basis" for sustaining a rejection, the rejection is new. *Id.* at 1060-61 (finding that the Board had sustained a rejection on a "wholly different basis" and had conceded as much by admitting that its comments "were merely 'an additional reason' for affirming the examiner's rejection"). However, a rejection is not based on new grounds if "appellants have had fair opportunity to react to the thrust of the rejection." *In re Kronig*, 539 F.2d 1300, 1302 (CCPA 1976); *accord id.* at 1303 (finding that an applicant had fair opportunity to challenge a

---

negligence. [Citations to *DeSeversky*, 424 F.2d at 858 n.5; *Ladd*, 356 F.2d at 821 n.18; *MacKay*, 641 F. Supp. at 570; *Kamp*, 269 F. Supp. at 822; *Killian v. Watson*, 121 U.S.P.Q. 507, 507 (D.D.C. 1958)].

MANUAL ON PATENT EXAMINING PROC. § 1216.02.

rejection because "[t]he basic thrust of the rejection at the examiner and board level was the same").

Hyatt faults the Board for not directly quoting the Examiner's written description rejections. *See, e.g.*, Pl.'s Opp'n at 18 ("The PTO's failure to quote the precise language used by the Examiner is telling."). By this logic, the Board could only avoid raising a new grounds of rejection by using the exact words the Examiner used to sustain a written description rejection. Though a patent applicant is entitled to respond to the "thrust of the rejection," *Kronig*, 539 F.2d at 1302, not every new turn of phrase by the Board entitles a patent applicant to an additional response. A rejection is not new simply because the Board fails to use the exact words of the Examiner in sustaining a rejection or if the Board simply elaborates on the Examiner's rationale. *In re Oetiker*, 977 F.2d 1443, 1445-46 (Fed. Cir. 1992).

After closely comparing the Examiner's rejections with the Board's rejections,[5] the court concludes that the "thrust" of the Board's written description rejections

---

[5] *Compare* R642-43 (Examiner's rejection of written description of vector processor) *with* R1605-07 (Board's sustaining same written description rejection); *compare* R643-44 *with* R1608-09 (processor responsive to an accessed block of video pixel image information); *compare* R647 *with* R1613-14 (rejections of block processor generating two dimensional processed image information); *compare* R651 *with* R1615-16 (rejections of block boundary smoothing); *compare* R652 *with* R1617 (written description rejections video image date compression system); *compare* R653 *with* R1617-19 (written description rejections of weighting processor is a quantization weighting processor); *compare* R654 *with* R1620-21 (written description rejections of generating data compressed video information).

are the same as those of the Examiner.[6] With regard to each limitation rejected for lack of written description, the Examiner identified the specific limitation using a short phrase,[7] and explained simply that that particular feature was not described in Hyatt's specification or a parent application (No. 06/662,211) cited by Hyatt.[8]

---

[6] There is one exception. For claims 153-172, "making a product in response to image information," the Examiner issued a rejection on the grounds that it was not described in Hyatt's specification. R655. Upon review, the Board went beyond simply elaborating on the Examiner's rejection or explaining its own attempts to find the "making a product" feature in the specification. It found that the limitation produced "signals" and that, as a matter of law, "signals" were not "products." R1621-1624. However, the Board made this determination in response to Hyatt's argument in his appeal brief that a "product" could be a "signal." R836-37. It is therefore not a "new" grounds for rejection because Hyatt had and took the opportunity to argue his position. In addition, in his opposition to the PTO's motion for summary judgment, Hyatt does not contend that the Board provided new grounds for rejection for these claims. Pl.'s Opp'n at 39-40.

[7] R642-43 ("vector processor responsive to an accessed block of video pixel image information and to vector information"); R643-44 ("processor responsive to an accessed block of video pixel image information"); R647 ("block processor responsive to an accessed block of pixel image information and to vector information"); R651 ("block boundary smoothing"); R652 ("video image data compression system"); R653 ("weighting processor is a quantization weighting processor"); R654 ("generating data compressed video information").

[8] Because the Examiner's rejections were terse—for these limitations, no more than a paragraph each—Hyatt claims that the Examiner did not meet his *prima facie* burden. The controlling law, however, indicates otherwise. If an Examiner simply cannot find a claimed limitation described in a specification, he is not required to say more than that to reject a claim for lack of written description. *In re Alton*, 76 F.3d 1168, 1175 (Fed. Cir. 1996) ("If the applicant claims embodiments of the invention that are completely outside the scope of the specification, then the examiner or Board need only establish this fact to make

The Board reversed 38 of the Examiner's rejections based on lack of written description. R1639 (reversing Examiner's written description rejection of limitations common to claims 19, 22-25, 35, 37, 49-52, 82-84, 95-97, 99-105, 115, 117, 118, 135, 137-140, 142, 144, and 149-152 because the particular features were described in the specification). However, the Board sustained the remaining rejections using the same rationale—the claimed features were simply not described in Hyatt's specification.[9]

Mostly, the Board's rejections were longer than the Examiner's. The majority of the Examiner's written description rejections were one paragraph long, *see, e.g.*, R642-43, while the Board at times took several pages to uphold the same rejections. *See, e.g.*, R1605-07. With some rejected written descriptions, the Board did not expand much on the Examiner's one paragraph rejection, using only slightly different words to say that it could not find the claimed limitations in Hyatt's specification. *See, e.g.*, R1608, R1609, R1617. With other rejections, the Board described its attempts to find certain

---

out a prima facie case.") (citing *In re Wertheim*, 541 F.2d 257, 263-64 (CCPA 1976)).

[9] *See* R1607 ("[W]e find no written description for a processor coupled to and performing the 'generating' function 'in response to' the vector information as well as 'in response to' image information from the image memory"); R1613 (citing R1607 and sustaining similar written description rejection); R1608 ("[W]e find no disclosure of the processor 'generating data compressed video image information,' as claimed"); R1609, R1617, R1620 (citing R1608 and sustaining similar written description rejections); R1616 ("We find nothing in the specification that describes 'smoothing' or 'block boundary smoothing.'"); R1619 ("[W]e fail to see how the program GRAPH.ASC, or the other programs LD.ASC or FTR.ASC, provide written description support for the limitation at issue.").

limitations in Hyatt's specification—for instance, by searching the specification for individual words or features in the limitation—and then noting that it still could not find written description support for the claimed limitation as a whole.[10] In short, the Board showed that it made an independent and thorough assessment of Hyatt's specification before upholding the Examiner's written description rejections for certain limitations. Furthermore, Hyatt already had a chance to respond to the "thrust" of the Examiner's written description rejections before his appeal to the board. As a result, the court concludes that Hyatt's declaration, which addresses many of the written description rejections, could have been presented earlier, perhaps during Hyatt's proceedings before the Examiner, but certainly by the time his patent application was considered by the Board.[11]

---

[10] *See, e.g.*, R1605-07 (observing that, with regard to the "vector processor generating two dimensional vector processed image information" limitation, Hyatt's specification disclosed a processor, coupled to the accessing circuit and to the vector generator, but not one functioning "in response to" vector information and image information from the image memory); R1615 (noting that, for the "block boundary smoothing" limitation, the Board knew what a "block boundary" was, and that a software program in Hyatt's specification included the word "smoothing," but that neither "smoothing" nor the combined phrase "block boundary smoothing" was otherwise described in the specification).

[11] Hyatt also argues that the Board improperly refused to consider his request for rehearing; however, if a patent applicant fails to present an argument in her appeal to the Board that could have been presented earlier, she may not present it in her request for rehearing. *Cooper v. Goldfarb*, 154 F.3d 1321, 1331 (Fed. Cir. 1998) ("A party cannot wait until after the Board has rendered an adverse decision and then present new arguments in a request for reconsideration."). In Hyatt's request for rehearing, he presented 50 pages of new argument, which at last included detailed explanations addressing the Board's reasons for rejecting his claims. R1648-98. In addition, he submitted almost 100

The court, therefore, excludes from its consideration Hyatt's declaration because: (1) the "thrust" of the Board's written description rejections were the same as the Examiner's; (2) Hyatt had the opportunity to present to the Board, if not the Examiner, his declaration indicating that one skilled in the art would recognize his claimed limitations as described in the specification for the '702 application; (3) Hyatt has no other explanation (aside from the "new grounds" argument) to address why he failed to offer his declaration during the proceedings before the Board; and (4) Hyatt's failure to explain why he didn't submit his declaration earlier is negligent, and the district court need not consider evidence negligently submitted after the end of administrative proceedings. *Killian*, 121 U.S.P.Q. at 509 ("Where a plaintiff in an action under Section 145 . . . offers no explanation for his failure to submit to the Patent Office, during the prosecution of his application for patent, evidence purporting to show that he invented the claimed subject matter prior to the effective filing date of the application on which a patent said to anticipate was granted, such evidence is not properly admissible."). As a result, the court finds that Hyatt's declaration is not admissible.

Because Hyatt offers no other additional evidence aside from his declaration, the court reviews all of the Board's fact-findings using the more deferential "sub-

---

pages of new photographs, drawings, and reference material that he also failed to present earlier to the Board. R1699-1793. The Board denied Hyatt's request for rehearing because his "extensive new arguments" could have been presented earlier. R1807. Upon review of Hyatt's request for rehearing, the court agrees. Hyatt has not offered any justifiable excuse for not submitting these arguments to the Board earlier. As such, Hyatt's request for rehearing was properly denied.

stantial evidence" standard. *Mazzari*, 323 F.3d at 1004-05. Under this standard, the court "asks whether a reasonable fact-finder could have arrived at the agency's decision." *In re Gartside*, 203 F.3d 1305, 1312 (Fed. Cir. 2000). The Board's findings are not rendered unsupported by substantial evidence simply because it is possible to draw "two inconsistent conclusions." *Velander v. Garner*, 348 F.3d. 1359, 1374 (Fed. Cir. 2003) (quoting *Consolo v. Fed. Mar. Comm'n*, 383 U.S. 607, 620 (1966)). Therefore, "if the evidence of record will support several reasonable but contradictory conclusions, we will not find the Board's decision unsupported by substantial evidence because the Board chose one finding over another plausible alternative." *Id.* (citing *In re Jolley*, 308 F.3d 1317, 1320 (Fed. Cir. 2002)).

B. The Board's Affirmation of the Examiner's Written Description Rejections

Before the court for review are ten written descriptions, relating to seventy-nine claims, that were rejected by both the Examiner and the Board. The rejections can be grouped into five categories. The court considers each category in turn.

1. Vector Processor and Block Processor

The Examiner rejected twenty-nine claims based on their common "vector processor" and "block processor" subparagraphs.[12] R642-43, 647. The Board upheld the

---

[12] An exemplary "vector processor" subparagraph for claims 1, 2, 5, 9, 10, 12, 20, 81, 85, 98, 110-114, 119, 120, 123, 127, 128, 130, 136, 153, 157, and 161 is set forth in claim 1:

> a two dimensional vector processor coupled to the accessing circuit and coupled to the vector generator, the two dimensional vector pro-

rejections of the vector and block processor limitations because Hyatt did not adequately describe the processors specified in his claims.[13] Specifically, the Board found that both limitations "require[] that the processor perform the function of 'generating two dimensional processed image information in response to . . . video pixel information . . . and in response to the two dimensional vector information generated by the vector generator.'" R1606. It determined that this language "implies that the 'generating' function operates on two kinds of input data: a pixel information from memory and vector information." *Id.* It found that "the specification describes graphics vectors being generated . . . into image memory . . . , not being generated and used by a processor together with accessed pixel data read out from the block image memory, which would require bypassing the block memory." R1606-07. In other

---

cessor generating two dimensional vector processed image information in response to the accessed blocks of video pixel image information accessed by the accessing circuit and in response to the two dimensional vector information generated by the vector generator;

R1009-10. An exemplary "block processor" subparagraph for claims 17, 18, 133, and 134 is set forth in claim 17:

a two dimensional block processor coupled to the frame buffer accessing circuit and coupled to the vector generator, the two dimensional block processor generating two dimensional processed image information in response to the blocks of pixel image information accessed by the frame buffer accessing circuit and in response to the two dimensional vector information generated by the vector generator;

R1026-27.

[13] The Board noted the similarity of the vector processor claims and the block processor claims and used the same reasoning in rejecting both limitations. R1607, 1613-14; *see also* R642.

words, "the disclosed processor only controls the vector generator, it does not receive data from it or operate 'in response to' it." R1607. The Board therefore concluded that "[s]ince the vector information is stored into the block memory, we find no written description for a processor coupled to and performing the 'generating' function 'in response to' the vector information as well as 'in response to' image information from the image memory." *Id.* In essence, the Board found that while Hyatt did describe a processor, he did not describe "one that receives or responds to the two particular kinds of information—video pixel information and vector information—specified in his claim." Def.'s Reply at 16-17.

In his appeal to the Board, Hyatt presented one piece of evidence, Table 1, which identifies twenty-four words found in his claims and lists the number of times each one appears in his specification and the page number on which each is located. R832. It offers no explanation or response to the Examiner's rejections. Both the Examiner and the Board found Table 1 unhelpful and unpersuasive, for "merely pointing to isolated words scattered throughout the specification does not describe the invention claimed as a combination of elements, functions, and interconnections any more than a dictionary provides written description support for a book where words are used in combination to provide a certain meaning." R1595. With respect to the vector and block processor limitations, the Board stated that Hyatt "merely points to Table 1 . . . for occurrences of words in the limitation and does not show where the specification describes the claimed structure or process." R1607. Notably, Hyatt did "not point to a written description of a processor performing a generating function responsive to the two specific types of information." *Id.*

It is well established that "the written description must include all of the limitations of the [claim], or the applicant must show that any absent text is necessarily comprehended in the description provided." *Hyatt v. Boone*, 146 F.3d 1348, 1354 (Fed. Cir. 1998). Because a reasonable fact-finder could have arrived at the Board's conclusion that Hyatt did not "include all of the limitations" of this claim because he did not describe a processor that responds to both video pixel information and vector information, the court finds that the Board's decision to uphold the vector and block processor rejections was supported by substantial evidence.[14]

2. Processor Generating Data Compressed Video

The Board upheld the Examiner's rejection of fifty-two claims based on their common "data compression" subparagraphs because Hyatt again did not describe his claimed inventions in his specification.[15] The Board

---

[14] In his opposition, Hyatt relies on his declaration to support his contention that "the processor recited in the claims is supported by the disclosure." Pl.'s Opp'n at 19. However, the court has already determined that it will not consider Hyatt's declaration in deciding this motion on this or any other claim.

[15] An exemplary "data compression" subparagraph for claims 3, 4, 11, 121, 122, and 129 is set forth in claim 3:

> a processor coupled to the accessing circuit and generating data compressed video image information in response to accessed blocks of video pixel image information generated by the accessing circuit;

R1012. An exemplary "data compression" subparagraph for claims 1, 85, 110-112, 119, and 157 is set forth in claim 1:

> a two dimensional spatial processor coupled to the buffer memory and generating data compressed video image information in response to the buffered blocks of video pixel information stored in said buffer

found that "[w]hile a processor is coupled to the accessing circuit comprising the block memory of figures 6E to 6N and the raster scan address generator of figures 6O and 6P, we find no disclosure of the processor 'generating data compressed video image information,' as claimed." R1608. It explained that "[t]he only compression mentioned in the specification is concerned with compression and decompression offline or online prior to loading into the image memory or in connection with an emulation program, not after it is stored in the block image memory." *Id.* In other words, Hyatt successfully describes data compression, but he fails to describe data compression of *video image information* because he only describes data compression that takes place *before*

---

memory and in response to the buffered two dimensional vector processed image information stored in said buffer memory;

R1010. An exemplary "data compression" subparagraph for claims 6-9, 13, 14, 124-127, 131, and 132 is set forth in claim 6:

A two dimensional frequency domain transform processor coupled to the accessing circuit and generating data compressed video image information in response to the accessed blocks of video frequency domain information accessed by the accessing circuit;

R1016. Claim 112's "data compression" subparagraph is as follows:

wherein the memory system is a video image data compression system;

R1073. An exemplary "data compression" subparagraph for claims 2-14, 113, 114, and 120-132 is set forth in claim 2:

a two dimensional vector processor coupled to the accessing circuit and coupled to the vector generator, the two dimensional vector processor generating data compressed video image information in response to the accessed blocks of video pixel image information accessed by the accessing circuit and in response to the two dimensional vector information generated by the vector generator;

R1011.

the video image information is formed; he never describes the data compression as taking place *after* the image data has been stored in the memory. R1608, 1609, 1611, 1617, 1620. Hyatt's appeal to the Board relied upon Table 1, which the Board again found unpersuasive. Because a reasonable fact-finder could conclude, as the Board did, that Hyatt failed to describe data compression of video image information, the Board's rejections of these claims are affirmed.

3. Block Boundary Smoothing

The Board upheld the Examiner's rejections of twenty claims based on their common block boundary smoothing" paragraph because it found "nothing in the specification that describes 'smoothing' or 'block boundary smoothing.'"[16] R1616. In his appeal to the Board, Hyatt directed them to Table 1, which lists the number of times and the page numbers on which the words "block " "boundary" and "smoothing" occur. R832. The Board considered this but again found it unhelpful, noting that the table "does not show written description for the limitation of 'block boundary smoothing'. . . . " *Id.* It explained that while the word "smoothing" appears in Hyatt's specification in a particular program, it refers only to "'SMOOTHING PRINTOUTS' without explanation." *Id.* Furthermore, the program which contains the word "smoothing" involves conventional computer memory, "it does not use a memory having blocks or block

---

[16] An exemplary "block boundary smoothing" paragraph for claims 34, 36, 42-45, 106-109, 141, 143, 145-148, and 169-172 is set forth in claim 34: "a block boundary smoothing processor generating block boundary smoothing information to smooth the pixel image information at boundaries between blocks of pixel image information; . . . . " R1037.

boundaries and so is not relevant to the issue of block boundary smoothing." *Id.* It was reasonable for the Board to determine that "block boundary smoothing" was not adequately described because the specification only mentions the word "smoothing" one time, and even in that lone occurrence, it is not used in the context of "block boundary smoothing." R234. The Board's rejections are affirmed.

4. Quantization

The Board upheld the Examiner's rejection of claim 116 for lack of written description support for the limitation that "the weighting processor is a quantization weighting processor. . . . "[17] R1617, 1619. Based on Table 1, which Hyatt presented in response to the Examiner's determination that a quantization weighting processor was not described in the specification, R653, the Board found that quantization did exist somewhere in the system, but its mere existence "was not persuasive or written description support for the particular claim limitation at issue." R1619. The Board explained that "[t]he claim limitation is directed to quantization *after* the pixel image information is accessed (read) from block memory." *Id.* (emphasis added). Two of the programs in Hyatt's specification that involve quantization

---

[17] The quantization subparagraph of claim 116 states:

> wherein the weighting processor is a quantization weighting processor generating the weighted frequency domain image information as quantize weighted frequency domain image information by weighting the frequency domain image information generated by the frequency domain processor in response to the accessed weight information generated by the weight memory accessing circuit.

R1074-75.

deal with loading a file to the image memory and pre-filtering, both of which occur *before* the image information is accessed from the memory. *Id.* They therefore "do not appear relevant to the quantization written description at issue." *Id.* A third program, GRAPH.ASC (R216-18), "simply accesses (reads) pixel information out of memory . . . and does not perform any frequency domain processing, does not control the weight memory accessing circuit, and does not perform any quantization weighting of weighted frequency domain information." *Id.* In short, "Hyatt claims a post- processor data manipulation when his description is limited to data manipulation that is pre-processor." Def.'s Reply at 31. The court once again finds that a reasonable fact-finder could have reached the same result as the Board did, and the rejection of this claim is sustained.

5. Making a Product in Response to the Output Image Information

Finally, the Board upheld the Examiner's rejection of claims 153-172 based on the following exemplary subparagraph, set forth in claim 153: "the act of making a product in response to the output image information." R1084. Both the Examiner and the Board found that there was no written description support for "making a product." R1621; *see also* R655.

In his appeal to the Board, Hyatt attempted to argue that the term "products" necessarily includes "machines," "manufactures" and "signals," and because he discloses a "signal," his written description for "making a product" is sufficient. R837. The Board expressly addressed and rejected this argument because in the limitation, which states "making a product in response to

. . . image information," the "'image information' is the signal and the 'product' must [therefore] be something else, which is not disclosed." R1621. It went on to explain that the Patent Act only covers three product classes: machines, manufactures, and compositions of matter. An electrical signal is a form of energy; it therefore does not fall within any of the three product classes and cannot be claimed. R1622; 35 U.S.C. § 101. A reasonable fact-finder could determine that a "signal" is not a "product" and conclude that Hyatt's "making a product" claim therefore lacks an adequate description. As such, the Board had substantial evidence to reject these claims.

C. Enablement

Hyatt moves for partial summary judgment, arguing that the Board failed to meet its burden of proof in rejecting the claims for lack of enablement. The PTO concedes that its enablement rejections are tied entirely to its written description rejections. *See* Def.'s Mot. at 29. Having already rejected all of Hyatt's claims for lack of written description, the court need not decide Hyatt's motion for it is moot. *See Univ. of Rochester v. G.D. Searle & Co.*, 358 F.3d 916, 929-30 (Fed. Cir. 2004) (holding that upon affirming the district court's decision to reject the written descriptions, "we consider the enablement issue to be moot").

CONCLUSION

For the foregoing reasons, the court grants the PTO's motion for summary judgment and denies Hyatt's motion for partial summary judgment. A separate order accompanies this memorandum opinion.

Henry H. Kennedy, Jr.
United States District Judge

Dated: September 30, 2005

APPENDIX D

The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

BOARD OF PATENT APPEALS
AND INTERFERENCES

No. 2000-2049
Application 08/471,702[1]

EX PARTE GILBERT P. HYATT

[Decided: July 30, 2002]

DECISION ON APPEAL

Before: KRASS, BARRETT, and LALL, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

---

[1] Application for patent filed June 6, 1995, entitled (as amended) "A Data Compression System," which claims the benefit of the priority dates under 35 U.S.C. § 120 of numerous applications, the earliest of which is Application 06/661,649, filed October 17, 1984, now abandoned.

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172, which are all of the pending claims.

We affirm-in-part.

BACKGROUND

The invention relates to an image memory system and a process of operating an image memory system wherein the image information is stored in a two dimensional array of rows and columns of blocks of pixel image information.

Claim 1 is reproduced below.

1. A memory system comprising:

a data decompressed video image-input circuit generating data decompressed video image information;

a two dimensional pixel block image memory storing a two dimensional array of blocks of video pixel image information, the two dimensional array of blocks of video pixel image information arranged in a two dimensional array of rows and columns of blocks of video pixel image information;

an address generator generating write addresses and generating read addresses;

a memory writing circuit coupled to the data decompressed video image input circuit, coupled to the two dimensional pixel block image memory, and coupled to the address generator, the memory writing circuit writing the two dimensional array of blocks of video pixel image information into the two dimen-

sional pixel block image memory in response to the data decompressed video image information generated by the data decompressed video image input circuit and in response to the write addresses generated by the address generator;

an accessing circuit coupled to the two dimensional pixel block image memory and coupled to the address generator, the accessing circuit generating accessed blocks of video pixel image information by accessing the two dimensional array of blocks of video pixel image information from said two dimensional pixel block image memory in response to the read addresses generated by the address generator;

a vector generator generating two dimensional vector information;

a two dimensional vector processor coupled to the accessing circuit and coupled to the vector generator, the two dimensional vector processor generating two dimensional vector processed image information in response to the accessed blocks of video pixel information accessed by the accessing circuit and in response to the two dimensional vector information generated by the vector generator;

a buffer memory coupled to the accessing circuit and coupled to the two dimensional vector processor, the buffer memory storing buffered blocks of video pixel information in response to the accessed blocks of video pixel image information accessed by said accessing circuit, and storing buffered two dimensional vector processed image information in response to the two dimensional vector processed image informa-

tion generated by the two dimensional vector processor; and

a two dimensional spatial processor coupled to the buffer memory and generating data compressed video image information in response to the buffered blocks of video pixel image information stored in said buffer memory and in response to the buffered two dimensional vector processed image information stored in said buffer memory.

THE PRIOR ART

The examiner relies on the following references:

Lelke	4,069,511	January 17, 1978
Hill	4,200,867	April 29, 1980
Lord et al. (Lord)	4,322,750	March 30, 1982

THE REJECTIONS

For reference purposes, pages of the final rejection (Paper No. 21) are referred to as "FR__"; pages of the examiner's answer (Paper No. 34) are referred to as "EA__"; pages of the appeal brief (Paper No. 30) are referred to as "Br __"; and pages of the reply brief (Paper No. 42) are referred to as "RBr__". The rejections are summarized below.

1. Claims 1-14, 110-114[2], and 119-132 stand rejected under 35 U.S.C. § 112, first paragraph, based on a lack of written description and, lack of enablement for the

---

[2] Although the statement of the rejection does not include claims 110-114, since these claims depend on rejected independent claims 1 or 2, the failure to include these claims in the rejection appears to be an oversight.

limitation of "a data decompressed video image input circuit generating data decompressed image information" (EA4-6 ¶¶ 10.2 & 10.3).[3]

2. Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 (all claims) stand rejected under 35 U.S.C. § 112, first paragraph, based on a lack of written description and lack of enablement for simultaneously writing into and accessing (reading) from the block memory (EA6-7 ¶¶ 10.4 & 10.5).

3. Claims 1, 2, 5, 9, 10, 12, 20, 81, 85, 98, 110-114, 119, 120, 123, 127, 128, 130, 136, 153, 157, and 161 stand rejected under 35 U.S.C. § 112, first paragraph, based on a lack of written description and lack of enablement for a vector processor generating two dimensional vector processed image information in response to video pixel information and in response to vector information (EA8-9 ¶¶ 10.6 & 10.7).

4. Claims 3, 4, 11, 121, 122, and 129 stand rejected under 35 U.S.C. § 112, first paragraph, based on a lack of written description and lack of enablement for a processor generating data compressed video image information in response to accessed blocks of video pixel image information (EA9-10 ¶¶ 10.8 & 10.9).

5. Claims 1, 85, 95, 110-112, 119, 157, and 158 stand rejected under 35 U.S.C. § 112, first paragraph, based on a lack of written description and lack of enablement for a spatial processor generating data compressed video image information in response to video pixel infor-

---

[3] In all of the rejections based on 35 U.S.C. § 112, first paragraph, rejections numbered 1-13, the claims are held to lack enablement because they are found to lack written description support.

mation and in response to vector processed image information (EA10-11 ¶¶ 10.10 & 10.11).

6. Claims 6-9, 13, 14, 24, 34, 36, 42, 49, 50, 102, 106, 115-118, 124-127, 131, 132, 139, 141, 143, 145, 149, 150, 165, and 169 stand rejected under 35 U.S.C. § 112, first paragraph, based on a lack of written description and lack of enablement for a frequency domain transform processor generating data compressed video image information or generating frequency domain image information (EA11-12 ¶¶, 10.12 & 10.13).

7. Claims 17, 18, 133, and 134 stand rejected under 35 U.S.C. § 112, first paragraph, based on a lack of written description and lack of enablement for the limitation of a block processor generating two dimensional processed image information in response to pixel image information and in response to vector information (EA12-13 ¶¶ 10.14 & 10.15).

8. Claims 24, 34-37, 42-45, 49-51, 102-109, 115-118, 139-151, and 165-172 stand rejected under 35 U.S.C. § 112, first paragraph, based on a lack of written description and lack of enablement for an input weight circuit generating input weight information (EA13-16 ¶¶ 10.16 & 10.17).

9. Claims[4] 34, 36, 42-45, 106-109, 141, 143, 145-148, and 169-172 stand rejected under 35 U.S.C. § 112, first paragraph, based on a lack of written description and lack of enablement for the claimed block boundary smoothing (EA16-17 ¶¶ 10.18 & 10.19)

---

[4] The statement of the rejection recites claims 141-148. However, claims 142 and 144 depend on claims 35 and 37, respectively, which are not rejected. Accordingly, we have restated claims 141-148 to be claims 141, 143, and 145-148.

10. Claim 112 stands rejected under 35 U.S.C. § 112, first paragraph, based on a lack of written description and lack of enablement for the memory system being a video image data compression system (EA17-18 ¶¶ 10.2 [sic, 10.20] & 10.21).

11. Claim 116 stands rejected under 35 U.S.C. § 112, first paragraph, based on a lack of written description and lack of enablement for the weighting processor being a quantization weighting processor (EA18-19 ¶¶ 10.22 & 10.23).

12. Claims 2-14, 113, 114, and 120-132 stand rejected under 35 U.S.C. § 112, first paragraph, based on a lack of written description and lack of enablement for "generating data compressed video information" (EA19-20 ¶¶ 10.24 & 10.25).

13. Claims 153-172 stand rejected under 35 U.S.C. § 112, first paragraph, based on a lack of written description and lack of enablement for the limitation of "making a product in response to the output image information" (EA20-21 ¶¶ 10.26 & 10.27).

14. Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52 81-85 and 95-172[5] stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over:

---

[5] The statement of the rejection refers to claims 95-162. However, it appears that "162" is an inadvertent mistake and should be "172" so as to include all the pending claims. There is no apparent reason why the claim grouping should end at claim 162 since claims 163-172 also include the limitation of making a product and it appears to be the examiner's intent to reject all the claims of the present application over all the claims in each of the copending applications.

- claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 96-173 of copending Application 08/471,704;
- claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 of copending Application 08/471,712;
- claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 of copending Application 08/471,925;
- claims 17-20, 22-25, 42-45, 49-52, 71-74, 81-85, and 110-162 of copending Application 08/472,062;
- claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 of copending Application 08/479,086;
- claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 of copending Application 08/479,087;
- claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 96-173 of copending Application 08/479,088; and
- claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 90-167 of copending Application 08/483,016.

The examiner states that although the claims are not identical, they are not patentaply distinct and the minor differences are obvious variations of the same claimed invention (EA23-24 ¶ 10.29).

15. Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172[6] stand provisionally rejected for double patenting based on *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968) (so-called *Schneller*-type double patenting) over:

- claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 96-173 of copending Application 08/471,704;
- claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 of copending Application 08/471,712;
- claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 of copending Application 08/471-925;
- claims 17-20, 22-25, 42-45, 49-52, 71-74, 81-85, and 110-162 of copending Application 08/472,062;
- claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 of copending Application 08/479,086;
- claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 of copending Application 08/479,087;
- claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 96-173 of copending Application 08/479, 088; and
- claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 90-167 of copending Application 08/483,016.

---

[6] See footnote 5.

The examiner states that the subject matter of the present claims is fully disclosed in the copending applications, would be covered by any patent granted in the copending applications, that there is no reason why appellant would be prevented from presenting claims corresponding to the present claims in the other copending applications, and therefore a provisional double patenting rejection is proper under *Schneller* (EA24-25 ¶¶ 10.30).

16. Claims 22, 23, 82-84, 95, 99, 137, and 138 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Hill (EA26 ¶¶ 10.32 & 10.33).

17. Claims 19, 25, 96, 100, 101, 135, and 140 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lord, Hill, and Lelke (EA ¶¶ 27-28, 10.35 & 10.36).

OPINION

The written description rejection

Legal standards

The test for written description is summarized in *Purdue Pharma L.P. v. Faulding Inc.*, 230 F.3d 1320, 1323, 56 USPQ 2d 1481, 1483 (Fed. Cir. 2000):

> In order to satisfy the written description requirement, the disclosure as originally filed does not have to provide *in haec verba* support for the claimed subject matter at issue. *See Fujikawa v. Wattanasin*, 93 F.3d 1559, 1570, 39 USPQ 2d 1895, 1904 (Fed. Cir. 1996). Nonetheless, the disclosure "must . . . convey with reasonable clarity to those skilled in the art that . . . [the inventor] was in possession of the invention." *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1563-64, 19 USPQ 2d 1111, 1117 (Fed. Cir. 1991).

> Put another way, one skilled in the art, reading the original disclosure, must "immediately discern the limitation at issue" in the claims. *Waldemar Link GmbH & Co. v. Osteonics Corp.*, 32 F.3d 556, 558, 31 UPSQ 2d 1855, 1857 (Fed. Cir. 1994). That inquiry is a factual one and must be assessed on a case-by-case basis. *See Vas-Cath*, 935 F.2d at 1561, 19 USPQ 2d at 1116 ("Precisely how close the original description must come to comply with the description requirement of § 112 must be determined on a case-by-case basis.").

As further stated in *Lockwood v. American Airlines Inc.*, 107 F.3d 1565, 1572, 41 USPQ 2d 1961, 1968 (Fed. Cir. 1997):

> One shows that one is "in possession" of *the invention* by describing *the invention*, with all of its claimed limitations, not that which makes it obvious. [*Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1563-64, 19 USPQ 2d 1111, 1117 (Fed. Cir. 1991)] ("[T]he applicant must also convey to those skilled in the art that, as of the filing date sought, he or she was in possession *of the invention*. The invention is, for purposes of the 'written description' inquiry, *whatever is now claimed.*") (emphasis in original). One does that by such descriptive means as words, structures, figures, diagrams, formulas, etc., that fully set forth the claimed invention. Although the exact terms need not be used *in haec verba*, *see Eiselstein v. Frank*, 52 F.3d 1035, 1038, 34 USPQ 2d 1467, 1470 (Fed. Cir. 1995) ("[T]he prior application need not describe the claimed subject matter in exactly the same terms as used in the claims . . . "), the specification must contain an equivalent description of the

claimed subject matter. A description which renders obvious the invention for which an earlier filing date is sought is not sufficient.

Response to appellant's general comments

This section responds to appellant's general comments on the written description rejection. Basically, we are not persuaded by general arguments about what the examiner should have done, about perceived inconsistencies in the rejection, and boilerplate statements of the law. What is important is the merits of the particular written description rejections, as discussed in the following sections. Appellant's comments regarding specific limitations are discussed in connection with those limitations.

Appellant argues that the § 112 rejections are non-critical "technical" rejections and are "clearly improper" (Br16 § 8.1).

Section 112 is a statutory requirement of patentability which may not be ignored.

Appellant argues that since the disclosure in the instant application is the same in pertinent part as the disclosure in ancestor Patent 5,584,032 ('032 patent) and the disclosure of an issued patent is already established as legally correct and presumptively valid, the disclosure in the present application must also be presumed to be correct (Br17-19 § 8.1.1). It is argued that the rejections do not provide acceptable evidence or reasoning to overcome the presumption of correctness (Br17). The examiner notes that the claims in this application are different than the claims in the '032 patent (EA28).

The issue is whether there is written description support for certain terminology in the claims. Appellant seems to misunderstand in the pages and pages of argument that the fact that the relevant disclosure may be the same between the present application and the '032 patent says *nothing* about written description support for the limitations in the present claims. To the extent the '032 patent claims contain language which is rejected here for lack of written description (e.g., "making a product" terminology in section 13), such a rejection is not precluded. *See In re Riddle*, 438 F.2d 618, 620, 169 USPQ 45, 47 (CCPA 1971) ("two wrongs cannot make a right").

Appellant argues (Br19 § 8.1.2) that the examiner expressly admits the final rejection that the disclosure is adequate, citing the following statement (FR26, in the *Schneller*-type double patenting rejection): "The subject matter claimed in the instant application is fully disclosed in the referenced copending application[s] . . . ." The examiner states that this means the copending applications have the same specification and is not an admission that the specification supports the claims at issue (EA29). Appellant argues that the examiner is estopped from assuming contrary positions (RBr9 § 1.4).

It appears that the examiner did not think to carefully qualify the statement in the double patenting rejection, which is part of the test of *Schneller*, in view of the written description rejection. Nevertheless, the written description rejection demonstrates that the examiner does not admit that written description exists in the copending applications (and, hence, this case) for the limitations at issue.

Appellant argues that the subject terminology finds extensive basis in the disclosure and the examiner has failed to reconcile the § 112 rejections with the large number of recitations of the subject terminology in the specification as provided in Table 1; thus the examiner has failed to consider the disclosure as a whole (Br20 § 8.1.3; Br23-24 § 8.1.5). The examiner responds that a lengthy specification is not proof of written description (EA29-30). As to Table 1, the examiner responds (EA30): "This Table [1] is merely a list of simply terms and does not list the complex combinations of elements in the claims. Therefore the specification, while extensive, does not support the claims."

The merits of the disclosure are addressed in connection with the individual rejections. We agree with the examiner that merely pointing to isolated words scattered throughout the specification does not describe the invention claimed as a combination of elements, functions, and interconnections, anymore than a dictionary provides written description support for a book where words are used in combination to provide a certain meaning.

Appellant argues that various claims are erroneously rejected based on unclaimed subject matter (Br21-22 § 8.1.4; RBr12-17 § 2.1).

We agree that the written description inquiry is directed to the claimed invention. Certain rejections are reversed because we agree that they are based on unclaimed subject matter.

Appellant concludes that the examiner requires *verbatim* recitation of strings of words *in exact sequence*, which is contrary to the law (Br48-51 § 8.3.2). Neverthe-

less, it is argued, "there is significant *verbatim* and literal claim terminology in the specification" (Br48).

The examiner does *not* require *in haec verba* (verbatim) support for the claimed subject matter at issue. The examiner properly requires appellant to show written description support for the claim limitation as a whole and not just for isolated words of the limitation spread out over the specification.

General discussion of "processor" disclosure

Many of the rejections deal with lack of written description for: (1) a processor (or vector processor, spatial processor, frequency domain transform processor, etc.) which acts on data accessed (read) from a block memory or from a buffer memory following the block memory; (2) the interconnections of the processor (i.e., what it is coupled to and works "in response to"); and (3) the function of the processor (e.g., generating "two dimensional vector processed image information," "data compressed video image information," "two dimensional spatially processed image information," "weighted frequency domain image information," etc.). Appellant merely provides a Table 1 (Br25) that lists occurrences of words in the limitations somewhere in the specification. "Picking and choosing" terms to assemble limitations without ever disclosing the combination in one location does not establish possession of the claimed limitations pointed out by the examiner as being without support.

To aid in the following analysis, the relevant various processor descriptions, as best we can glean from the disclosure, are summarized below.

The specification discloses a graphics processor having an address generator for generating graphics vectors for storing into image memory and scanning out the information from image memory to refresh a display (spec. at 10). The input device 115A in figure 1 for loading image memory may be a supervisory processor (spec. at 10, 90). The processor for reading out information from the memory is later referred to as a display processor and, in the experimental system, is synchronized with the supervisory processor (spec. at 87).

A register interface may be provided between the buffer memory and the post-processor (spec. at 141). The nature of the post-processor is not described, but it is disclosed that a weight RAM is provided that stores weight information in response to weight information from the buffer memory (spec. at 141), which implies spatial processing, as discussed *infra*.

The specification discloses spatial filtering for anti-aliasing, etc. (spec. at 16). Spatial filtering, as illustrated in figure 5A, may use a 9-pixel "kernel" organized as a 3x3 array comprising a central pixel of interest and 8 surrounding pixels, the pixels are read out from the image memory 520B, each pixel intensity is multiplied by a weight from weight table 520C in a corresponding multiplier 520E, the weights are summed in a summer 520F, and the sum may be converted to analog form in digital to analog converter (DAC) 520G for display (spec. at 16-17). Spatial processing advantageously uses a buffer, such as the first-in first-out (FIFO) buffer in figure 5D, to hold output from the image memory and reduce the number of accesses to the image memory (spec. at 64-74). The disclosed experimental system discloses a 4-line FIFO buffer which stores and outputs

pixel intensities and weight information (figures 6Y to 6AF). Buffered lines of pixels may be shifted from the buffer over 3 output channels to a 3x3 array of registers (figure 6AG) to form a 9-pixel kernel for spatial processing. In spatial filtering, the 9-pixel kernel is provided to the weight logic of figure 6AH for spatial filtering (spec. at 160-164). The spatial filtering is performed under processor control for providing the addresses and control signals.

The specification discloses that the memory arrangement can be applied to a "display system" (spec. at 31-32), a "correlator processor memory" for a "correlator" (spec. at 32), an "FFT [fast Fourier transform] processor memory" for an "FFT processor" (spec. at 33), a "general purpose computer memory" (spec. at 34-35), and "computer main memories, buffer memories, signal processing memories, and other memory applications in addition to display memories" (spec. at 35; *see also* spec. at 59). This discloses, albeit very broadly, use of the memory by special types of processors, but provides no details of the processors.

The specification discloses that image processing can be done offline in the database or online with a preprocessor (spec. at 23, lines 5-7). Online preprocessing can be performed during system operation, such as by accessing database images and preprocessing the accessed database images; prior to loading into image memory (spec. at 23, lines 9-12). The online preprocessing may include compression and decompression prior to loading into image memory (spec. at 23, lines 9-12, 17-19). However, preprocessors dealing with loading image information into the image memory are not relevant to the pro-

cessor limitations at issue, which involve accessing (reading) from the memory.

The specification describes a program FTR.ASC for accessing pixels from a database, "unpacking" the pixels (i.e., decompressing the pixel information), spatially filtering the pixels, "packing" (compressing) the pixels, and storing the pixels in another file (spec. at 18-24; flowchart in figure 7; FTR.ASC listing at 231-236). The program FTR.ASC emulates a hardware filter processor (spec. at 18, lines 2-3) and demonstrates offline filtering and preprocessing (before the image data is loaded into memory) (spec. at 23, lines 20-22). Thus, the emulator program and the processor it runs on does not deal with program control of the claimed hardware memory architecture and is not relevant to the written description issue. *See Lockwood*, 107 F.3d at 1572, 41 USPQ2d at 1968 ("One shows that one is "in possession" of *the invention* by describing *the invention*, with all of its claimed limitations, not that which makes it obvious.").

The specification discloses a software program LD.ASC for loading vectors into memory and a software program GRAPH.ASC for refreshing a CRT monitor from memory (spec. at 91, last para.; LD.ASC described at 10-14 and listing at 217-230; GRAPH.ASC mentioned at 10 and listing at 214-216). A processor is clearly required to perform these functions. The relevant program to the claimed processors is the program GRAPH.ASC which reads data from memory. The operation of the program is not described except in the cryptic comments to the program. However, insofar as we can tell, the program only reads data from memory and does not perform any kind of processing on the data.

1. Claims 1-14, 110-114, and 119-132: "a data decompressed video image input circuit generating data decompressed image information"

The limitation, "a data decompressed video image input circuit generating data decompressed video image information" (independent claims 1-5 and 10-12) requires a "video input circuit" that generates "data decompressed image information," which we interpret to mean image information that has been decompressed from compressed data image information[7] for storage in a block image memory. Independent claims 6-9, 13, and 14 add the limitation "frequency domain" before "image information," but since this is not mentioned by the examiner, we analyze the limitation from claim 1 as representative.

Appellant argues that there is literal support for the limitation because the individual words of the limitation are found somewhere in the specification, referring to Table 1 (Br25) for a listing of occurrences of the terminology "compress" (4 occurrences on page 23), "data compressed" (1 occurrence on page 23), "decompressed" (1 occurrence on page 23), "information" (>100 occurrences throughout the specification), "input" (>200 occurrences throughout the specification), and "video" (8 occurrences on pages 77, 166, 168-171).

Merely pointing to individual words of the limitation scattered throughout the specification is totally unpersuasive of possession of the invention because words in isolation do not describe the structure, functions, and

---

[7] The term "data decompressed" is grammatically unusual if the word "decompressed" is intended to be an adjective modifying "data," because in English adjectives precede the noun.

interconnections among elements defined by the words when combined together in the limitation. It is far easier for appellant to describe where the limitation he wrote is disclosed than for the Office to prove that the limitation is not disclosed. Appellant has failed to point to written description support for the limitation at issue.

Nevertheless, in this case, we find support in the specification at page 23 where it discusses data decompression. The specification describes that image processing can be done offline in the database or online with a preprocessor (spec. at 23, lines 5-7). Online preprocessing can be performed during system operation, such as by accessing database images and preprocessing the accessed database images, prior to loading into image memory (spec. at 23, lines 9-12). The online preprocessing circuitry is a "video image input circuit" for the image memory. Online preprocessing includes "data decompression" (spec. at 23, lines 17-18). Thus, the online preprocessing circuitry generates "decompressed video image information" for writing into the image memory. The "unpacking" described in connection with the offline filtering of figure 7 and the program FTR.ASC (spec. at 18-24) is an example of a well known kind of data decompression, although the FTR.ASC program is a software emulation (spec. at 18) of offline filtering (spec. at 23) and is *not* part of the written description of the memory hardware. We find there is written description support for "a data decompressed video image input circuit generating data decompressed image information." This basis for the written description rejection of claims 1-14, 110-114, and 119-132 is reversed.

2. Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 (all claims): simultaneously writing to and accessing (reading) from memory

The examiner finds that the claims cover simultaneous writing and reading of a block of graphic image data to the block memory, referring to claims 110 and 117, whereas the specification describes a sequential write to and read from the block memory (EA6-7 ¶ 10.4).

Appellant argues that the examiner improperly rejects claims which do not recite "simultaneous" memory accessing and writing (RBr14). It is also argued that the "simultaneous" accessing and writing terminology characterizes the re-addressing and scanout memory architecture (RBr15).

Initially, it is noted that the term "accessing" is used in two different ways. One meaning is sending an address to the memory circuits to select a particular address within all 64 memory circuits arranged in an 8x8 array on a board ("re-addressing") (*see* claim 110 which requires "simultaneously accessing the 64 pixels arranged as eight rows and eight columns of pixel information") *or* selecting a particular memory circuit within the 8x8 array on the selected board to read out the pixel data ("scanout") (*see* spec. at 47: "The access time from the address select is significantly greater than the access time from the chip select or the output enable select. Therefore, accessing with the chip select and output enable signals can proceed at a significantly faster rate than accessing with the address select."). That is, all of the 64 memory circuits may be accessed simultaneously by re-addressing, as in claim 110, but only 1 of the 64 pixels is accessed to be read out sequentially by

scanout (spec. at 49). However, the general meaning from the specification is "reading" from the memory, which includes sequential "re-addressing" and "scanout" steps. Although it would be better to use different words for different functions to prevent confusion, the terminology is consistent with the specification and the particular meaning is clear in context.

The claims do not recite simultaneously writing and accessing (reading) the memory. Therefore, the examiner erred in rejecting the claims for lack of written description of this unclaimed feature. The fact that the claims do not preclude simultaneous writing and accessing means that the claims are broad. However, claim breadth should not be confused with indefiniteness. *In re Miller*, 441 F.2d 689, 693, 169 USPQ 597, 600 (CCPA 1971). Similarly, claim breadth should not be mistaken for lack of written description. In any case, it is disclosed that the image memory can be implemented as a dual port memory for simultaneously writing into and accessing (reading) from image memory (spec. at 11), as was well known. This basis for the written description rejection of claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 is reversed.

3. Claims 1, 2, 5, 9, 10, 12, 20, 81, 85, 98, 110-114, 119, 120, 123, 127, 128, 130, 136, 153, 157, and 161: vector processor generating two dimensional vector processed image information in response to video pixel information and in response to vector information

An exemplary limitation is (claim 1):

a two dimensional vector processor coupled to the accessing circuit and coupled to the vector

> generator, the two dimensional vector processor generating two dimensional vector processed image information in response to the accessed blocks of video pixel information accessed by the accessing circuit and in response to the two dimensional vector information generated by the vector generator; . . . .

An exemplary process limitation is (claim 81):

> generating two dimensional processed image information in response to the accessed blocks of pixel image information and in response to the two dimensional vector information; . . . .

Minor differences in language exist among the claims that do not affect the analysis. For example, claim 20 refers to a "block processor" instead of a "vector processor," and refers to a "pixel block memory accessing circuit" instead of an "accessing circuit, but the written description problem is the same. It is noted that the vector processor in claims 2, 5, 10, and 12 generates "data compressed video image information," instead of "two dimensional vector processed image information," which limitation is addressed in a subsequent rejection in section 12.

The specification discloses a processor (which may be a supervisory processor coupled with a display processor, spec. at 87) controlling the various elements of the memory architecture including the address generators of figures 6Q and 6R for generating graphics vectors into memory (which we interpret to be the "vector generator") and the address generators of figures 6O and 6P for generating raster scan addresses for scanning out image memory (which we consider to be part of the "ac-

cessing circuit"), memory arrays, clock and control logic, buffer memory, and spatial processing circuitry. That is, the processor may be thought of as a processor for writing information into the block memory and a processor for accessing (reading) information from block memory and controlling further operations, such as the spatial processing of figure AG and 6AH, although the drawings, such as figure 1, do not illustrate a processor block connected to the memory, buffer, and output device. Thus, there is support for a processor "coupled to the accessing circuit and coupled to the vector generator."

However, the limitation at issue requires that the processor perform the function of "generating two dimensional processed image information in response to . . . video pixel information . . . and in response to the two dimensional vector information generated by the vector generator." This implies that the "generating" function operates on two kinds of input data: pixel information from memory and vector information. However, the specification describes graphics vectors being generated (strobed) into image memory (e.g. spec. at 11-12), *not* being generated and used by a processor together with accessed pixel data read out from the block image memory, which would require bypassing the block memory. That is, the disclosed processor only controls the vector generator, it does not receive data from it or operate "in response to" it. Since the vector information is stored into the block memory, we find no written description for a processor coupled to and performing the "generating" function "in response to" the vector information as well as "in response to" image information from the image memory.

Appellant merely points to Table 1 (Br25) for occurrences of words in the limitation and does not show where the specification describes the claimed structure or process. This does not show written description for the limitation as a whole and is not persuasive of error in the rejection. Appellant does not point to a written description of a processor performing a generating function responsive to the two specific types of information. Manifestly, the time for appellant to have pointed to support for the limitations at issue was in the appeal brief or reply brief and not by the way of new arguments in any request for rehearing; new arguments will not be considered. This basis for the written description rejection of claims 1, 2, 5, 9, 10, 12, 20, 81, 85, 98, 110-114, 119, 120, 123, 127, 128, 130, 136, 153, 157, and 161 is sustained.

4. Claims 3, 4, 11, 121, 122, and 129: a processor generating data compressed video image information in response to accessed blocks of video pixel image information

An exemplary limitation is (claims 3 and 4):

> a processor coupled to the accessing circuit and generating data compressed video image information in response to the accessed blocks of video pixel image information generated by the accessing circuit; . . . .

Claim 11 replaces "accessing" with "pixel block memory reading" and removes the term "accessed"; however, "accessing" is the same as "reading." This limitation requires a processor generating compressed data from ("in response to") pixel image information accessed

(read) from the block image memory. This rejection is cumulative to the rejection of section 12.

While a processor is coupled to the accessing circuit comprising the block memory of figures 6E to 6N and the raster scan address generator of figures 6O and 6P, we find no disclosure of the processor "generating data compressed video image information," as claimed. The only compression mentioned in the specification is concerned with compression and decompression offline or online prior to loading into the image memory or in connection with an emulation program, not after it is stored in the block image memory.

Appellant merely points to Table 1 (Br25) for occurrences of words in the limitation and does not show where the specification describes the claimed structure or process. This does not show written description for the limitation as a whole and is not persuasive of error in the rejection. This basis for the written description rejection of claims 3, 4, 11, 121, 122, and 129 is sustained.

5. Claims 1, 85, 95, 110-112, 119, 157, and 158: spatial processor generating data compressed video image information in response to video pixel information and in response to vector processed image information

An exemplary limitation is (claim 1):

> a two dimensional spatial processor coupled to the buffer memory and generating data compressed video image information in response to the buffered blocks of video pixel information stored in said buffer memory and in response to

the buffered two dimensional vector processed image information stored in said buffer memory.

A processor controls the spatial processing circuitry of figures 6AG and 6AH, and the processor and controlled spatial processing circuitry together are considered a "two dimensional spatial processor." However, as discussed in the preceding section 4, we find no disclosure of a processor "generating data compressed video image information" on data anytime after it is stored in the block image memory. Nor do we find any disclosure of compression of data taken from the buffer memory. The specification discloses compression and decompression of data prior to loading into the image memory (spec. at 23), but this does not teach compression elsewhere in the circuitry. *See Lockwood*, 107 F.3d at 1572, 41 USPQ 2d at 1968 (obviousness is not the test of written description). In addition, the limitation of "generating data compressed video image information *in response to* . . . video pixel information . . . *and in response to* . . . two dimensional vector processed image information" (emphasis added), implies that the processor somehow distinguishes between (operates "in response to") the two different types of information, and appellant has also failed to show written description support for these "in response to" limitations. Finally, as discussed in section 3, the specification does not provide written description support for the "processor generating two dimensional vector processed image information in response to [video pixel information and in response to vector information]," as claimed, so there is no written description support for the limitation of "buffered two dimensional vector processed image information stored in said buffer memory."

Appellant merely points to Table 1 (Br25) for occurrences of words in the limitation and does not show where the specification describes the claimed structure or process. This does not show written description for the limitation as a whole and is not persuasive of error in the rejection. This basis for the written description rejection of claims 1, 85, 110-112, 119, and 157 is sustained.

Process claim 95 does not contain any of the noted problem limitations. Accordingly, the rejection of claims 95 and 158 is reversed.

6. Claims 6-9, 13, 14, 24, 34, 36, 42, 49, 50, 102, 106, 115-118, 124-127, 131, 132, 139, 141, 143, 145, 149, 150, 165, and 169: frequency domain transform processor generating data compressed video image information or generating frequency domain image information

There are two types of limitations. A first exemplary limitation is (claim 6):

> a two dimensional frequency domain transform processor coupled to the accessing circuit and generating data compressed video image information in response to the accessed blocks of video frequency domain information accessed by the accessing circuit;

A second exemplary limitation is (claim 24):

> a frequency domain transform processor coupled to the pixel block memory accessing circuit and generating frequency domain image information in response to the blocks of pixel image

> information accessed by the pixel block memory accessing circuit; . . . .

In the first case, the processor generates "data compressed video image information" and, in the second case, the processor generates "frequency domain image information."

Independent claims 6-9, 13, and 14 all contain the limitation of "generating data compressed video image information." As discussed in sections 4 and 5, there is no written description support for any data compression by a processor after information is stored in the image memory. This rejection is cumulative to the rejection of section 12 as to claims 6-9, 13, 14, 124-127, 131, and 132.

Appellant merely points to Table 1 (Br25) for occurrences of words in the limitation and does not show where the specification describes "data compression" of information from the memory. This is not persuasive of error in the rejection. This basis for the written description rejection of independent claims 6-9, 13, and 14, and dependent claims 124-127, 131, and 132 is sustained.

Independent claims 24, 34, 36, 42, 49, 50, 102, 106 recite "generating frequency domain image information in response to . . . image information [from the memory]." Appellant refers to the terminology "frequency (FFT)" in Table 1 (Br25), which refers to 7 occurrences on pages 33-34. The corresponding note to this entry states (Br27):

> NOTE-C: An FFT (Spec. at 33-34) is a well known frequency domain transform. The term "frequency-domain" is described in Appellant's prior Patent No. 4,209,843. [Footnotes omitted.]

Appellant does not point out support for the limitation as a whole. Nevertheless, we find that the specification discloses that the memory arrangement can be applied to an "FFT [fast Fourier transform] processor memory" for an "FFT processor" (spec. at 33), and that the buffer memory (and, by implication, the image memory) store FFT data. We agree that one of ordinary skill in the art would recognize an FFT as a two dimensional frequency domain transform, so an FFT processor would generate frequency domain image information. Thus, there seems to be minimal, but sufficient, support for a two dimensional frequency domain transform processor accessing frequency domain information and generating frequency domain image information in response to that information as recited in claims 24, 34, 36, 42, 49, 50, 102, 106. Therefore, the rejection of independent claims 24, 34, 36, 42, 49, 50, 102, and 106, and dependent claims 115-118, 139, 141, 143, 145, 149, 150, 165, and 169 is reversed.

7. Claims 17, 18, 133, and 134: block processor generating two dimensional processed image information in response to pixel image information and in response to vector information

An exemplary limitation is (claim 17):

> a two dimensional block processor coupled to the frame buffer accessing circuit and coupled to the vector generator, the two dimensional block processor generating two dimensional processed image information in response to the blocks of pixel image information accessed by the frame buffer accessing circuit and in response to the

two dimensional vector information generated by the vector generator; . . . .

As discussed in section 3, the specification does not describe a processor acting "in response to" vector information because vector information generated by the vector generator (address generators of figures 6Q and 6R; spec. at 11) is stored in the block memory (e.g., spec. at 11, 50) under control of a processor and the vector information it is not combined by a processor with pixel data accessed (read) from the image memory (or, at least, appellant has failed to show that it is). Since a processor is not connected to receive both vector information from the vector generator and pixel image information from the image memory, there is no written description for a processor performing the function of "generating two dimensional processed image information *in response to* . . . [pixel image information] *and in response to* . . . [vector information]."

Appellant merely points to Table 1 (Br25) for occurrences of words in the limitation and does not show where the specification describes the claimed structure or process. This does not show written description for the limitation as a whole and is not persuasive of error in the rejection. This basis for the written description rejection of claims 17, 18, 133, and 134 is sustained.

8. Claims 24, 34-37, 42-45, 49-51, 102-109, 115-118, 139-151, and 165-172: input weight circuit generating input weight information

The examiner finds (EA13-14):

No claims in this application directly claim an input weight circuit generating input weight infor-

> mation, however, claims 24, 34-37, 42-45, 49-51, 102-109, 115, and 116 claim other weight related elements. An input weight circuit generating input weight information is not supported by the specification.

The examiner finds that the specification fails "to teach an address generator which will generate weight addresses for selecting weight values from the weight table to perform the desired weighting function at the spatial filter" (EA15). The examiner notes that "this rejection is derived from the copending applications which explicitly claimed *an input weight circuit generating input weight information*" (EA30). The examiner states that the unclaimed limitations are critical and necessary to the claim for support (EA30).

Appellant argues that this rejection is erroneously based on unclaimed subject matter (RBr12-14 § 2.1).

A written description rejection must be based on the claimed subject matter. The examiner expressly admits that the claims do not recite the limitation for which written description support is said to be lacking. If the unclaimed limitations are critical and necessary to the claim for support, it would seem that there should be some limitation in the claim which requires this unclaimed subject matter in other language. We will not guess at what language that would be. Since the rejection is based on unclaimed subject matter, the written description rejection is in error. The rejection of claims 24, 34-37, 42-45, 49-51, 102-109, 115-118, 139-151, and 165-172 is reversed.

9. Claims 34, 36, 42-45, 106-109, 141, 143, 145-148, and 169-172: block boundary smoothing

An exemplary limitation is (claim 34):

> a block boundary smoothing processor generating block boundary smoothing information to smooth the pixel image information at boundaries between blocks of pixel image information;
> . . . .

A "block" is disclosed to be an array of 64 pixels arranged in 8 rows and 8 columns having a single address (or "re-address") of 11 bits. Pixels are selected within this block by a "scanout" address comprising the 3 least significant bits of the X and Y address. A "block boundary" occurs going from one block (one 11-bit address) to another block (another 11-bit address) during "re-addressing." We find nothing in the specification that describes "smoothing" or "block boundary smoothing." While the word "smoothing" occurs in the program FTR2.ACS (spec. at 232, program line 110), this refers to "SMOOTHING PRINTOUTS" without explanation. In any case, the program FTR2.ASC is for prefiltering the database image by taking an image from a file in conventional computer memory, filtering the kernel of 9 pixels using one of three sets of weights (program lines 170-210), and storing the image back into a file: as we understand it, it does *not* use a memory having blocks or block boundaries and so is not relevant to the issue of block boundary smoothing.

Appellant merely points to Table 1 (spec. at 23) (Br25) for occurrences of the terminology "block," "boundary," and "smoothing." This does not show written description for the limitation of "block boundary

smoothing" as a whole and is not persuasive of error in the rejection. This basis for the written description rejection of claims 34, 36, 42-45, 106-109, 141, 143, 145-148, and 169-172 is sustained.

10. Claim 112: video image data compression system

Claim 112 recites "wherein the memory system is a video image data compression system."

The limitation requires that the output of the memory system is compressed data. As discussed in sections 4-6, we find no written description for the output of the image memory or the buffer memory being compressed.

Appellant merely points to Table 1 (spec. at 23) (Br25) for occurrences of the terminology. This does not show written description support for the limitation at issue. This basis for the rejection of claim 112 is sustained.

11. Claim 116: weighting processor is a quantization weighting processor

Claim 116 depends on claim 24 and recites:

> wherein the weighting processor is a quantization weighting processor generating the weighted frequency domain information as quantized weighted frequency domain information by weighting the frequency domain image information generated by the frequency domain processor in response to the accessed weight information generated by the weight memory accessing circuit.

Appellant points to Table 1 (Br25) which indicates that there are over 100 occurrences of the terminology "quantization," at representative pages 231-236, and states (Br27):

> NOTE-E: The Basic computer programs (Spec. at 214-236) use, for example, the "%" integer declaration character, the "FIX" truncated integer arithmetic function, and the "INT" integer arithmetic function. These Basic computer instructions round, truncate, and otherwise quantize the operands. (*See* Exhibit-4). The "%" declaration character occurs more than 100 times, the "FIX" arithmetic function occurs more than 10 times in the Basic computer programs, and the "INT" arithmetic function occurs more than 100 times in the Basic computer programs (Spec. at 214-36).

Table 1 is misleading in the sense that the word "quantization" does not actually appear in the specification. Instead, appellant relies on the "%" symbol, and the "FIX(exp)" and "INT(exp)" arithmetic functions in the computer programs at pages 214-236 as showing quantization. The "%" symbol after an identifier indicates an integer type (Exhibit 4, p. 2, under "Variable Type Declaration Characters") and if an integer variable, say "A%", is set equal to a numeric constant of another type, say a floating point number 23.42, it will convert it into an integer value, 23 (Exhibit 4 § 1.7, example 1).[8] The "FIX(exp)" function returns a truncated integer of the expression and the "INT(exp)" function evaluates the expression for the largest integer contained

[8] Of course, setting an integer variable equal to an integer is not quantization.

therein (Exhibit 4, p. 13).[9] The examiner finds that "%" is rounding and not truncation and that appellant's argument does not support truncation (EA32). It is not known why the examiner is talking about truncation, when the issue is "quantization." We agree that changing floating point numbers to integers in the three ways described in Exhibit 4 to the brief constitutes "quantization." However, the existence of quantization somewhere in the system is not persuasive or written description support for the particular claim limitation at issue.

The claim limitation is directed to quantization after the pixel image information is accessed (read) from the block memory. Thus, the program LD.ASC (spec. at 217-230), which deals with loading a file to the image memory (spec. at 91), and the program FTR.ASC (spec. at 231-236), which deals with prefiltering the database image (spec. at 18-24), do not appear relevant to the quantization written description issue. The program GRAPH.ASC (spec. at 214-216), which deals with refreshing a CRT monitor from memory (spec. at 91), could be relevant. However, the GRAPH.ASC apparently simply accesses (reads) pixel information out of memory (and it is very cryptic how it does that) and does not perform any frequency domain processing, does not control the weight memory accessing circuit, and does not perform any quantization weighting of weighted frequency domain information. Thus, we fail to see how the program GRAPH.ASC, or the other programs, LD.ASC

---

[9] Although appellant states that the "INT" function occurs more than 100 times, we do not find any actual occurrences of the "INT (exp)" function. An expression such as "INT1%=0" (24 places in spec. at 229) gives an integer variable an integer value; it is not an example of the "INT(exp)" function, nor is it an example of quantization of a floating point number.

or FTR.ASC, provide written description support for the limitation at issue. This basis for the rejection of claim 116 is sustained.

12. Claims 2-14, 113, 114, and 120-132: "generating data compressed video information"

An exemplary limitations is (claim 2):

> a two dimensional vector processor coupled to the accessing circuit and coupled to the vector generator, the two dimensional vector processor *generating data compressed video image information* in response to the accessed blocks of video pixel image information accessed by the accessing circuit and in response to the two dimensional vector information generated by the vector generator; . . . . [Emphasis added.]

Independent claims 2-8 recite that the "data compressed video image information" is stored in a buffer memory and independent claims 9-14 recite an output circuit for outputting the "data compressed video image information."

As discussed in sections 4-6, we find nothing in the specification that describes "generating data compressed video image information" from the accessed blocks of video pixel information. The rejection of claims 3, 4, and 11 in section 4, and the rejection of claims 6-9, 13, and 14 in section 6, are redundant in the sense they are based on the absence of written description for the same language of "generating data compressed video image information." In view of the complicated claim structure, it is difficult to form groups without some overlap.

Appellant merely points to Table 1 (spec. at 23) (Br25) for occurrences of the terminology in the limitation. This does not show written description support for the limitation as a whole and is not persuasive of error in the rejection. This basis for the written description rejection of claims 2-14, 113, 114, and 120-132 is sustained.

13. Claims 153-172: "making a product in response to the output image information"

An exemplary limitation is "the act of making a product in response to the output image information" (claim 153).

Appellant argues that "product" terminology is statutory language under 35 U.S.C. § 271(g) (Br29 § 8.1.6).

The issue is not whether "product" is statutory language, but whether there is written description support for the step of making a product in response to certain information.

Appellant argues that products include "machines" and "manufactures" and that clearly the disclosed apparatuses constitute "machines" and "manufactures" and, hence, products (Br29-30 § 8.1.6). Therefore, the disclosed signals constitute "manufactures" (and hence "products") because the signals are physical things made by the disclosed circuits (Br30).

The terminology "producing a product" finds no written description support in the specification. Appellant's position is that the "product" can be a signal. We disagree. *First*, the claims recite "making a product in response to . . . image information," where the "image

information" is the signal and the "product" must be something else, which is not disclosed.

Second, the three product classes (machine, manufacture, and composition of matter) have traditionally required physical structure or matter and a signal, while physical, does not have a tangible physical structure. A "composition of matter" "covers all compositions of two or more substances and includes all composite articles, whether they be results of chemical union, or of mechanical mixture, or whether they be gases, fluids, powders or solids." *Shell Development Co. v. Watson*, 149 F. Supp. 279, 280, 113 USPQ 265, 266 (D.D.C. 1957), *aff'd*, 252 F.2d 861, 116 USPQ 428 (D.C. Cir. 1958). A signal is not matter, but is a form of energy, and therefore is not a composition of matter.

"The term machine includes every mechanical device or combination of mechanical device or combination of mechanical powers and devices to perform some function and produce a certain effect or result." *Corning v. Burden*, 56 U.S. (15 How.) 252, 267 (1854); *see also Burr v. Duryee*, 68 U.S. (1 wall.) 531, 570 (1863) (a machine is a *concrete* thing, consisting of parts or of certain devices and combinations of devices). A modern definition of machine no doubt includes electronic devices which perform functions. Indeed, devices such as flip-flops and computers are referred to in computer science as sequential machines. A signal, while physical, has no concrete tangible physical structure, and does not itself perform any useful, concrete and tangible result; thus, a signal does not fit within the definition of a machine (or product).

The Supreme Court has read the term "manufacture" in accordance with its dictionary definition to

mean "the production of articles for use from raw or prepared materials by giving to these materials new forms, qualities, properties, or combinations whether by hand-labor or by machinery." *Diamond v. Chakrabarty*, 447 U.S. at 308, 206 USPQ at 196-97 (*quoting American Fruit Growers, Inc. v. Brogdex Co.*, 283 U.S. 1, 11, 8 USPQ 131, 133 (1931), which, in turn, quotes the *Century Dictionary*). Other courts have applied similar definitions. *See American Disappearing Bed Co. v. Arnaelsteen*, 182 F. 324, 325 (9th Cir. 1910), *cert. denied*, 220 U.S. 622 (1911). These definitions require physical substance, which a signal does not have. Accordingly, we conclude that a signal is not a product.

Appellant argues that claims reciting "making a product" have already been issued in an ancestor patent, the claims in that patent have a presumption of validity, and since the present disclosure is the same as the disclosure in that patent, it must be accepted that there is written description for the terminology in this application (Br30).

The fact that other patents have been issued with similar language is irrelevant. *See Riddle*, 438 F.2d at 620, 169 USPQ at 47 ("two wrongs cannot make a right").

Appellant argues that the disclosure recites ample product related terminology, such as "constructed," "manufactured," "implemented," "interconnected," etc. (Br32-33 § 8.1.7).

These terms deal with the apparatus and have not been shown to be relevant to the claimed process limitation of "producing a product."

In conclusion, we find no written description support for "producing a product." The rejection of claims 153-172 is sustained.

The enablement rejection

Appellant argues that the disclosure is enabling because it includes extensive design details of the circuitry and signals down to pin designations and wire connections (Br38-40 § 8.2.1) and makes extensive use of commercially available products and integrated circuit components (Br40-44 § 8.2.2). It is argued that the enablement rejection improperly ignores the level of skill in the art (Br44-46 § 8.2.3).

The issue is whether one of ordinary skill in the art could make the *claimed* invention *having all the limitations which are said to be without written description support, not* whether one of ordinary skill could make the subject matter described in the specification. There appears to be no question that what is described is enabled. Appellant's enablement arguments are not persuasive because they do not address the claimed invention. It is well settled that the enablement requirement is separate and distinct from the written description requirement of § 112, first paragraph, *see Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555, 1563, 19 USPQ 2d 1111, 1117 (Fed. Cir. 1991), and that a specification may enable one skilled in the art to make and use an invention and yet still not describe it, *see id.* at 1562, 19 USPQ 2d at 1115. Nevertheless, here we treat the enablement rejections as standing or falling together with the written' description rejections because appellant provides no arguments why the *claimed* invention is enabled even if it based on a lack of written description. That is, it is fair to presume that one of ordinary skill would not

know to make an invention which is not described, absent argument to the contrary.

The rejections of claims 1-14, 17, 18, 20, 34, 36, 42-45, 81, 85, 98, 106-114, 116, 119-134, 136, 141, 143, 145-148, and 153-172 under § 112, first paragraph, based on lack of enablement are sustained based on the affirmance of the lack of written description rejections. The rejections of claims 19, 22-25, 35, 37, 49-52, 82-84, 95-97, 99-105, 115, 117, 118, 135, 137-140, 142, 144, and 149-152 for lack of enablement are reversed.

14. Obviousness-type double patenting

Line of demarcation between applications

Appellant alleges that the double patenting rejections are inappropriate in view of the 12-way restriction requirement in parent Application 08/034,627, now U.S. Patent 5,584,032, and the restriction requirements in copending (but apparently unrelated) Applications 08/471,710 and 08/464, 441 (Br53-56 § 8.4.1). Appellant also argues that the claimed invention is independent and distinct from the claimed inventions in the copending applications (Br57-58 § 8.4.2). The examiner seems to say that the present invention is not to one of the restricted inventions and the claim subject matter is an obvious variant of the inventions claimed in the copending applications (EA36-37).

When subject matter has been restricted, an applicant is required to maintain "consonance" between applications. *See Gerber Garment Technology Inc. v. Lectra Systems Inc.*, 916 F.2d 683, 688, 16 USPQ 2d 1436, 1440 (Fed. Cir. 1990) ("Consonance requires that the line of demarcation between the 'independent and distinct' inventions that prompted the restriction re-

quirement be maintained. Though the claims may be amended, they must not be so amended as to bring them back over the line imposed by the restriction requirement."). The restriction requirement should clearly define the "independent and distinct inventions." Similarly, where, as here, an applicant voluntarily files divisional (or multiple continuation) applications without a restriction requirement, examiners have the authority to require the applicant to define and maintain a clear line of demarcation between the applications by requiring a description of the independent and distinct invention contained in each application. *See* 37 CFR § 1-78(b) (where two of more copending applications contain overlapping or conflicting claimed subject matter, an applicant may be required to cancel the conflicting claims from all but one application); *Manual of Patent Examining Procedure* § 822. Regardless of whether the identification of the independent and distinct inventions arises from a restriction requirement or from a statement by the applicant, the line of demarcation is the surest way to particularly identify what independent and distinct invention is being claimed in each application and to keep the inventions separate (i.e., to keep the inventions from migrating from case to case over time). Double patenting rejections should only occur when applicant crosses over the line.

Unfortunately, it does not appear that the examiner has required appellant to define the independent and distinct invention in each application at issue, so the line of demarcation is not defined. While appellant argues that independent and distinct inventions are claimed, we have no definition of what those inventions might be. Nor do we have any evidence that the present application is a result of a restriction requirement. Manifestly,

it would be to everyone's benefit to have a master list of what independent and distinct invention is (or is intended to be) claimed in each application. Here, we are forced to look at the double patenting rejection.

Analysis

The examiner rejects all the claims of the present application as being unpatentable over apparently all of (we cannot tell without ordering all the files) the claims in each of eight copending applications. No claim charts, discussions, or other means of comparison or correlation of the present claims with the claims in the copending applications are provided. In the response to the arguments section of the examiner's answer, the examiner invites (at EA37-38) the Board to compare the following claims with each other:

	claims	application	
compare	22, 23, 84	08/471,702	(present application for a first level of claim detail)
with	25, 105	08/471,704	
	4, 6, 96	08/471,712	
	7, 8, 9, 97	08/471,925	
	43, 112	08/472,062	
	7, 8, 83	08/479,086	
	23	08/479,087	
	7, 8, 97, 98	08/479,088	
	3, 6, 91	08/483,016	

	claims	application	
compare	25, 100	08/471,702	(present application for a second level of claim detail)
with	25, 82	08/471,712	
	25, 100	08/471,925	
	45	08/472,062	
	25, 82	08/479,086	
	25, 52	08/479,087	
	25, 102	08/479,088	
	22, 94, 96	08/483,016	

The examiner concludes that "[c]learly claims in this application claim the same obvious invention that is claimed in the copending applications" (EA38). The examiner states that a limitation-by-limitation comparison is not necessary, because "when the above listed claims are compared it is clear that small variations exist between at least some of the claims in the copending applications" (EA39).

Appellant responds that the examiner has listed only five claims (22, 23, 25, 84, and 100) as conflicting with 36 claims in eight copending applications and only these claims should be relevant to the rejection (RBr5-6). It is argued the rejection should be reversed because the examiner has failed to perform a limitation-by-limitation analysis.

The rejection rejects 117 claims of the present application over 117 claims in each of the applications 08/471,704, 08/471,712, 08/471,925, 08/479,086, 08/479,087, 08/479,088, and 08/483,016, and over 78 claims in application 08/472,062. No correlation of the

individual claims of the present application with individual claims in the copending applications is provided. Thus, the rejection invites comparison of each of the 117 claims in the present application to each of the 117 (or 78) claims in the copending applications, for a possible 117 117 = 13,689 or 117 78 = 9,126 comparisons per copending application. This is not feasible or reasonable. The rejection of five claims in the present application over 36 claims in the eight copending applications as set forth in the tables in the examiner's remarks (EA37-38), still requires comparing two claims of the present application with 22 claims of the copending applications, or three claims of the present application with 14 claims of the copending applications. However, since there are a fewer number of claims, we will at least look at these claims.

In view of the examiner's assertion that a simple comparison of claims is required to establish that there are only small variations between at least some of the claims, and the absence of any discussion of the obviousness of the differences, we would expect the claimed subject matter to be nearly identical. However, this is not true. While we recognize that appellant is a practiced "wordsmith" who often uses different terminology to describe the same thing, it is the examiner's duty to account for all the differences in terminology, as well as other differences, to establish a *prima facie* case of obviousness-type double patenting. We have spent considerable time (undoubtably much more than the cursory nature of the rejection deserves) comparing the limitations of claims 22, 23, 25, 84, and 100 of the present application with the 36 claims of the copending applications. We find numerous limitations in the claims of this application which are not found in the claims of the copending

applications and *vice versa*. Although we do not completely agree with appellant's claim charts (Exhibit 2 to brief; Exhibits to reply brief), the claim charts do point out the many differences which the examiner has not addressed. Absent reasoning by the examiner to explain why these differences are immaterial or would have been obvious, the rejection fails to state a *prima facie* case. The obviousness-type double patenting rejection of claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 is reversed.

15. Schneller-type double patenting

The Board affirmed, *inter alia*, a double patenting rejection under the *Schneller* rationale against the present appellant in *Ex parte Hyatt*, Appeal No. 98-0586, Application 05/948,053 (Bd. Pat. App. & Int. March 24, 1999) (*Schneller*-type double patenting where appellant was trying to claim subject matter which was fully disclosed in U.S. Patent 4,016,540 issued in 1977, and covered by claims 16 and 20 of that patent, which claims we noted had been held invalid for obviousness in *Mattel v. Hyatt*, 206 USPQ 499 (C.D. Cal. 1979), *aff'd* 644 F.2d 757, 212 USPQ 808 (9th Cir. 1981)). Therefore, we are not persuaded by appellant's arguments that *Schneller* is overruled (e.g., Br72-75 §§ 8.6.1).

In the past, the U.S. Patent and Trademark Office (USPTO) applied the term "non-'obviousness-type'" (as opposed to "obviousness-type") double patenting to the factual situation in *Schneller*, MPEP § 804 (6th ed. Jan. 1995), pages 800-15, -16, but does not now use this label, *see* MPEP § 804 (7th ed. July 1998), pages 800-21 through 800-23, characterizing it as a second form of nonstatutory double patenting. In our view, *Schneller*

is a special obviousness-type double patenting case with very special facts and, thus, should be rarely used.

Schneller applies to those situations where: (1) the subject matter recited in the claims of the application is fully disclosed *and* covered by a claim in the patent (i.e., there has been no improvement or modification invented after filing *and* the application claim reads on subject matter which has been protected by a patent claim); *and* (2) there is no reason why appellant was prevented from presenting the same claims for examination in the issued patent (i.e., there is no justification for extending the protection, such as the existence of a restriction requirement). The examiner states in a conclusory manner that these conditions are satisfied (EA25) without providing any further reasoning.

It is not clear that provisional rejections are consistent with *Schneller*, which dealt with the issue of extending the term of an issued patent by claiming subject matter which was covered by claims of the patent. Since the present application and the copending applications were all filed on the same date, June 6, 1995, the same considerations are not present. Manifestly, if the examiner had required appellant to specify and maintain a line of demarcation between independent and distinct inventions in the copending applications, there now would be no kind of double patenting issue. The present application is a continuation of Application 08/815,644, now U.S. Patent 5,584,032 ('032 patent), but the examination does not reject the claims of the present application for obviousness-type double patenting or *Schneller*-type double patenting over the claims of the '032 patent. However, assuming, *arguendo*, that a provisional rejection is proper under *Schneller*, the examiner has not

even attempted to prove the requirement that the claims of the present application are covered by (within the scope of) the claims in the copending applications. As with the obviousness-type double patenting rejection, the examiner provides no analysis of the claim limitations. Therefore, we conclude that the examiner has failed to establish a *prima facie* case of double patenting under *Schneller* and the rejection of claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 is reversed.

16. Anticipation

Appellant argues that the § 102 rejection does not establish identity of subject matter (Br100-102 § 8.8.1). It is argued that the "ing" functions (e.g., generating, storing, etc.), the "in response to" limitations, and the "coupling" limitations all constitute contested limitations and the claims all have novel distinctions over Hill (Br102-107 § 8.8.2). Appellant states that representative limitations which distinguish over Hill are excerpted (Br104). It is argued that the examiner fails to establish a *prima facie* case because he has not provided a limitation-by limitation analysis (Br108 § 8.8.3).

The examiner properly notes that "Appellant has not pointed to any specific differences between Hill and the rejected claims" (EA45). The examiner for the first time provides an idea of how the claims are intended to be read on Hill (EA45-46).

Appellant responds by alleging specific differences not taught by Hill (RBr51-58 §§ 4.1 & 4.2). It is sufficient to address one of the differences. Claims 22, 83 recite "the frame of image information *arranged in a two dimensional array of rows and columns of blocks of pixel image information*" (emphasis added) and claims

23, 82, 84, 95, and 99 recite "the two dimensional array of blocks of pixel image information *arranged in a two dimensional array of rows and columns of blocks of pixel image information*" (emphasis added). The examiner finds that Hill "stores a block of video data" (EA26). Appellant argues (RBr51) that this is not the same as "a two dimensional array of rows and columns of blocks of pixel image information." We agree that an array of blocks is different from a block. The examiner finds that Hill teaches "storing an array of blocks (164) (EA46). Appellant argues that Hill does not teach that the matrix RAM 164 stores blocks (RBr51). We agree that Hill does not teach storing an array of blocks. There are no details of the picture matrix memory 164; the block diagram of figure 5 shows only a linear address space. Therefore, the examiner erred in finding anticipation because Hill does not teach, at least, "a two dimensional array of rows and columns of blocks of pixel image information." The anticipation rejection of claims 22, 23, 82-84, 95, 99, 137, and 138 is reversed.

17. Obviousness

Appellant argues that the obviousness rejection relies on improper hindsight (Br110-115 § 8.9.1).

These arguments are merely a boilerplate summary of the case law and do not specify what modifications are thought to be based hindsight. This mode of argument is totally unpersuasive.

Appellant argues that the examiner has failed to make the required findings under *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966) and has failed to provide an express limitation-by-limitation analysis (Br115-117 § 8.9.2).

This panel will not reverse for these reasons.

Appellant argues that the claims distinguish over the references based on certain limitations (Br117-120 § 8.9.3). Appellant argues that the examiner has not established a *prima facie* case of obviousness and fails to consider important claim limitations (Br121-123 § 8.9.4).

These arguments do not point to any actual differences and do not address the deficiencies in the actual rejection.

In the reply brief, appellant argues that the claims define over Hill, Lord, and Lelke by novel block-related limitations (RBr59-60) and novel addressing, writing, accessing, and clocking limitations (Br60-62). The underlining of terms appearing in the claims is not persuasive because it fails to address the collective teachings of the references. Nevertheless, upon review, we will not sustain the rejection.

Lord discloses a television display system which increases the number of fields per second and/or lines per second to improve the quality of the lines. The field stores in figure 1 may, in one example, hold two fields (even and odd) which constitutes a television frame; thus, the field stores holding two fields is broadly considered a "frame buffer," as claimed. As shown in figure 6, the field may be read out twice with a slight perturbation in the horizontal or vertical scan waveform causing a slight offset (col. 4, line 33 to col. 5, line 16). It is possible to interpolate between points on lines of a field and between points of a line as shown in figure 10 (col. 5, lines 17-38) or in other ways using the interpolator 21 following the line stores. (The television display does not have fixed pixel locations like a computer monitor.)

We find that the interpolator 21 is broadly a "spatial processor generating two dimensional spatially processed image information in response to [image information accessed from the frame buffer]," since a "processor" can be any circuit that performs a function and does not have to be a computer.

However, although not argued by appellant, we cannot ignore that the field and line stores in Lord are not described to be digital memories, as apparently assumed by the examiner. Note the absence of analog-to-digital (AD) and digital-to-analog (DAC) converters and digital circuitry. It is not described how the write and line stores (memories) are constructed; however, Lord only requires reading out lines from the memories and the memories do not need to be arbitrarily addressable. As of the filing date of Lord in 1980, video storage was likely to be an array of analog sensing cells as described in the section entitled "Storage Area" in Kiver et al., *Television Electronics: Theory and Servicing* (8th ed. Van Nostrand Reinhold Co. 1983), pp. 98-103 (copy attached). It is true that the claims do not specifically require a digital memory. However, we do not know what the memory is in Lord. Thus, we do not find the motivation to substitute the particular memory of Lelke in for the memory of Lord. If Lord had an addressable memory, then we agree that substitution of the addressable memory architecture of figure 13 in Lelke would have been obvious, but the examiner has not made this showing in Lord. We conclude that the examiner has failed to establish a *prima face* case of obviousness. The rejection of claims 9, 25, 96, 100, 101, 135, and 140 is reversed.

NOTICE REGARDING ANY REQUEST FOR REHEARING

Any request for rehearing of this decision under 37 CFR § 1.197(b) is limited to points of fact and/or law which appellant believes were overlooked or misapprehended in rendering this decision. New arguments which were not presented in the appeal brief or reply brief will *not* be considered. *See Ex parte Hindersinn*, 177 USPQ 78, 80 (Bd. App. 1971) (argument advanced in petition for reconsideration not advanced in the brief or the reply brief are not properly before us); *cf. Pentax Corp. v. Robison*, 135 F.3d 760, 762 (Fed. Cir. 1998) (citing cases supporting the proposition that issues not raised before the court are not addressed on rehearing). In any request for rehearing, appellant must state with particularity each point of law or fact he believes was overlooked or misapprehended, must, argue in support of each point, and must refer with particularity to where the argument was made originally in the appeal brief or reply brief.

CONCLUSION

The rejections of claims 1-14, 17, 18, 20, 34, 36, 42-45, 81, 85, 98, 106-114, 116, 119-134, 136, 141, 143, 145,148, and 153-172 under 35 U.S.C. § 112, first paragraph, based on a lack of written description are sustained. The rejections of claims 19, 22-25, 35, 37, 49-52, 82-84, 95-97, 99-105, 115, 117, 118, 135, 137-140, 142, 144, and 149-152 for lack of written description are reversed.

The rejections of claims 1-14, 17, 18, 20, 34, 36, 42-45, 81, 85, 98, 106-114, 116, 119-134, 136, 141, 143, 145-148, and 153-172 under § 112, first paragraph, based on lack

of enablement are sustained. The rejections of claims 19, 22-25, 35, 37, 49-52, 82-84, 95-97, 99-105, 115, 117, 118, 135, 137-140, 142, 144, and 149-152 for lack of enablement are reversed.

The rejections of claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 based on obviousness-type double patenting or *Schneller*-type double patenting are reversed.

The rejection of claims 22, 23, 82-84, 95, 99, 137, and 138 under § 102 is reversed.

The rejection of claims 19, 25, 96, 100, 101, 135, and 140 under § 103 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

/s/ ERROL A. KRASS
ERROL A. KRASS
Administrative Patent Judge

/s/ LEE E. BARRETT
LEE E. BARRETT
Administrative Patent Judge

/s/ PARSHOTAM S. LALL
PARSHOTAM S. LALL
Administrative Patent Judge

BOARD OF PATENT APPEALS AND INTERFERENCES

Appeal No. 2000-2049
Application 08/471,702

Gilbert P. Hyatt
P.O. Box 81230
Las Vegas, NV 89180

APPENDIX E

BOARD OF PATENT APPEALS
AND INTERFERENCES

No. 2000-2049
Application 08/471,702
EX PARTE GILBERT P. HYATT

[Decided: Jan. 23, 2003]

DECISION ON REQUEST FOR REHEARING

Before: KRASS, JERRY SMITH[1], and BARRETT, *Administrative Patent Judges.*

BARRETT, *Administrative Patent Judge.*

Appellant filed a request for rehearing (Paper No. 52) on September 30, 2002, of our decision entered July 30, 2002 (paper No. 50) (pages referred to as "D___").

The request for rehearing is *dismissed* without consideration of the merits.

---

[1] Administrative Patent Judge Parshotam S. Lall, who was on the original panel decision, has retired. There is no problem with substituting a board member. *See In re Bose Corp.*, 772 F.2d 866, 869-870, 227 USPQ 1, 4 (Fed. Cir. 1985) (third signatory replaced original third panel member who resigned shortly after the oral argument).

OPINION

Our original decision expressly notified appellant that any new arguments which were presented for the first time in any request for rehearing will *not* be considered (D56-57):

NOTICE REGARDING ANY REQUEST FOR REHEARING

> Any request for rehearing of this decision under 37 C.F.R. § 1.197(b) is limited to points of fact and/or law which appellant believes were overlooked or misapprehended in rendering this decision. New arguments which were not presented in the appeal brief or reply brief will *not* be considered. *See Ex parte Hindersinn*, 177 USPQ 78, 80 (Bd. App. 1971) (argument advanced in petition for reconsideration not advanced in petition for reconsideration not advanced in the brief or the reply brief are not properly before us); *cf. Pentax Corp. v. Robison*, 135 F.3d 760, 762 (Fed. Cir. 1998) (citing cases supporting the proposition that issues not raised before the court are not addressed on rehearing). In any request for rehearing, appellant must state with particularity each point of law or fact he believes was overlooked or misapprehended, must argue in support of each point, and must refer with particularity to where the argument was made originally in the appeal brief or reply brief.

The request for rehearing ignores the requirements set forth in the last sentence. In particular, it fails to point out where the arguments in the request for rehearing were made originally in the appeal brief or the

reply brief. Thus, appellant has not shown that arguments in the brief or reply brief were overlooked or misapprehended and that the arguments are not new arguments.

The examiner's final rejection specifically identified imitations in the claims that were without written description support. On appeal, appellant's only arguments were that words in the various limitations appear in the specification, as evidence by Table 1, which was not deemed persuasive of written description support (D25 § 3; D26-27 § 4; D28 § 5; D32 § 7; D34 § 9; D35 § 10; D35-37 § 11; D38-39 § 12). Appellant now attacks our decision with extensive new arguments about how the disclosure can be interpreted to satisfy the claim limitations. Appellant also makes new arguments about the "making a product" limitations. Since the final rejection expressly identified the limitations without written descriptive support, appellant could have presented the arguments earlier and cannot contend that he is merely responding to new rationale in our opinion.

This panel spent three weeks considering the 238 page specification, the 42 drawing figures, the 128 page appeal brief, and the 64 page reply brief as applied to 54 independent claims and 63 dependent claims in writing our original decision. Now, on request for rehearing, after receiving a decision stating why his arguments were not persuasive, appellant wants us to consider 51 pages of a new document.

Our choices are to either consider the new arguments on the merits or refuse to consider the arguments because they were not timely presented. In this case, appellant was clearly notified in the final rejection of the limitations that the examiner found to be without writ-

ten description and, thus, there is no reason why the arguments now presented could not have been presented in the appeal brief or the reply brief. Appellant is an experienced *pro se* applicant and a registered patent agent who has prosecuted many patent applications (including appeals to the Board, the Court of Customs and Patent Appeals, and the U.S. Court of Appeals for the Federal Circuit) for over 30 years and who should be familiar with how to write an appeal brief. Appellant, although appearing *pro se*, was assisted at the oral hearing by a former member of the Board of Patent Appeals and Inferences. Lastly, appellant was expressly warned in our decision that the request for rehearing should not include new arguments. For these reasons, we refuse to consider the request for rehearing on the merits. Considering the new arguments would condone appellant's failure to argue the errors to the examiner and the Board in the first instance.

The request for rehearing is *dismissed* without consideration of the merits.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

DISMISSED

/s/ ERROL A. KRASS
ERROL A. KRASS
Administrative Patent Judge

/s/ JERRY SMITH
JERRY SMITH
Administrative Patent Judge

/s/ LEE E. BARRETT
LEE E. BARRETT
Administrative Patent Judge

BOARD OF PATENT APPEALS
AND INTERFERENCES

APPENDIX F

Table-1

REPRESENTATIVE TERMINOLOGY	NOTES[22]	OCCURRENCES	REPRESENTATIVE CITES PAGE(S)
access	A	>100	25-83, 128-164
address	A	>500	25-83, 128-164
block	A	>80	25-83, 128-164
boundary		=3	14, 41
compress		=4	23
data compressed		=1	23
decompressed		=1	23
frequency (FFT)	C	=7	33-34
graphic	D	>20	9-14, 214-230
image		>50	50-55
information		>100	THROUGHOUT
input		>200	THROUGHOUT
memory	A	>400	25-83, 128-164
pixel		>300	THROUGHOUT
processor		>50	85-98
quantization	E	>100	231-236
read	A	>50	25-83, 128-164
simultaneous		>8	36, 45, 46, 50
smoothing		=1	232
spatial	B	>20	15-24, 231-236
vector	D	>50	9-14, 214-230
video		=8	77, 166, 168-171
weight	F	>100	162-164
write	A	>100	25-83, 128-164

[22] Each note is discussed below.

APPENDIX G

UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF COLUMBIA

Civil Action No. 03-00901 (HHK) ECF

GILBERT P. HYATT, PLAINTIFF

v.

HON. JAMES E. ROGAN, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE, DEFENDANT

Filed: Jan. 28, 2004

DECLARATION OF GILBERT P. HYATT IN SUPPORT OF HIS OPPOSITION TO DEFENDANT'S MOTION FOR SUMMARY JUDGMENT

I, Gilbert P. Hyatt, declare as follows:

1. I am the applicant for U.S. Patent Application Serial No. 08/471,702 ("'702 application"), the inventor of the inventions claimed therein, and the plaintiff in this action.

2. I am an individual inventor, entrepreneur, and businessman. My patenting activities reflect the importance I place on my research and development, and on obtaining patent protection for my resulting inventions.

The numerous applications I have filed with the U.S. Patent and Trademark Office ("PTO") reflect my life's work in developing innovations and improvements in, among others, the field of computer technology. The PTO has recognized my inventive efforts by issuing over sixty patents in my name, including patents for the microcomputer.

BACKGROUND

3. I received a Bachelor of Science Degree in electrical engineering from the University of California in 1959 and a Master of Science Degree in electrical engineering from the University of Southern California in 1965. I worked in the aerospace industry on various types of systems including missile, aircraft, spacecraft, guidance, fire control, computer, and other types of systems.

4. I worked for the Boeing Aircraft Company, North American Aviation, Hughes Aircraft Company, and Teledyne Systems Company as an Electrical Engineer during the period 1959 to 1968, advancing to the position of Head of Computer Design at the Teledyne Advanced Systems Division. In 1968, I founded Micro Computer Inc. and continued as Vice President of Engineering. In 1971, I founded Digital Nutronics Corp., an aerospace consulting firm, where I continued as President and Consulting Engineer through the mid-1980s. I spent most of this 25-year career designing computer hardware and programming digital computers for aerospace and commercial systems. In the early 1980s, I designed, built, programmed, checked out, and demonstrated the "experimental system" disclosed in the instant patent disclosure.

5. I am a self-taught Patent Agent. I became registered as a Patent Agent with the PTO in the mid-1970s and I have prepared and prosecuted the more than sixty patents that have issued to me.

6. In 1968, I formed my first company, Micro Computer Inc., and developed the first Micro Computer on which I hold various patents. At that time I established my first research and development laboratory, in my home, where I designed, built, and demonstrated my Micro Computer. From the early 1970s and into the mid-1980s I worked as a consultant to self-finance my ongoing research and development efforts. I established research and development laboratories in my homes during this period, and I designed, built, and demonstrated various technologies, including hardware and software. I also designed, built, and demonstrated the experimental system disclosed in the '702 application in my home. Except for a period in 1969 to 1971 in which my company—Micro Computer, Inc.—received venture capital financing to help commercialize some of my technologies, all of my research and development activities were performed without any outside financing or government grants or subsidies.

7. My patent disclosures are large because I actually reduced-to-practice embodiments of my inventions and I incorporate much of the theoretical, design, and construction documentation, including hardware and software, into my patent applications. This is to aid an artisan so that he/she would be able to practice my inventions with a minimum of experimentation. My patent disclosures are also large because I disclose various uses and applications of my technologies so that an artisan

would better understand how to use and apply my technologies.

8. Because of my educational and professional background and experience, as well as my skill in the art of the technology of my patent applications, I believe I am qualified to speak to what the disclosure of my '702 application (and the associated materials) would have made clear to those of ordinary skill in the art at the time the application was filed.

THE '702 APPLICATION

9. I am and have been aware of the GATT legislation that included special incentives to inventors to file patent applications. I filed the '702 application in accordance with that law. I have since learned that many others have benefitted from this law. In particular, I am informed that more than 50,000 patent applications were filed in the nine-day period prior to the June 8, 1995 cut-off. The PTO called this the "bubble" because of the increased filings.

10. I filed more than twenty patent claims in the '702 application and, in accordance with the PTO rules, duly paid the PTO fees required for filing "excess" patent claims.

11. I reduced-to-practice and disclosed in the '702 application an experimental system embodiment. The application provides a top-down disclosure from the top level of block diagrams *(e.g.*, Figs. 1 and 6A) (901-F-252 and -257) down to detailed schematic diagrams *(e.g.*, Figs. 6B to 6AH) (901-F-258 to -290). Such schematic diagrams disclose the wiring of, and enable the practice of, the experimental system embodiment. Further, the text portion of the disclosure describes in detail how the

design works and how the design is interconnected together, to a large degree, component-by-component and wire-by-wire. I designed the working experimental system, was proud of it, and wanted to be sure that it was properly understood and appreciated.

12. I am offended that the PTO accuses me of being a "submarine" applicant. I am a *bona fide* inventor (indeed, the PTO has acknowledged as much by issuing over sixty patents in my name) and have endeavored to file my patent applications in accordance with all applicable patent laws, regulations, and PTO rules. I claimed all of my inventions in good faith. I do not believe that any of my "patent-filing practices" are illegal, improper, or otherwise inappropriate.

13. I have read the Memorandum of Points and Authorities In Support of Defendant's Motion for Summary Judgment filed by the PTO in this case. In its motion, the PTO implies that I failed to present any arguments regarding the written description rejections in my appeal brief. I disagree. In my appeal brief, I presented arguments that the claimed inventions were supported by the disclosure of the '702 application. In particular, TABLE-1, its associated notes, and its associated arguments point one skilled in the art to the location of the relevant disclosure regarding the limitations questioned by the Examiner. In my opinion, this was sufficient to identify to one skilled in the art the written description support for the challenged claim limitations. In addition, Exhibit-3 informs one skilled in the art which limitations are found in which claims, and Exhibit-4 identifies certain information known to one skilled in the art at the time the application was filed. From the '702 disclosure, one skilled in the art would have been informed

that I was in possession of the claimed inventions at the time the application was filed.

14. In the Appeal Brief and the Reply Brief, I presented arguments that neither the written description rejections nor the enablement rejections establish a *prima facie* case (901A-F-0841-0844, 0854, 0858, and 1300-1302); that the product claims were adequately described and enabled (901A-F-0836-0840); and that the application discloses extensive relevant details of the "experimental system" (901-F-0816-0820, 0830-0831, 0845-0851, and 1315-1316).

15. In the Reply Brief, I responded to the arguments presented in the Examiner's Answer. I specifically referred to the basis for the disputed claim limitations in the disclosure; I addressed the TABLE-1 evidence (particularly the detailed "NOTES" to TABLE-1) that were initially addressed in the Appeal Brief; and I also addressed the "product" claims (901-F-1319-1325). Thus, there was a discussion of TABLE-1 by both the Examiner and me during the appellate briefing (901A-F-1195 to -1196; 901A-F-833 to -834; 901A-F-1321 to -1323).

PTO DELAYS

16. I currently have **[REDACTED]** of patent applications pending before the PTO. For some reason, the PTO has been very dilatory in examining my applications in each phase of the process.

17. The PTO has suspended and delayed the examination of many of my applications currently pending at the PTO. For example, the PTO on its own has suspended and delayed examination in over **[REDACTED]** of my pending patent applications. Specific examples of these suspensions and delays by the PTO are discussed below.

18. In one of these suspended applications (Serial No. [REDACTED]), over 80 months have passed since my last submission to the PTO without a response from the PTO *(e.g.,* an "Office Action"). In two other suspended applications (Serial Nos. [REDACTED] and [REDACTED]), over 70 months have passed since my last submission to the PTO without a response from the PTO. In two other suspended applications (Serial Nos. [REDACTED] and [REDACTED]]), over 60 months have passed since my last submission to the PTO without a response from the PTO. With respect to the remainder of these more than [REDACTED] suspended applications, an average of more than 20 months have passed since my last submission without a response from the PTO.

19. With respect to a group of [REDACTED] of my appealed applications (Serial Nos. [REDACTED], the PTO has delayed the processing of these patent applications on appeal to the Board of Patent Appeals and Interferences ("Board") for an average of 36 months. None of these applications has been heard by the Board. First, the PTO delayed in generating an Examiner's Answer (the name given to the Examiner's opposition brief) in response to my timely filed Appeal Briefs. While under the PTO's rules an Examiner's Answer should issue within two months, I waited an average of 18 months (and as long as 35 months in Serial [REDACTED]) before receiving an Examiner's Answer. The delays following the filing of my Appeal Brief were so long that, for each of the applications, I had to petition the Commissioner to intervene to direct the Examiner to issue an Examiner's Answer. Then, after further PTO delay lasting on average 12 months following the date of my Petition, I finally received Examiner's An-

swers in these applications. I then timely filed my Reply Briefs in these [REDACTED] applications and have been waiting an average of over 18 months to the present date for a hearing before the Board.

20. The PTO also has delayed the examination process by causing me to brief appealed applications and then vacating the appeals and reopening examination. This has resulted in delays by the PTO of over five years in some of my applications. For example, I prosecuted [REDACTED] applications to Final Actions, filed Notices of Appeal and Appeal Briefs in each application, and waited for the Examiner's Answers, which were due in two months (Serial Nos. [REDACTED]). After waiting as long as six months *(e.g.,* in Serial No. [REDACTED]), the Examiner in each of these [REDACTED] applications vacated the appeals (thereby wasting my effort and expense in briefing these cases), reopened prosecution, and started the examination process all over again. I again prosecuted these applications to Final Actions, filed Notices of Appeal and Appeal Briefs in each application, and waited for the Examiner's Answers. This "double" appeal process took an average of 31 months from the first Appeal Brief to the second Appeal Brief and an average of another 35 months until hearings at the Board. Two of these applications (Serial Nos. [REDACTED]) have still not been heard by the Board.

21. With respect to another group of [REDACTED] of my appealed applications, the Examiners vacated the appeals and issued new Office Actions after a significant delay (Serial No. [REDACTED]). I initially prosecuted these applications to Final Action, filed Notices of Appeal and Appeal Briefs in each application, and waited

for the Examiner's Answers. I waited more than 55 months with respect to two applications (Serial Nos.[REDACTED]) and waited an average of over 18 months in all [REDACTED] applications before the PTO vacated the appeals in these cases and issued new Office Actions.

22. In another of my appealed applications (Serial No. [REDACTED]), I prosecuted the application to Final Action, filed a Notice of Appeal and an Appeal Brief, and waited for the Examiner's Answer. After 42 months, the Examiner vacated the appeal (thereby wasting my effort and expense in briefing this case), reopened prosecution, and started the process all over again. I later filed a second Notice of Appeal and Appeal Brief in the application and the PTO again withdrew the appeal and reopened prosecution about eight months later.

23. There are other examples of the PTO's delay. For example, one of my applications (Serial No. [REDACTED]) had been fully examined and was in the process of issuing in early 1997 when the PTO withdrew this application from issuance. Almost seven years have passed without an Office Action from the Examiner.

24. Another application (Serial No. [REDACTED]) had been fully examined and was ready for issuance in 1997. Then, after delaying five and one-half years, the Examiner reopened prosecution and started the examination process over again.

25. In October 1999, one of my applications (Serial No. [REDACTED]) had 94 of 97 claims "allowed" (there were no rejections on these 94 claims). I filed a response to the three rejected claims and made no changes to any of the allowed claims. Nevertheless, the PTO delayed any action in the case for another two years. Then,

in June 2001, all of the previously "allowed" claims were rejected, thereby starting the examination process over again.

26. In March 1997, all of the claims pending in one of my applications (Serial No. [**REDACTED**]) were "allowed," yet the PTO has taken no action in this case for the past seven years.

WRITTEN DESCRIPTION SUPPORT FOR THE "VECTOR PROCESSOR" LIMITATION

27. I believe the '702 disclosure provides adequate written description support for the claimed "vector processor" limitation identified by the PTO.

28. Page 10 of the specification states:

> A graphics processor architecture can be implemented with a (sic) address generator and control logic generating graphics vectors for storing into image memory. Image memory can then be scanned out, such as in a raster scan form to refresh a display.

(901A-F-12.) From the '702 disclosure, one skilled in the art would be informed that "a graphics processor architecture" that generates "graphics vectors" could also be referred to as a "vector processor" or "two dimensional vector processor," as that phrase is found in the claims. One skilled in the art would also be informed that the same processor could be described as a "block processor."

29. The "vector processor" is further illustrated in detail in Figs. 6O, 6P, 6Q, and 6R, and, as identified in TABLE-1 under "vector", is discussed at pages 9-14 and 118-127 of the specification.

30. The "graphics processor architecture" described on page 10 of the specification corresponds to the address generator 115B of Fig. 1, and "two dimensional vector information" reads on "graphics commands".

31. The '702 disclosure supports a vector processor acting "in response to the two dimensional vector information." Page 10 of the specification states:

> One arrangement of the graphics system of the present invention is shown in Fig 1. Supervisory processor 115A loads graphics commands into address generators 115B. Address generators 115B generate addresses of graphics vectors for loading into image memory 115C and for raster scanning image memory 115C. The raster scan addresses scan-out the image in image memory 115C through the CRT interface 115D to refresh CRT 115E.

(901A-F-11). One skilled in the art would be informed that "two dimensional vector information" reads on "graphics commands" as described above and that "graphics processor architecture" (which supports the claimed "vector processor") corresponds to the address generator 115B of Fig. 1. Fig. 1 and page 10 of the specification inform one skilled in the art that the "vector processor" (address generator 115B) acts "in response to" "two dimensional vector information" (graphics commands, loaded into address generator 115B).

32. During re-addressing each of the 64 memory chips reads a byte of video pixel information into an internal data register. These 64 bytes form an accessed block of video pixel information. The address generators subsequently scan out these accessed bytes and

thus generate the output in response to the accessed blocks of video pixel information.

33. A skilled artisan would recognize that the output address generator of Figs. 6O and 6P has essentially the same construction as the input address generator of Figs. 6Q and 6R.

34. A skilled artisan would recognize that the address generator of Fig. 6Q and 6R likewise may be used to "scan out" or generate output vectors.

35. The two program listings GRAPH.ASC (901A-F-216 to -218) and LD.ASC (901A-F-219 to -232) n the '702 disclosure explain how to initialize the address generators of Figs. 6O to 6R for both types of operation.

36. The source code for GRAPH.ASC is set forth in full at pages 214-230 with annotations that explain how to use the address generators for both raster scan and vector scan operations.

37. It is clear to me from the Board's decision in this case that it interpreted the recited "two dimensional vector processor" to read on the "supervisory processor"; the recited "vector generator" to read on "[input] address generators of figures 6Q and 6R"; and the recited "accessing circuit" to read on "[output] address generators of figures 6O and 6P."

38. One skilled in the art would read "two dimensional vector processor" on the output address generators 6O and 6P; "vector generator" on the supervisory processor; and "accessed blocks of video pixel information" on the pixel data stored in the internal data registers of the 64 memory chips.

39. I believe, as a consequence of the Board's misreading of the '702 disclosure and application claims, that the Board concluded that "we find no written description for a processor coupled to and performing the 'generating' function 'in response to' the vector information as well as in 'response to' image information from the image memory." One skilled in the art would read "two dimensional vector processor" on the output address generators 6O and 6P; "vector generator" on the supervisory processor; and "accessed blocks of video pixel information" on the pixel data stored in the internal data registers of the 64 memory chips.

WRITTEN DESCRIPTION SUPPORT FOR THE "DATA COMPRESSION" LIMITATION

40. I believe the '702 disclosure provides adequate written description support for the claimed "data compression" limitation identified by the PTO.

41. The recited data compression is provided by the FTR.ASC program, which has a complete source code listing in the disclosure (901A-F-233 to -238) and which can be used for both pre-processing and post-processing. This "source code listing" is the actual computer language program that I programmed, which was compiled and then executed with the computer to perform the programmed functions.

42. The filter processor is shown in Fig. 5A (901A-F-254).

43. The teaching that the FTR.ASC program emulates a hardware filter processor directs one skilled in the art to interchangeably use either the hardware processor of Fig. 5 or the FTR.ASC program to perform the post processing function. One skilled in the art would

recognize that the Fig. 5 post processor and the FTR.ASC program perform substantially the same function and that the teaching that the FTR.ASC program emulates a hardware filter processor is a teaching that the post processor can be implemented with either the FTR.ASC program or the hardware post processor, thus providing data compression for data read from image memory as recited in the claims. The following provision in the disclosure teaches the equivalency of implementing the filter processor of Fig. 5A with either the FTR.ASC software program or hardware.

> Fig. 5A shows an arrangement of a display system. Address generator 520A generates pixel addresses to access a plurality of pixels, such as a 9-pixel kernel 520H, from image memory 520B. Pixel information can be latched in registers to provide parallel pixel words or can be accessed sequentially as provided with the BASIC PROGRAM LISTING FTR.ASC herein. Weight table 520C supplies a plurality of kernel weights appropriate to spatial filtering of the pixel kernel, such as a kernel of 9-weights 520I, from weight table 520C. Weight information can be latched in registers or in the weight table to provide parallel pixel words or can be accessed sequentially as provided with the BASIC PROGRAM LISTING FTR.ASC herein.

(901A-F-18).

44. Three different TABLE-1 entries under (1) compress, (2) data compressed and (3) decompressed, all directed the PTO to page 23 of the disclosure. This is the page which the Board said explained that the FTR.ASC program, which the Board recognized as having data compression, emulates a hardware filter proces-

sor. Thus, the key disclosure that the FTR.ASC program can be used interchangeably with the hardware filter processor in the recited post processing location is at the page that is listed in TABLE-1 as a "Representative Cite."

45. In addition to the Board recognizing that the FTR.ASC program provides data compression, the program is disclosed in detail in the disclosure. A complete source code listing with extensive annotations is provided at pages 231-236 (901A-F-233 to -238). In addition, a complete flow chart is provided in Fig. 7 (901A-F-293) and operation of the filter processor is explained in detail in a section entitled "Description of Fig. 7 and the FTR.ASC Listing" at pages 18 to 22 of the disclosure (901A-F-20 to -24). The first sentence of this section contains an additional suggestion to one skilled in the art to interchangeably use either the hardware or software filter processor, stating:

> A filter processor can be emulated in software to illustrate operation of a hardware configuration.

(901A-F-20).

46. In summary, while the Board recognized that the disclosure teaches that the program FTR.ASC provides data compression and emulates the hardware post processor, it failed to consider the result of substituting the program for the hardware post processor. One skilled in the art would recognize in the disclosure the direction to make this substitution and would thus find in the disclosure a teaching of compressing data stored in the image memory as recited in the claims.

WRITTEN DESCRIPTION SUPPORT FOR THE "BLOCK BOUNDARY SMOOTHING" LIMITATION

47. I believe the '702 disclosure provides adequate written description support for the claimed "block boundary smoothing" limitation identified by the PTO.

48. Block boundary smoothing is provided by the FTR.ASC program. The program divides an image into 8 stripes with each stripe containing a block of pixel data. Each stripe is stored in a different file and special operations are provided at the block boundaries to provide smoothing in response to data from more than one file or stripe.

49. TABLE-1 of the Appeal Brief specifically directed the Board to the program FTR.ASC for a teaching of block boundary smoothing (901A-F-832). For example, TABLE-1 lists page 232 as a representative cite under the word "smoothing". This page of the disclosure, which actually contains the word "smoothing," is a portion of the source code listing for filter processor program FTR.ASC.

50. One skilled in the art would recognize that the filter program smoothes image data by recalculating the value of each pixel as a function of the original pixel value, the value of the 8 pixels surrounding the original pixel and a weighting function. The disclosure teaches that special processing is provided at stripe (block) boundaries:

> The filtering operation accesses a kernel of pixels surrounding the center pixel and consequently overlaps stripes for the first line and the last line in a stripe.

(901A-F-26).

51. Section 9 of the Board decision recognized that the FTR.ASC program even contained the word "smoothing" (901A-F-1,616), but considered only the 64 blocks of pixels stored by the image memory as a possible block of data. However, one skilled in the art would recognize that the 8 stripes into which an image is divided for filtering by the filter program also constitute blocks of data.

WRITTEN DESCRIPTION SUPPORT FOR THE "QUANTIZATION" LIMITATION

52. I believe the '702 disclosure provides adequate written description support for the claimed "quantization" limitation identified by the PTO.

53. In particular, the disclosure informs one skilled in the art to use the FTR.ASC program to implement the Fig. 5A filter processor. Pages 231-236 of the specification, which I identified to the PTO in TABLE-1 during the appellate briefing as support for "quantization", provide the source code for the FTR.ASC program, which contains the expression:

WRR1%=WRR2%*WTS2

(901A-F-236 at line 1260.) This expression means multiply the value of WRR2% by WTS2, which is set to a fraction (a floating point number) at lines 390 and 400 of the program, and store the result in variable WRR1% as an integer value. This represents "quantization," as even the Board agrees. (901A-F-1,619.)

54. In its analysis, the Board erroneously disregarded the FTR.ASC program on the mistaken belief that

the disclosure of the program limits the program to being used only as a preprocessor program:

> The program FTR.ASC emulates a hardware filter processor (spec, at 18, lines 2- 3) and demonstrates offline filtering and *preprocessing* (before the image data is loaded into memory) (spec, at 23, lines 20-22).

(901A-F-l,599) (emphasis added).

55. However, the FTR.ASC program can be used to implement the post-processor of Fig. 5A. One skilled in the art would recognize that the Fig. 5A post-processor and the FTR.ASC program both perform the function of a 9-pixel kernel filter processor. One skilled in the art would further recognize that the teaching that the FTR.ASC program emulates the filter processor is a teaching of the implementation of the filter process with the FTR.ASC program, thus providing quantization while processing data read *from* image memory as recited in the claims. Accordingly, one skilled in the art would recognize that the disclosure demonstrates adequate written description support for the quantization feature.

WRITTEN DESCRIPTION SUPPORT FOR THE "MAKING A PRODUCT" LIMITATION

56. I believe that one skilled in the art would find that the '702 disclosure provides adequate written description support for the claimed inventions having the "making a product" limitation identified by the PTO.

57. I believe that one skilled in the art would find that the analog display image signal as disclosed in the '702 disclosure constitutes a product.

58. I believe that one skilled in the art would find that a display image as disclosed in the '702 disclosure constitutes a product.

59. Claim 81 recites the output image information as being generated in response to the two dimensional processed image information, *i.e.*, the information from the spatial processor shown in Fig. 5. The analog display image signal is not the same signal as the output image information recited in claim 81.

60. An electrical signal is made up of a concentration of electrons that varies with the information content of the signal. The electrons are physical and the structure may change as the information content of the signal changes, but that does not mean that the signal has no structure. Further, each electron is a substance *(i.e.*, matter) and since a signal is comprised of a large number of electrons, a signal is a composition of matter. One skilled in the art would recognize that the disclosure supports making a product in response to output image information as recited in the claim.

* * * * *

I declare under penalty of perjury that the foregoing is true and correct. Executed on January 28, 2004.

/s/ GILBERT P. HYATT
GILBERT P. HYATT

APPENDIX H

35 U.S.C. 145 provides:

An applicant dissatisfied with the decision of the Board of Patent Appeals and Interferences in an appeal under section 134(a) of this title may, unless appeal has been taken to the United States Court of Appeals for the Federal Circuit, have remedy by civil action against the Director in the United States District Court for the District of Columbia if commenced within such time after such decision, not less than sixty days, as the Director appoints. The court may adjudge that such applicant is entitled to receive a patent for his invention, as specified in any of his claims involved in the decision of the Board of Patent Appeals and Interferences, as the facts in the case may appear and such adjudication shall authorize the Director to issue such patent on compliance with the requirements of law. All the expenses of the proceedings shall be paid by the applicant.

OPPOSITION BRIEF

RECORD
AND
BRIEFS

Supreme Court, U.S.
FILED
MAY 27 2011
OFFICE OF THE CLERK

No. 10-1219

IN THE
Supreme Court of the United States

DAVID J. KAPPOS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR, UNITED STATES PATENT AND TRADEMARK OFFICE,
Petitioner,

v.

GILBERT P. HYATT,
Respondent.

On Petition for a Writ of Certiorari to the United States Court of Appeals for the Federal Circuit

BRIEF IN OPPOSITION FOR RESPONDENT

MICHAEL L. MARTINEZ
CROWELL & MORING LLP
1001 Pennsylvania Ave., N.W.
Washington, D.C. 20004
(202) 624-2500

GREGORY L. ROTH
5712 Parkwest Circle
La Palma, California 90623
(714) 723-6871

AARON M. PANNER
Counsel of Record
KELLOGG, HUBER, HANSEN, TODD, EVANS & FIGEL, P.L.L.C.
1615 M Street, N.W.
Suite 400
Washington, D.C. 20036
(202) 326-7900
(apanner@khhte.com)

May 27, 2011

Library of Congress
Law Library

QUESTIONS PRESENTED

1. Whether the Federal Circuit correctly decided that a patent applicant who files a "civil action" under 35 U.S.C. § 145, rather than an "appeal" under § 141, may generally introduce new evidence, in accordance with the Federal Rules of Civil Procedure and the Federal Rules of Evidence, to show that the "applicant is entitled to receive a patent."

2. Whether the Federal Circuit correctly reaffirmed existing law holding that a district court in an action under § 145 adjudicates factual issues *de novo* in cases where an applicant introduces new evidence that was not before the Patent and Trademark Office, a standard that the government did not challenge before the court below.

TABLE OF CONTENTS

Page

QUESTIONS PRESENTED i

TABLE OF AUTHORITIES iii

INTRODUCTION 1

STATEMENT OF THE CASE 3

REASONS FOR DENYING THE PETITION 11

I. THE FEDERAL CIRCUIT'S RULING THAT NEW EVIDENCE IS ADMISSIBLE IN ACTIONS UNDER § 145 DOES NOT MERIT REVIEW 11

A. The Federal Circuit's Ruling On Admission Of Evidence Is Correct 11

B. The Decision Below Is Of Limited Importance And Makes Policy Sense 23

II. THE FEDERAL CIRCUIT'S LIMITED RULING ON STANDARD OF REVIEW IS NOT BEFORE THE COURT AND IS PLAINLY CORRECT 28

A. The Government, Arguing Only Against Admission Of New Evidence, Did Not Contest Existing Federal Circuit Law Requiring *De Novo* Determination Where New Evidence Is Admitted 28

B. The Federal Circuit's *De Novo* Standard When New Evidence Is Admitted Is Correct 29

III. THE COURT SHOULD NOT HOLD THE PETITION 30

CONCLUSION 31

TABLE OF AUTHORITIES

Page

CASES

Appert v. Brownsville Plate Glass Co., 144 F. 115 (C.C.W.D. Pa. 1904) 17

Armstrong v. De Forest, 13 F.2d 438 (2d Cir. 1926) 17

Barrett Co. v. Koppers Co., 22 F.2d 395 (3d Cir. 1927) 8, 21

Bernardin v. Northall, 77 F. 849 (C.C.D. Ind. 1897) 17

Berry v. Robertson, 40 F.2d 915 (D. Md. 1930) 17

Boucher Inventions v. Sola Elec. Co., 131 F.2d 225 (D.C. Cir. 1942) 22

Bragdon v. Abbott, 524 U.S. 624 (1998) 18-19

Butler v. Shaw, 21 F. 321 (C.C.D. Mass. 1884) 17

Butterworth v. United States ex rel. Hoe, 112 U.S. 50 (1884) 16, 17

California Research Corp. v. Ladd, 356 F.2d 813 (D.C. Cir. 1966) 23, 24

Central Ry. Signal Co. v. Jackson, 254 F. 103 (E.D. Pa. 1918) 17

Chandler v. Roudebush, 425 U.S. 840 (1976) 11, 12

Christie v. Seybold, 55 F. 69 (6th Cir. 1893) 17

Citizens To Preserve Overton Park, Inc. v. Volpe, 401 U.S. 402 (1971) 10, 13

Consolo v. Federal Maritime Comm'n, 383 U.S. 607 (1966) 13

Curtiss Aeroplane & Motor Corp. v. Janin, 278 F. 454 (2d Cir. 1921) 17

Custis v. United States, 511 U.S. 485 (1994) 15

DeSeversky v. Brenner, 424 F.2d 857 (D.C. Cir. 1970) 23, 24

Dickinson v. Zurko, 527 U.S. 150 (1999) 1, 2, 13, 14, 18, 28, 29

Dowling v. Jones, 67 F.2d 537 (2d Cir. 1933) 22

Florida Power & Light Co. v. Lorion, 470 U.S. 729 (1985) 13

Fregeau v. Mossinghoff, 776 F.2d 1034 (Fed. Cir. 1985) 10, 28

Gandy v. Marble, 122 U.S. 432 (1887) 12, 17

General Elec. Co. v. Steinberger, 208 F. 699 (E.D.N.Y. 1913), *aff'd*, 214 F. 781 (2d Cir. 1914) 17

Globe-Union, Inc. v. Chicago Tel. Supply Co., 103 F.2d 722 (7th Cir. 1939) 22

Greene v. Beidler, 58 F.2d 207 (2d Cir. 1932) 22

Hien, In re, 166 U.S. 432 (1897) 17

Hoover Co. v. Coe, 325 U.S. 79 (1945) 19, 20

Mazzari v. Rogan, 323 F.3d 1000 (Fed. Cir. 2003) 28

McCarthy v. Madigan, 503 U.S. 140 (1992) 23

McKart v. United States, 395 U.S. 185 (1969) 23

Merrill Lynch, Pierce, Fenner & Smith, Inc. v. Curran, 456 U.S. 353 (1982) 19

Minnesota Mining & Mfg. Co. v. Carborundum Co., 155 F.2d 746 (3d Cir. 1946) 21, 22

Morgan v. Daniels, 153 U.S. 120 (1894)....17, 18, 29, 30

NBC v. United States, 319 U.S. 190 (1943) 13

Nichols v. Minnesota Mining & Mfg. Co., 109 F.2d 162 (4th Cir. 1940) 22

Schilling v. Schwitzer-Cummins Co., 142 F.2d 82 (D.C. Cir. 1944)..... 21-22

Sims v. Apfel, 530 U.S. 103 (2000) 23

Smith v. Prutton, 127 F.2d 79 (6th Cir. 1942)..... 22

Sosa v. Alvarez-Machain, 542 U.S. 692 (2004)..... 15

Squire, In re, 22 F. Cas. 1015 (C.C.E.D. Mo. 1877)..... 17

Tagg Bros. & Moorhead v. United States, 280 U.S. 420 (1930) 13

United States v. Carlo Bianchi & Co., 373 U.S. 709 (1963) 13

United States v. United Foods, Inc., 533 U.S. 405 (2001) 29

Western Elec. Co. v. Fowler, 177 F. 224 (7th Cir. 1910)..... 22

STATUTES, REGULATIONS, AND RULES

Act of Mar. 2, 1927, ch. 273, § 11, 44 Stat. 1335, 1336-37.....18, 20

Act of July 19, 1952, ch. 950, 66 Stat. 792..... 20

Act of Dec. 12, 1980, Pub. L. No. 96-517, 94 Stat. 3015..... 20

Administrative Procedure Act, 5 U.S.C. § 701 *et seq.* 10, 13

Civil Rights Act of 1964, Title VII, 42 U.S.C. § 2000e *et seq.* 12

§ 706, 42 U.S.C. § 2000e-5 12

Hobbs Act, 28 U.S.C. § 2341 *et seq.* 13

Packers and Stockyards Act, § 316, 7 U.S.C. § 217 13

Patent Act (35 U.S.C.):

35 U.S.C. § 141 ..... 1, 9, 11, 14, 24

35 U.S.C. § 144 14

35 U.S.C. § 145 ..... 1, 2, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 19, 20, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31

35 U.S.C. § 306 20

29 U.S.C. § 722(c)(5)(J)(i) 14

42 U.S.C. § 300e-9(d)(3) 14

Rev. Stat.:

§ 4911 16

§ 4915 ..... 9, 16, 18, 20, 22

37 C.F.R. § 1.114(e)(2) 25

Fed. R. Evid.:

Rule 402 13

Rule 1101(b) 13

LEGISLATIVE MATERIALS

H.R. Rep. No. 96-1307(I) (1980), *reprinted in* 1980 U.S.C.C.A.N. 6460 20

Procedure in the Patent Office: Hearing Before the S. Comm. on Patents, 69th Cong. (1926) 20

S. Rep. No. 82-1979 (1952) 20

To Amend Section 52 of Judicial Code and Other Statutes Affecting Procedure in the Patent Office: Hearing Before the H. Comm. on Patents, 69th Cong. (1926) 18, 19, 20

OTHER MATERIALS

Brief for the United States as Amicus Curiae Supporting Respondents, *Microsoft Corp. v. i4i L.P.*, No. 10-290 (U.S. filed Mar. 18, 2011)..... 21

4 Donald S. Chisum, *Chisum on Patents* (2005)..... 24

P.J. Federico, *Evolution of Patent Office Appeals*, 22 J. Pat. Off. Soc'y 838 (1940) 19

Manual of Patent Examining Procedure (8th ed. rev. 2008) 4

Giles S. Rich, *Outline of Patent Law and Procedure*, 3 J. Fed. Cir. Hist. Soc'y 61 (2009) 19

2A Norman J. Singer, *Statutes and Statutory Construction* (6th rev. ed. 2000)..... 15

2 Thomas A. Street, *Federal Equity Practice* (1909) 16

INTRODUCTION

The government's petition seeks to present two questions for review. The first relates to the standard for the admission of new evidence in a civil action under 35 U.S.C. § 145; the second relates to the standard for district court fact-finding in cases under that provision after new evidence is admitted. Neither question warrants review in this case; the second question is not properly presented at all.

First, the Federal Circuit's determination that new evidence is generally admissible in actions under § 145 leaves the law where it has stood for 170 years. The language, structure, and history of the statute establish that Congress did not intend to confine plaintiffs to on-the-record review in actions under § 145, but instead provided for admission of new evidence and district court fact-finding – as this Court has recognized. *See Dickinson v. Zurko*, 527 U.S. 150, 163-64 (1999). Section 145, like its predecessors, provides an alternative to appellate review on the Patent and Trademark Office ("PTO") record. To claim that differences between a "civil action" under § 145 and an "appeal" under § 141 create an "unjustified disparity," Pet. 28, is to ignore the statute's clear language. Moreover, the government's concerns about potential abuses are not just speculative but implausible. The integrity of the PTO's application process is protected by built-in constraints on § 145 suits, including the patent applicant's statutory obligation to bear the expense of the civil action and the risk of a negative ruling from the district court.

Second, the question of the appropriate deference to afford to prior PTO findings where a patent applicant introduces new evidence was not argued below and therefore is not properly presented. The Federal

Circuit simply reaffirmed existing precedent governing standard of review in actions under § 145; the government did not challenge those prior Federal Circuit decisions below. In particular, the rule that district courts must find facts *de novo* where new evidence is introduced in an action under § 145 has been the law in the Federal Circuit since 1985. *See* App. 31a. That rule is hardly surprising; it simply reflects the fact that, when there is new evidence that the PTO has not evaluated, there is no prior determination on the record for the district court to review. *See Zurko*, 527 U.S. at 164 ("The presence of . . . new or different evidence makes a factfinder of the district judge."). That determination does not mean that the district court disregards the proceedings before the PTO, as the Federal Circuit explained.

Third, there is no reason to hold the petition for the Court's forthcoming decision in *Microsoft Corp. v. i4i L.P.*, No. 10-290 (argued Apr. 18, 2011). The government effectively concedes that *Microsoft* will have no impact on the first question, which is the only question properly before the Court. As to the second question, because *Microsoft* addresses the weight to be given to a final PTO determination in later infringement litigation between private parties, it cannot affect the Federal Circuit's holding that a district court determines factual issues on a new factual record *de novo* in an action under § 145.

STATEMENT OF THE CASE

1. Plaintiff Gilbert Hyatt filed a patent application in June 1995 describing a data compression system for storing and processing image information. *See* C.A. App. A10402-89. As amended, the application has 117 independent and dependent claims covering both memory systems and a process of operating such systems.

On July 30, 1997, the examiner issued a final office action rejecting all claims for lack of written description and lack of enablement. *See id.* at A10638-56. All claims were also provisionally rejected for double patenting. *See id.* at A10656-60. In addition, numerous claims were rejected on anticipation and obviousness grounds. *See id.* at A10660-62.

For certain claim features, the examiner provided a brief explanation for the written-description rejections. In most cases, however, the examiner provided no explanation; instead, the examiner simply identified a claim feature and stated that the written description provided no support for that feature. For example, the examiner rejected multiple claims that included the feature "a vector processor responsive to an accessed block of video pixel image information and to vector information." *Id.* at A10642. The rejection states without further elaboration that "[t]his feature of the claims is not supported by applicant[']s originally filed specification nor by [the] parent application." *Id.* The examiner took the same approach with respect to nine other groups of claims. *See id.* at A10643-55.

2. Plaintiff appealed the rejection to the Board of Patent Appeals and Interferences ("Board"), filing a 129-page appeal brief. Plaintiff argued, first, that the examiner "has not provided the required objec-

tive reasons" in support of the written-description and enablement rejections. C.A. App. A10824.[1] Plaintiff noted that the specification included "detailed schematic diagrams showing actual commercially available electrical components . . . and even showing component pin designations and wire connections" but that the examiner failed to consider that disclosure as a whole. *Id.* at A10827. Next, plaintiff argued that "[v]arious claims stand rejected . . . based upon unclaimed subject matter" – that is, the examiner rejected claims because features *not* claimed were inadequately disclosed. *Id.* at A10828.

Plaintiff explained that the examiner's rejection had failed to "evaluate[] the numerous occurrences of" the terminology that provided the basis for the rejections. *Id.* at A10830. "The experimental system embodiment described in the specification and shown in the figures represents a detailed disclosure of an actual reduced to practice system." *Id.* "With the extensive memory disclosure (*e.g.*, Spec. at 99-135) and processor disclosure (*e.g.*, Spec. at 87-98, 214-36) . . . , it is unbelievable that the Examiner would object to the disclosure of memory and processor features." *Id.* at A10831.

Plaintiff then provided a table ("Table-1") that listed "representative terminology" related to the examiner's written-description rejections, the number of occurrences, and "representative cites" to the

---

[1] Plaintiff relied on Section 706.03 of the Manual of Patent Examining Procedure (8th ed. rev. 2008), which states that rejections for "lack of proper disclosure . . . should be stated with a full development of the reasons rather than by a mere conclusion coupled with some stereotyped expression." C.A. App. A10823.

specification. *Id.* at A10832. Table-1 was followed by notes elaborating on disclosure of several features.

3. The Board reversed much of the rejection but affirmed written-description and enablement rejections in part. *See* App. 200a-254a; *see also* App. 5a ("Mr. Hyatt prevailed on over 93% of the examiner's rejections at the Board level.").

The Board devoted the bulk of its opinion to the examiner's written-description rejections.[2] In the case of each of the written-description rejections for which the examiner provided some explanation beyond a bare assertion that the feature did not appear in the disclosure, the Board reversed the rejection, either because the specification adequately disclosed the feature or because the examiner's rejection was based on unclaimed subject matter. For the other written-description rejections, the Board affirmed while providing explanations absent from the examiner's rejection.

For example, as noted above, the examiner did not explain what aspect of the feature "vector processor responsive to an accessed block of video pixel image information and to vector information" he found unsupported. *See* C.A. App. A10642 (¶ 13). By contrast, the Board devoted three pages to an explanation of its reasons for affirming. After finding that the written description did provide "support for a processor 'coupled to the accessing circuit and coupled to the vector generator,'" as recited in the claim, the Board stated:

---

[2] The Board stated that it would "treat the enablement rejections as standing or falling together with the written description rejections." App. 240a.

> However, the limitation at issue requires that the processor perform the function of "generating two dimensional processed image information in response to . . . video pixel information . . . and in response to the two dimensional vector information generated by the vector generator." This implies that the "generating" function operates on two kinds of input data: pixel information from memory and vector information. However, the specification describes graphics vectors being generated (strobed) into image memory (e.g. spec. at 11-12), *not* being generated and used by a processor together with accessed pixel data read out from the block image memory, which would require bypassing the block memory. That is, the disclosed processor only controls the vector generator, it does not receive data from it or operate "in response to" it. Since the vector information is stored into the block memory, we find no written description for a processor coupled to and performing the "generating" function "in response to" the vector information as well as "in response to" image information from the image memory.

App. 223a (ellipses in original); *see also* App. 229a-230a (cross-referencing prior discussion).

The Board concluded with a boilerplate notice that "[a]ny request for rehearing . . . is limited to points of fact and/or law which appellant believes were overlooked or misapprehended" and that "[n]ew arguments which were not presented . . . will *not* be considered." App. 252a.

4. Plaintiff filed a rehearing request that provided detailed responses to the explanations the Board had newly offered. For example, in response

to the rejection quoted at length above, plaintiff explained the manner in which the claim limitation at issue read on the disclosure, concluding:

> [B]ecause the vector generation function first accesses a block of image information from image memory and then overlays the block with the vector, the image information written into the image memory is generated in response to both (1) accessed blocks of image information and (2) vector information.

C.A. App. A11656; *see also id.* at A11656-57, A11667-72, A11677-81. Plaintiff provided comparable elaboration with regard to the Board's other new rationales. *See id.* at A11648-85.

The Board refused to consider the request, stating that plaintiff had added new arguments not contained in his prior briefing. The Board stated that "[t]he examiner's final rejection specifically identified [l]imitations in the claims that were without written description support" and that plaintiff's "only arguments were that words in the various limitations appear in the specification." App. 257a. "Appellant now attacks our decision with extensive new arguments about how the disclosure can be interpreted to satisfy the claim limitations .... Since the final rejection expressly identified the limitations without written descriptive support, appellant could have presented the arguments earlier and cannot contend that he is merely responding to new rationale[s] in our opinion." *Id.*

5. Plaintiff filed an action in the U.S. District Court for the District of Columbia against the Director of the PTO pursuant to 35 U.S.C. § 145. In opposition to the Director's motion for summary judgment, plaintiff proffered a declaration explaining

that one of ordinary skill in the art would have found an adequate written description for each of the rejected claims. The district court held that plaintiff had provided no adequate explanation for failing to submit his declaration to the PTO during prosecution; that his failure was "negligent"; and that the evidence would be disregarded. App. 189a. Reviewing the Board's finding on the record before the Board under a "deferential 'substantial evidence' standard," the district court granted summary judgment against plaintiff. App. 189a-190a; *see* App. 190a-198a. Plaintiff's request for reconsideration was denied. *See* C.A. App. A26-32.

6. A divided panel of the Federal Circuit affirmed. The decision held that the district court had properly disregarded plaintiff's declaration because plaintiff had "willfully refused to provide evidence in his possession in response to a valid action by the examiner." App. 139a. The panel majority stated that it was not resolving the question whether a district court could exclude evidence "on grounds other than the type of refusal at issue here and in [*Barrett Co. v. Koppers Co.*, 22 F.2d 395 (3d Cir. 1927)]." App. 140a n.31. Judge Moore dissented, stating that the majority opinion "takes away this patent applicant's fundamental right to a 'civil action to obtain [a] patent' as granted by Congress in 35 U.S.C. § 145." App. 149a (alteration in original).

7. The *en banc* Federal Circuit granted rehearing and reversed. The court noted that § 145 authorizes a "civil action," without placing any special limitations on a plaintiff's right to introduce evidence. App. 12a. Such an action "is distinct from an appeal, in which the applicant would be limited to the record before the Patent Office"; the "plain language" of the

statute provides that "this civil action does not merely afford judicial review of agency action" but "directs that the district court may 'adjudge that such applicant is entitled to receive a patent for his invention . . . as the facts in the case may appear.'" *Id.* (ellipsis in original). The court found that the "lengthy legislative history of § 145 and its predecessor statute" confirms that "Congress intended to provide for a civil action in which an applicant would be free to introduce new evidence." *Id.*

The court rejected the government's argument that an applicant "is only allowed to introduce new evidence that the applicant could not reasonably have provided to the agency in the first instance." App. 21a (internal quotation marks omitted). With respect to the government's principal argument – namely, that the "bill in equity" authorized by Revised Statutes § 4915 ("R.S. § 4915"), the predecessor to § 145, was only a "bill of review" – the court held that a bill of review was strictly a mechanism for a court in equity to revisit *its own* prior decree. Such a characterization of the "bill in equity" authorized by R.S. § 4915 was contrary to not only basic rules of equity procedure but also Supreme Court and other federal court precedent. The court dismissed the government's "policy considerations" as matters within Congress's discretion. App. 32a-33a. Relying in part on *amicus* briefs filed by the leading associations of patent lawyers, the court specifically rejected the government's claim that its holding would either encourage patent applicants to withhold evidence or push them to file actions under § 145 rather than on-the-record appeals under § 141. *See* App. 33a-34a.

The court held that "proceedings before the Patent Office remain relevant in a § 145 action." App. 27a.

First, in the absence of new evidence, "the district court must apply the court/agency standard of review to [agency] fact finding." *Id.* (citing *Fregeau v. Mossinghoff*, 776 F.2d 1034, 1038 (Fed. Cir. 1985)). Second, the Court noted that "*issues* (and evidence relating to new issues) that were not raised in the Patent Office proceedings generally may not be raised in a § 145 proceeding." App. 28a (emphasis added). Third, while the court "reject[ed] the Director's proposed restrictions on admissibility," it noted that, under existing law, "the district court may consider the proceedings before and findings of the Patent Office in deciding what weight to afford an applicant's newly-admitted evidence." *Id.*

8. Judge Newman concurred in part and dissented in part; she would have held that the district court is required to make all determinations *de novo* – whether or not new evidence is introduced. App. 36a-43a.

Judge Dyk, joined by Judge Gajarsa, dissented; he would have held that an action under § 145 is no different from any other action for administrative review under the Administrative Procedure Act ("APA") and "based on the agency record" unless "'agency fact-finding procedures are inadequate.'" App. 51a (quoting *Citizens To Preserve Overton Park, Inc. v. Volpe*, 401 U.S. 402, 415 (1971)). Acknowledging that this was not the government's position, the dissent insisted that "there is little difference between the standard for the receipt of new evidence urged by the PTO and the standard I think is appropriate." App. 52a n.4.

REASONS FOR DENYING THE PETITION

I. THE FEDERAL CIRCUIT'S RULING THAT NEW EVIDENCE IS ADMISSIBLE IN ACTIONS UNDER § 145 DOES NOT MERIT REVIEW

A. The Federal Circuit's Ruling On Admission Of Evidence Is Correct

The Court should deny review with respect to the first question presented because the government provides no reason to doubt that the Federal Circuit's resolution of the question is correct. The unique language of § 145, the unusual structure of the patent statute – which separately provides for on-the-record review (under § 141) and a civil action (under § 145) – and the history of the action that § 145 preserves compel the conclusion that a plaintiff in a civil action under § 145 may, consistent with ordinary procedural rules and the Federal Rules of Evidence, introduce new evidence to attempt to prove that he "is entitled to receive a patent for his invention." 35 U.S.C. § 145.

1. a. The language of the statute indicates that Congress intended a *de novo* proceeding and not an action for on-the-record judicial review. The statute authorizes a dissatisfied patent applicant to bring a "civil action" in federal district court "against the Director [of the PTO]" in which the "court may adjudge that such applicant is entitled to receive a patent for his invention . . . as the facts in the case may appear." 35 U.S.C. § 145. "The terminology employed by Congress," *Chandler v. Roudebush*, 425 U.S. 840, 845 (1976), indicates that the district court is not restricted to review of the prior decision of the PTO. Congress expressly directs district courts to adjudicate whether the invention is patentable "as the facts

in the case may appear." That language makes clear that the court is not restricted to evaluating the PTO's decision on the facts that were before the PTO, but instead is to determine, for itself, whether the patent should issue.[3] That language indicates that the "civil action" to which applicants "are entitled" under § 145 "is to be a trial *de novo*." *Id.*[4]

The government argues that the civil action authorized under § 145 should presumptively be subject to limitations on the nature and scope of review generally associated with "judicial review of agency action." Pet. 12. But that argument takes as its premise the claim that § 145 simply provides for judicial review of the PTO's decision, rather than, as the language (and title) of the provision plainly indicate, a civil action *to obtain a patent*. In each of the cases that the government relies on as establishing the "background principles" of law (*id.*) that the Federal Circuit sup-

---

[3] The government seeks to distinguish *Chandler* (upon which the Federal Circuit relied) on the basis that the right to a trial *de novo* for federal employees under Title VII of the Civil Rights Act of 1964 was the same as the right for private sector employees. But that has nothing to do with the Court's analysis of the amended statutory language of § 706 of the Civil Rights Act, 42 U.S.C. § 2000e-5, which, the Court found, "reflects the *de novo* character of the private sector 'civil action' even more clearly than did the 1964 version." 425 U.S. at 845.

[4] This does not mean that the district court disregards the administrative record. By its terms, § 145 authorizes the district court to "adjudge that [the] applicant is entitled to receive a patent for his invention, *as specified in any of his claims involved in the decision of the Board*." 35 U.S.C. § 145 (emphasis added). Thus a § 145 "proceeding is, in fact and necessarily, a part of the application for the patent," *Gandy v. Marble*, 122 U.S. 432, 439 (1887), in that the question is whether the plaintiff is entitled to a patent on the claims as presented in the application.

posedly disregarded, the statute expressly provides an action to review a prior administrative decision, rather than a civil action to obtain adjudication by the district court of underlying statutory rights.[5] As this Court recognized in *Zurko*, § 145 provides for a fundamentally different remedy from agency-review remedies. *See* 527 U.S. at 164.

The language of § 145 thus is contrary to any general restriction on admission of new evidence. Rather, in a "civil action" under § 145, as in any civil action, the Federal Rules of Evidence govern the admissibility of new evidence. *See* Fed. R. Evid. 1101(b) ("[t]hese rules apply generally to civil actions"); *id.* 402 ("All relevant evidence is admissible, except as otherwise provided by the Constitution of the United States, by Act of Congress, by these rules, or

---

[5] *See Florida Power & Light Co. v. Lorion*, 470 U.S. 729, 744 (1985) (Hobbs Act review in court of appeals); *Citizens To Preserve Overton Park*, 401 U.S. at 413-14 (APA review); *Consolo v. Federal Maritime Comm'n*, 383 U.S. 607, 613 (1966) (action brought in court of appeals pursuant to statute authorizing actions "to enjoin, set aside, suspend . . . or determine the validity of . . . final orders of the . . . Federal Maritime Board") (third ellipsis in original); *United States v. Carlo Bianchi & Co.*, 373 U.S. 709, 714 (1963) ("the statute is designated as an Act 'To permit review' and . . . the reviewing function is one ordinarily limited to consideration of the decision of the agency or court below"); *NBC v. United States*, 319 U.S. 190, 193 (1943) (suit brought to enjoin enforcement of Federal Communications Commission regulation); *Tagg Bros. & Moorhead v. United States*, 280 U.S. 420 (1930) (proceeding under § 316 of the Packers and Stockyards Act, which deals with actions seeking to "suspend[] or restrain[] the enforcement, operation, or execution of, or the setting aside in whole or in part the orders" of, the Secretary of Agriculture, 7 U.S.C. § 217).

by other rules prescribed by the Supreme Court pursuant to statutory authority.").[6]

b. Congress's authorization of a *de novo* proceeding in § 145 is particularly clear in light of other provisions of the statute, which authorize an "appeal" of a PTO decision to the Federal Circuit. 35 U.S.C. § 141. In such an appeal, Congress directed that the court "shall *review* the decision from which an appeal is taken *on the record*" before the PTO. *Id.* § 144 (emphases added). This language makes clear not only that Congress knew how to confine a reviewing court to the agency record, but also that Congress intended to draw a fundamental distinction between an action merely seeking *review* (*i.e.*, an appeal) and a *de novo* action where new evidence would be admitted and the merits of the applicant's claims "adjudicat[ed]" by the district judge.

The government's argument that allowing new evidence in an action under § 145 "creates an unjustified disparity between the two statutory avenues for judicial review," Pet. 28, is nothing but a challenge to Congress's determination to give a dissatisfied patent applicant two fundamentally different avenues for relief from an adverse decision: an appeal (on the record) and a civil action (with new evidence). *See Zurko*, 527 U.S. at 164 (rejecting the argument that review of district court fact-finding in an appeal of a

---

[6] Section 145's "civil action" language contrasts with the language of "civil action *for review*" of an administrative decision, 29 U.S.C. § 722(c)(5)(J)(i) (emphasis added). The latter, because of its "review" language, required Congress to add explicit authorization to introduce new evidence in court. No such direction is needed for § 145's simple "civil action" language, without the "review" qualifier. *Cf. also, e.g.*, 42 U.S.C. § 300e-9(d)(3) (providing that "civil action brought to review" civil penalty shall be "a trial de novo").

decision under § 145 would create an anomaly and noting that § 145 calls for "nonexpert judicial fact-finding"). To complain, as the government does, that one avenue allows a patent applicant to obtain a *de novo* adjudication while the other provides only for review on the record is to complain about the statutory scheme, which intentionally gives patent applicants that choice. *See Sosa v. Alvarez-Machain*, 542 U.S. 692, 711 n.9 (2004) (applying "the usual rule that 'when the legislature uses certain language in one part of the statute and different language in another, the court assumes different meanings were intended'") (quoting 2A Norman J. Singer, *Statutes and Statutory Construction* § 46:06, at 194 (6th rev. ed. 2000)); *Custis v. United States*, 511 U.S. 485, 492 (1994). The government must direct that complaint to Congress.

c. The long history of § 145 strongly reinforces the conclusion that the provision means what it plainly says. Section 145 is the current codification of a cause of action that dates back to 1839. From that date until 1952 (when Congress adopted the modern terminology "civil action"), the statute authorized a "bill in equity" that – like § 145 – required the court to "adjudge that such applicant is entitled" to a patent. Congress would have understood that such a bill would invoke the original – not appellate – jurisdiction of the federal court and that new evidence would consequently be admitted in such cases.[7]

---

[7] The government notes in passing that new evidence was restricted in cases involving a "bill of review." Pet. 19-20. But that was not the language of § 145's "bill in equity" predecessors, and the government rightly no longer claims (as it argued below) that Congress would have understood a suit under those provisions to be, or to be analogous to, a bill of review. A "bill of review" was a particular form of action used for a purpose far

i. Courts have long recognized that the basic distinction between direct appeal and the "bill in equity" authorized by § 145's predecessors was precisely that the latter allowed for introduction of new evidence and an adjudication of the patent applicant's rights on the complete record. As this Court explained in its 1884 decision in *Butterworth v. United States ex rel. Hoe*, 112 U.S. 50 (1884), under the appeal provision – Section 4911 of the Revised Statutes – "the court act[s] only on the evidence adduced before [the Commissioner], and confin[es] its revision to the points set forth in the reasons of appeal." *Id.* at 60. By contrast, the "bill in equity" – R.S. § 4915 (the predecessor of § 145) – "means a proceeding in a court of the United States having original equity jurisdiction under the patent laws, according to the ordinary course of equity practice and procedure." *Id.* at 61. The Court went on:

> It is not a technical appeal from the patent-office, like that authorized in section 4911, confined to the case as made in the record of that office, but is prepared and heard upon *all* competent evidence adduced, and *upon the whole merits*. Such has been the uniform and correct practice in the circuit courts.

Id. (emphases added).

---

afield from the present setting, namely, to obtain an equity court's *reconsideration of its own ruling* (specifically, after the time to file a petition to rehear had passed). *See* 2 Thomas A. Street, *Federal Equity Practice* § 2117, at 1255 (1909) ("[T]he bill of review [is] in its nature only a more formal mode of obtaining a rehearing."); *id.* § 2121, at 1257 ("The principle that *a bill of review will lie only in the court where the decree to be reversed was rendered* is subject to no exception whatever.") (emphasis added). A bill of review was never used as a mechanism for obtaining judicial review of agency action.

This Court repeatedly confirmed this understanding. *See In re Hien*, 166 U.S. 432, 439 (1897) ("The bill in equity provided for by section 4915 is wholly different from the proceeding by appeal from the decision of the commissioner .... The one is in the exercise of original, the other of appellate, jurisdiction."); *Morgan v. Daniels*, 153 U.S. 120, 124-25 (1894); *Gandy*, 122 U.S. at 439 ("the proceeding by bill in equity, under section 4915, on the refusal to grant an application for a patent, intends a suit according to the ordinary course of equity practice and procedure, and is not a technical appeal from the patent-office, nor confined to the case as made in the record of that office, but is prepared and heard upon all competent evidence adduced").[8]

Morgan v. Daniels provides no support for the government's position, because that case has nothing to do with the standard governing admission of evidence. After an interference proceeding (priority contest) in the Patent Office, the plaintiff filed an

---

[8] Numerous lower court decisions – including decisions cited with approval by the Court in *Butterworth* – recognized and applied the same rule. *See, e.g., Armstrong v. De Forest*, 13 F.2d 438, 440 (2d Cir. 1926); *Curtiss Aeroplane & Motor Corp. v. Janin*, 278 F. 454, 458 (2d Cir. 1921); *Central Ry. Signal Co. v. Jackson*, 254 F. 103, 105 (E.D. Pa. 1918); *General Elec. Co. v. Steinberger*, 208 F. 699, 700 (E.D.N.Y. 1913), *aff'd*, 214 F. 781 (2d Cir. 1914); *Appert v. Brownsville Plate Glass Co.*, 144 F. 115, 117 (C.C.W.D. Pa. 1904); *Bernardin v. Northall*, 77 F. 849, 852 (C.C.D. Ind. 1897); *Christie v. Seybold*, 55 F. 69, 72 (6th Cir. 1893) (Taft, J.); *Butler v. Shaw*, 21 F. 321, 326-27 (C.C.D. Mass. 1884); *In re Squire*, 22 F. Cas. 1015, 1016 (C.C.E.D. Mo. 1877); *see also Berry v. Robertson*, 40 F.2d 915, 917 (D. Md. 1930) ("[t]he present proceeding is not in the nature of an appeal, but rather a trial de novo, with all the customary power of an equity court to hear the evidence fully and to make its own findings").

action challenging the ruling for the defendant. The case was submitted to the trial court "without any additional testimony," and the court ruled for the plaintiff. 153 U.S. at 122. *Morgan* thus stands for the proposition that, where a plaintiff chooses *not* to rely on new evidence in challenging the outcome of a PTO interference proceeding, the district court's review of the PTO's findings of fact is deferential. *See also Zurko*, 527 U.S. at 164 (noting that a court-agency standard of review might apply "insofar as the district judge does no more than review PTO fact-finding"). It does not announce any restrictions on the introduction of new evidence.

ii. It was against this backdrop of settled judicial interpretation of Section 4915 that Congress, in 1927, revised and recodified the provision. Until then, a dissatisfied patent applicant could file a bill in equity only after pursuing a direct appeal. Under the new statute, an applicant chooses between challenging the Patent Office decision on direct appeal or filing a bill in equity.[9] The law otherwise preserved the existing provision for a bill in equity.

By re-enacting a provision for a "bill in equity" in light of decades of precedent interpreting that provision to allow for the introduction of new evidence in a *de novo* proceeding before a court of original jurisdiction, Congress incorporated that settled interpretation into the revised provision. *See Bragdon v.*

---

[9] *See* Act of Mar. 2, 1927, ch. 273, § 11, 44 Stat. 1335, 1336-37 (amending R.S. §4915). An initial draft of what became the 1927 statute would have eliminated the direct appeal altogether while preserving the bill in equity. *See To Amend Section 52 of Judicial Code and Other Statutes Affecting Procedure in the Patent Office: Hearing Before the H. Comm. on Patents*, 69th Cong. 7-8 (1926) ("House Hr'g").

Abbott, 524 U.S. 624, 645 (1998) (when "judicial interpretations have settled the meaning of an existing statutory provision, repetition of the same language in a new statute indicates, as a general matter, the intent to incorporate its . . . judicial interpretations as well"); *Merrill Lynch, Pierce, Fenner & Smith, Inc. v. Curran*, 456 U.S. 353, 378-79 (1982). Congress thus must be understood to have continued to allow plaintiffs to introduce new evidence in accordance with ordinary equity practice.[10] *See Hoover Co. v. Coe*, 325 U.S. 79, 87 (1945) (holding that the 1927 statute "sav[ed] to litigants the option of producing new evidence in a court, by retaining the equity procedure").[11]

---

[10] The late Judge Giles Rich, meticulous even as a law student, wrote in his 1929 paper on patent procedure that the "obvious difference between the regular bill and this bill in equity [under the 1927 version of R.S. §4915] is that in the former the case is heard on the record from the Patent Office, where in the latter new evidence may be introduced." *See* Giles S. Rich, *Outline of Patent Law and Procedure*, 3 J. Fed. Cir. Hist. Soc'y 61, 78 (2009). Judge Rich was one of the principal drafters of the 1952 Act; P.J. Federico – who shared Judge Rich's understanding of the scope of the bill in equity – was the other. *See* P.J. Federico, *Evolution of Patent Office Appeals*, 22 J. Pat. Off. Soc'y 838, 935 (1940).

[11] The legislative hearings that led up to the adoption of the 1927 revision further reinforce the point, reflecting the uniform understanding of the patent bar that an equity action under § 145 was a *de novo* proceeding complete with new evidence. Henry Huxley, a member of the ABA committee that had drafted the 1927 bill, explained that, in *ex parte* cases, a patent applicant could "start a suit in equity and have a real trial" to obtain a patent. House Hr'g at 9. Charles Howson, chairman of the ABA Committee on Patent Law Revision, testified that the bill in equity "enables the party in interest, desiring to obtain a patent to take evidence in a court or tribunal whose business it is to try issues of facts and make up a record in addition to that

iii. There is no dispute that the further recodification of R.S. § 4915 in 1952 at 35 U.S.C. § 145 – in a form close to the present one – made "'no fundamental change'" to the various mechanisms for obtaining relief from PTO rejections. Pet. 22 (quoting S. Rep. No. 82-1979, at 7 (1952)). The decision to preserve the existing remedy by trial *de novo* takes on additional significance because, prior to the adoption of the 1952 Act but after the 1927 Act, this Court had reconfirmed the nature of an action under R.S. § 4915. "It is evident that alternative rights of review are accorded an applicant, – one by appeal . . . , the other by bill in equity." *Hoover*, 325 U.S. at 83. In the latter, "*a formal trial is afforded on proof which may include evidence not presented in the Patent Office.*" *Id.* (emphasis added).[12]

---

he has been enabled to furnish the examiners in the Patent Office, and therefore get before a court of competent jurisdiction everything connected with his rights and every fact connected with his patent." *Id.* at 20-21. In the Senate hearing, testifying in support of the bill, Patent Commissioner Thomas Robertson testified that "a suit in equity under Section 4915 of the Revised Statutes" allowed a patent applicant to "start de novo and litigate the matter through the courts." *Procedure in the Patent Office: Hearing Before the S. Comm. on Patents*, 69th Cong. 7 (1926); *see also* App. 14a-18a.

[12] When Congress extended § 145 to additional situations after 1952, it again stated its understanding that the remedy affords a *de novo* proceeding on all evidence. In 1980, Congress amended the patent laws to provide for the current reexamination procedure. *See* Act of Dec. 12, 1980, Pub. L. No. 96-517, 94 Stat. 3015. The Committee Report accompanying the legislation noted that, under that provision, "[a]dverse final decisions . . . could be appealed . . . *or de novo review of the reexamination decision could be sought*" in district court. H.R. Rep. No. 96-1307(I), at 8 (1980) (emphasis added), *reprinted in* 1980 U.S.C.C.A.N. 6460, 6467; *see* 35 U.S.C. § 306.

iv. The government argues that the Federal Circuit's decision is inconsistent with pre-1952 circuit court decisions that "recognized limits on the admissibility of new evidence that the proponent could have presented to the PTO in the first instance." Pet. 20-21. But the government does not and cannot claim that any supposed "limits" recognized in these cases resemble the general bar on new evidence that could have been presented to the PTO that the government proposes here.[13] To the contrary, the cases that the government cites do not establish any limits on the introduction of evidence that are "different from a customary civil action." App. 11a-12a. Those cases – for example, *Barrett* – at most stand for the proposition that an applicant may be subject to equitable estoppel if he seeks to introduce evidence contrary to positions taken before the PTO.[14] Courts

---

[13] The government's reliance on those cases is particularly misplaced because, as the Federal Circuit noted, Congress could not have "implicitly adopted the different approaches various courts took with regard to an admissibility standard." App. 19a; *see* U.S. Br. at 18 n.4, *Microsoft Corp. v. i4i L.P.*, No. 10-290 (U.S. filed Mar. 18, 2011) ("Congress's inaction . . . raises no inference that it acquiesced in any particular standard . . . because there was no clear consensus among the courts of appeals.").

[14] The Third Circuit noted in *Barrett* that it was "anxious that no one should think that we hold that any evidence not [in the record] is inadmissible in an action under section 4915" because "[s]uch a notion would destroy the action given by section 4915." 22 F.2d at 397; *see also Minnesota Mining & Mfg. Co. v. Carborundum Co.*, 155 F.2d 746, 748 (3d Cir. 1946) ("*3M*") (rejecting the argument that evidence could be excluded simply because it was "available to the plaintiffs at the time of the proceedings in the Patent Office" as an effort "to rewrite the statute").

In the other court of appeals cases the government cites – *Schilling v. Schwitzer-Cummins Co.*, 142 F.2d 82 (D.C. Cir.

of appeals repeatedly reconfirmed in the years leading up to the 1952 recodification that evidence could not be excluded in an action under R.S. § 4915 simply because it was available and not introduced before the PTO.[15]

2. There is no tension between Congress's decision to authorize the introduction of new evidence under § 145 and principles of administrative exhaustion. The government does not dispute that plaintiff met the statute's express exhaustion requirements. Plaintiff pursued his application for a patent through "the Board of Patent Appeals and Interferences in an appeal under section 134(a)," and he limits his § 145 suit to "claims involved in the decision of the Board." 35 U.S.C. § 145.

1944); *Boucher Inventions v. Sola Electric Co.*, 131 F.2d 225 (D.C. Cir. 1942); *Globe-Union, Inc. v. Chicago Telephone Supply Co.*, 103 F.2d 722 (7th Cir. 1939); *Greene v. Beidler*, 58 F.2d 207 (2d Cir. 1932); and *Western Electric Co. v. Fowler*, 177 F. 224 (7th Cir. 1910) – the district court had admitted (or, in one case, considered without formally admitting) the evidence that the plaintiffs sought to introduce over objections by the defendants that such evidence had not been presented to the Patent Office, and therefore involve no holding that evidence could be excluded under any standard. *See also Smith v. Prutton*, 127 F.2d 79, 81 (6th Cir. 1942) ("[t]he statute . . . gives the litigants permission to present the case anew to the District Court after it has been finally closed in the Patent Office, and imposes upon the District Judge the obligation of hearing the evidence and determining the issue").

[15] *See, e.g., 3M*, 155 F.2d at 748 (to exclude evidence "available to the plaintiffs at the time of the proceedings in the Patent Office" "would be to change the nature of an R.S. Section 4915 proceedings and to rewrite the statute"); *Nichols v. Minnesota Mining & Mfg. Co.*, 109 F.2d 162, 166-67 (4th Cir. 1940); *Globe-Union*, 103 F.2d at 728; *Dowling v. Jones*, 67 F.2d 537, 538 (2d Cir. 1933) (L. Hand, J.).

The Federal Circuit also held that "issues (and evidence relating to new issues) that were not raised in the Patent Office proceedings generally may not be raised in a § 145 proceeding." App. 28a. That principle of "issue exhaustion," *Sims v. Apfel*, 530 U.S. 103, 110 (2000), does not apply to new *evidence*. Because plaintiff contested the examiner's written-description rejections at every stage before the PTO, he satisfied any non-textual exhaustion requirement. None of the government's cases supports the argument that principles of administrative exhaustion can be invoked to bar the introduction of *new evidence* relevant to issues that were raised and decided by the agency.[16]

B. The Decision Below Is Of Limited Importance And Makes Policy Sense

1. In the 35 years since the Federal Circuit was established with exclusive jurisdiction over appeals of actions under § 145, that court had no occasion to address the standard governing admission of evidence in such cases.[17] The absence of controversy on

---

[16] *See McKart v. United States*, 395 U.S. 185, 196-97 (1969) (rejecting government's argument that exhaustion barred judicial review where "[w]e are not . . . faced with a premature resort to the courts" because "all administrative remedies are now closed to petitioner"); *McCarthy v. Madigan*, 503 U.S. 140, 145 (1992) (rejecting claim that prisoner was obligated to exhaust administrative remedies).

[17] The government relies on *DeSeversky v. Brenner*, 424 F.2d 857 (D.C. Cir. 1970) (per curiam), and *California Research Corp. v. Ladd*, 356 F.2d 813 (D.C. Cir. 1966), to argue that, after 1952 but before the establishment of the Federal Circuit, some courts excluded evidence on bases other than those recognized below. Even if there were any inconsistency, that would not justify review, given the Federal Circuit's exclusive jurisdiction. In any event, those cases do not support the government.

this issue undermines the government's claim that it is one of general significance in the administration of the patent statute.

It has been the understanding of the patent bar that new evidence is generally admissible in actions under § 145. The most-cited treatise advises that, "[u]nlike the 'on-the-record' review by direct appeal to the Federal Circuit, the civil action is a *de novo* proceeding. The PTO record is admissible evidence, but both the applicant and the PTO may offer additional evidence." 4 Donald S. Chisum, *Chisum on Patents* § 11.06[3][c][ii] (2005) (footnotes omitted). The leading associations of patent lawyers filed *amicus* briefs below agreeing that new evidence is admissible under § 145 whether or not it was available and introduced in the PTO. *See* AIPLA Br. 6 (given settled expectation that new evidence may be presented under § 145, decision "altering the judicial landscape would be counterproductive and harmful"); NYIPLA Br. 8-9; FICPI Br. 2-3.

Notwithstanding applicants' ability to proffer new evidence, actions under § 145 have been scarce, both in absolute number and relative to direct appeals under § 141. The government told the Federal Circuit that there were 46 actions filed under § 145 in a seven-year period, compared with more than 300 direct appeals under § 141 filed during the same

---

In *DeSeversky*, the D.C. Circuit recognized that an action under § 145 is "a trial *de novo*" in which the applicant "may introduce evidence not previously presented to the Patent Office," but stated that the applicant "is precluded from presenting new *issues*." 424 F.2d at 858 (second emphasis added). In *California Research*, the court reversed the exclusion of evidence by the district court, emphasizing that the proceeding under § 145 is "a trial de novo." 356 F.2d at 818.

period. *See* Gov't En Banc Br. 40 n.11.[18] Furthermore, the government conceded that evidence is frequently admitted in § 145 cases without objection by the PTO. There is simply no basis for the government's claim that the ruling below will have any broad impact.[19]

2. Congress's decision to afford patent applicants an opportunity to introduce new evidence in an action under § 145 is self-evidently within its power; it also sensibly reflects institutional considerations. To build a case for consideration by a non-expert district judge may require evidence that would be superfluous before the PTO. This case provides an illustration: because the examiner is expected to have ordinary skill in the relevant art, an applicant is not required to provide evidence to establish what the examiner should already know. The government's pervasive emphasis on the PTO's comparative expertise thus itself provides a central explanation for

---

[18] While the government argues that the decision below may encourage additional cases under § 145, there is no reason to expect any such surge, given that the decision below confirmed the law as it had been understood. Even if there had been uncertainty, that does not explain why – if the possibility of introducing new evidence provided the sort of procedural advantage that the government claims – applicants had rarely tested the limits.

[19] As the government concedes, where an application is denied because some additional evidence is required, an applicant can usually address that deficiency through a request for continued examination or a continuation application. *See* Pet. 3. Those remedies make district court litigation even more unlikely. Those remedies were not available to plaintiff, however, because his application was filed before June 8, 1995, claiming benefit of a 1984 application, *see* 37 C.F.R. § 1.114(e)(2), and because, if plaintiff had filed a continuation application, any issued patent would have expired in 2004.

§ 145's allowance of additional evidence when non-expert district courts must address patentability issues.

There are additional reasons that allowing new evidence is warranted. Particularly in *ex parte* proceedings (as opposed to interferences), the practical limits on the time the PTO can spend on each application may limit an applicant's ability to identify critical issues and present responsive evidence. Here, the Board invested substantial time in its review, but the examiner's rejection and his answering brief provided little guidance as to the basis for the written-description rejections. With respect to the rejections that were affirmed, the Board was the first to provide an articulation of reasons. When the plaintiff filed a request for rehearing addressing the Board's new rationales, the Board refused to consider it. Section 145 provides important protection against that type of procedural unfairness.

3. The government's suggestion that the decision below will encourage applicants to withhold evidence from the PTO is baseless. Irrespective of the opportunity to present additional evidence later, patent applicants always have an incentive to present their best case to the PTO: any appeal is expensive, and an action under § 145 is even more so because a plaintiff under § 145 must pay the costs of the proceeding – even if the plaintiff prevails. *See* 35 U.S.C. § 145. Expert witness testimony – which is rare before the PTO but often needed in district court – further inflates the applicant's financial burden. As *amici* explained below, it would be contrary to an applicant's interest to fail to put the best possible case before the PTO to overcome a rejection. *See* IPOA Br. 4 ("Understanding the interests of applicants

proceeding before the PTO and district court reveals that the panel's concern that patentees will 'game the system' by withholding evidence from the PTO is without basis."); NYIPLA Br. 10; *see also* FICPI Br. 3 (explaining potential burden on PTO if evidence were introduced solely for purposes of establishing record for appeal). A nearly unanimous Federal Circuit, including judges with long experience dealing with the patent system, rightly concluded that "[a]n applicant has every incentive to provide the Patent Office with the best evidence in its possession, to obtain a patent as quickly and inexpensively as possible." App. 33a.

Any supposed temptation that an applicant might otherwise have to withhold evidence before the PTO is further counterbalanced by the general risk that the district court will rule against the applicant. An applicant has every incentive to get a favorable decision from the PTO in the first instance and not to rely on § 145 litigation. Here, the evidence that plaintiff sought to introduce simply provided – in response to grounds given for the first time in the Board decision – further explanation of what was already before the PTO, that is, the patent disclosure. Plaintiff did his best to submit additional argument responding to the new grounds of decision articulated in the Board's decision, but the Board dismissed his request for rehearing. There can be no question of any sandbagging.

II. THE FEDERAL CIRCUIT'S LIMITED RULING ON STANDARD OF REVIEW IS NOT BEFORE THE COURT AND IS PLAINLY CORRECT

A. The Government, Arguing Only Against Admission Of New Evidence, Did Not Contest Existing Federal Circuit Law Requiring *De Novo* Determination Where New Evidence Is Admitted

The standard of review in a case under § 145 was settled by the Federal Circuit in 1985 and reconfirmed (after making appropriate adjustments in light of *Zurko*) in 2003. In *Fregeau v. Mossinghoff*, the court held that, where new evidence is introduced, "a *de novo* finding will be necessary to take such evidence into account together with the evidence before the board." 776 F.2d at 1038. In *Mazzari v. Rogan*, 323 F.3d 1000 (Fed. Cir. 2003), the court confirmed that, if "parties choose to present additional evidence . . . , the district court would make *de novo* factual findings." *Id.* at 1005. If, however, there is no new evidence, "the court reviews the case on the same record presented to the agency and the reviewing court must apply the APA's substantial evidence standard." App. 30a-31a; *see also Mazzari*, 323 F.3d at 1005; *Fregeau*, 776 F.2d at 1038. The Federal Circuit in this case simply restated existing law. *See* App. 30a-32a.

The government below argued for strict limitations on the *introduction of new evidence* in an action under § 145, but it did not challenge the Federal Circuit's settled rules governing *standard of review*. *See* App. 31a ("The Director does not dispute that these standards of review apply in a § 145 action."). The government cited *Fregeau* and *Mazzari* a dozen times

and did not suggest that any aspect of those cases was in error. At most, as the court of appeals noted, the government argued that "the principles of deference to agency fact finding . . . would tend to support more restrictions on the admissibility of evidence." *Id.* Given the government's failure to challenge the applicable standard of review, that question is not properly presented in its petition. *See United States v. United Foods, Inc.*, 533 U.S. 405, 416-17 (2001).[20]

B. The Federal Circuit's *De Novo* Standard When New Evidence Is Admitted Is Correct

In any event, the Federal Circuit's holding that the district court rules on factual issues *de novo* when new evidence is admitted is correct. That holding simply reflects the fact that, when new evidence is admitted in court, there is no prior decision on that record for the district court to review. *See Zurko*, 527 U.S. at 164 (noting that, in an action under § 145, "[t]he presence of ... new or different evidence makes a factfinder of the district judge"). That standard is consistent with the language of § 145, which authorizes the district court to rule on the plaintiff's entitlement to receive a patent "as the facts in the case may appear." 35 U.S.C. § 145.

That does not mean that the PTO proceedings and findings are irrelevant in a case under § 145. As

---

[20] The government asserted, in passing, that "no determination of the USPTO will be overturned based on evidence the agency never had the opportunity to consider unless that evidence 'in character and amount carries thorough conviction' that the agency's decision was mistaken." Gov't En Banc Br. 29 (quoting *Morgan*, 153 U.S. at 125). Such a passing reference is no substitute for a direct request, let alone a developed argument, for overruling established precedents (that the government itself repeatedly cited).

the Federal Circuit made clear, under existing law, when new evidence is admitted, "the court must still consider the administrative record in making its fact findings." App. 32a. "[T]he district court may consider the proceedings before and findings of the Patent Office in deciding what weight to afford an applicant's newly-admitted evidence." App. 28a. For example, "[s]hould the facts of a particular case cast suspicion on new evidence that an applicant failed to introduce before the Patent Office, the district court in a § 145 action would be within its discretion to give that evidence less weight." App. 28a-29a.

The Federal Circuit's reaffirmation of the *de novo* standard is not in tension with the Court's decision in *Morgan*. The plaintiff in *Morgan* did not proffer any additional evidence; the Court therefore had no occasion to resolve the question of how to weigh new evidence against a prior PTO determination. *See supra* pp. 17-18. *Morgan*'s statements regarding the burden on a plaintiff (in an interference) seeking to overcome the outcome of a prior adversary proceeding before the PTO are not inconsistent with the holding that admission of new evidence, in any civil action challenging the denial of a patent, requires a *de novo* determination as held by the court below.

III. THE COURT SHOULD NOT HOLD THE PETITION

There is no justification for holding the petition for *Microsoft* because, as the United States effectively admits, *Microsoft* can have no relevance to the question whether new evidence may be admitted in an action under § 145. Pet. 31 ("[T]he first question presented . . . has no analogue in *Microsoft*."). That is the only question properly before the Court in this case.

Moreover, any guidance that *Microsoft* provides concerning the evidentiary weight to be given to final PTO determinations in later infringement litigation will not affect the judgment of the Federal Circuit. The decision below provides that, where an applicant introduces new evidence in a civil action under § 145, the court decides factual issues *de novo* on a new factual record. Whatever the outcome in *Microsoft*, it would provide no basis for granting the petition, even for the purpose of a remand to the Federal Circuit.[21]

CONCLUSION

The petition for a writ of certiorari should be denied.

---

[21] The basis of the government's "hold" recommendation here appears to be that, if the Court affirms in *Microsoft*, its decision may be based on principles of deference to final PTO decision-making that would be relevant to the standards governing in a § 145 action. But the government argues for *affirmance* of existing Federal Circuit standards governing the defense of patent invalidity. Given that Federal Circuit standards in both areas have co-existed for decades, the government's suggestion that a decision in *Microsoft* could undermine existing Federal Circuit law in this quite different context is particularly unfounded.

Respectfully submitted,

MICHAEL L. MARTINEZ
CROWELL & MORING LLP
1001 Pennsylvania Ave., N.W.
Washington, D.C. 20004
(202) 624-2500

GREGORY L. ROTH
5712 Parkwest Circle
La Palma, California 90623
(714) 723-6871

AARON M. PANNER
Counsel of Record
KELLOGG, HUBER, HANSEN,
TODD, EVANS & FIGEL,
P.L.L.C.
1615 M Street, N.W.
Suite 400
Washington, D.C. 20036
(202) 326-7900
(apanner@khhte.com)

May 27, 2011

REPLY BRIEF

No. 10-1219

In the Supreme Court of the United States

DAVID J. KAPPOS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR, UNITED STATES PATENT AND TRADEMARK OFFICE, PETITIONER

v.

GILBERT P. HYATT

ON PETITION FOR A WRIT OF CERTIORARI TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

REPLY BRIEF FOR THE PETITIONER

NEAL KUMAR KATYAL
Acting Solicitor General
Counsel of Record
Department of Justice
Washington, D.C. 20530-0001
SupremeCtBriefs@usdoj.gov
(202) 514-2217

TABLE OF CONTENTS

Page

I. The Federal Circuit's decision disregards administrative-law principles and departs from the prevailing understanding of Section 145's predecessor statute 2
II. The questions presented are important and warrant review 8
Conclusion 11

TABLE OF AUTHORITIES

Cases:

Barrett Co. v. *Koppers Co.*, 22 F.2d 395 (3d Cir. 1927) 8
Butterworth v. *United States ex rel. Hoe*, 112 U.S. 50 (1884) 7
California Research Corp. v. *Ladd*, 356 F.2d 813 (D.C. Cir. 1966) 8, 9
Chandler v. *Roudebush*, 425 U.S. 840 (1976) 4
DeSeversky v. *Brenner*, 424 F.2d 857 (D.C. Cir. 1970) .. 8, 9
Dickinson v. *Zurko*, 527 U.S. 150 (1999) 3, 6, 9
Gandy v. *Marble*, 122 U.S. 432 (1887) 7
Globe-Union, Inc. v. *Chicago Tel. Supply Co.*, 103 F.2d 722 (7th Cir. 1939) 8
Hien, In re, 166 U.S. 432 (1897) 7
Hoover Co. v. *Coe*, 325 U.S. 79 (1945) 7
INS v. *Orlando Ventura*, 537 U.S. 12 (2002) 6
Knutson v. *Gallsworthy*, 164 F.2d 497 (D.C. Cir. 1947) 8
Morgan v. *Daniels*, 153 U.S. 120 (1894) 2, 3, 6, 7, 11

Cases—Continued: Page

Tagg Bros. & Moorhead v. *United States*, 280 U.S. 420 (1930) 5
United States v. *Carlo Bianchi & Co.*, 373 U.S. 709 (1963) 4

Statutes and rule:

Administrative Procedure Act, 5 U.S.C. 701 *et seq.* 3, 7
Rev. Stat. § 4915 (1878) 3, 7, 9
35 U.S.C. 2(a) 2
35 U.S.C. 141 ..... 4, 9
35 U.S.C. 144 4
35 U.S.C. 145 ..... 2, 3, 4, 7, 9
42 U.S.C. 405(g) 4
Fed. R. Civ. P. 2 4

Miscellaneous:

4 Donald S. Chisum, *Chisum on Patents* (2005) 9
S. Rep. No. 1979, 82d Cong., 2d Sess. (1952) 7

In the Supreme Court of the United States

No. 10-1219

DAVID J. KAPPOS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR, UNITED STATES PATENT AND TRADEMARK OFFICE, PETITIONER

v.

GILBERT P. HYATT

ON PETITION FOR A WRIT OF CERTIORARI TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

REPLY BRIEF FOR THE PETITIONER

The Federal Circuit held that a disappointed patent applicant may challenge the considered decision of the United States Patent and Trademark Office (PTO) based on evidence that the applicant could have presented to the PTO. The court compounded that error by holding that the district court should engage in de novo review of any issues to which the new evidence pertains, including ultimate questions of patentability. As the petition for a writ of certiorari explains, that decision disregards fundamental principles of administrative review, and it undermines the PTO's ability to exercise its expert judgment in determining whether patents should issue.

In defending the Federal Circuit's approach, respondent argues that Section 145 is not an action for judicial review of the PTO's decision. Respondent further contends that, because Section 145 does not wholly preclude the introduction of new evidence, the plaintiff in such a suit may introduce evidence that it failed without cause to present to the agency. Those arguments lack merit. This Court recognized long ago that actions under Section 145's statutory predecessor involved judicial review of agency determinations, see *Morgan* v. *Daniels*, 153 U.S. 120, 124 (1894), and the fact that new evidence is admissible in such actions does not alter the fundamental nature of the proceeding. The extent to which new evidence is admissible in a Section 145 suit, and the standard of review under which the PTO's decision should be evaluated, therefore should be determined in light of the background principles that govern review of agency action. Respondent's efforts to minimize the anomalous nature and perverse consequences of the Federal Circuit's decision are similarly unpersuasive.

I. THE FEDERAL CIRCUIT'S DECISION DISREGARDS ADMINISTRATIVE-LAW PRINCIPLES AND DEPARTS FROM THE PREVAILING UNDERSTANDING OF SECTION 145'S PREDECESSOR STATUTE

A. Respondent contends (Br. in Opp. 12) that Section 145 is a freestanding "civil action *to obtain a patent*" from the district court, rather than an action for judicial review of an administrative decision. That view is inconsistent with the statutory text and with this Court's decision in *Morgan*.

Congress has authorized the PTO to determine whether a patent should issue. See 35 U.S.C. 2(a). Section 145 provides that a patent applicant "dissatisfied with the decision" of the PTO may seek a "remedy by civil action against the Director" in district court. 35 U.S.C. 145. And if the court

in a Section 145 suit concludes that the plaintiff "is entitled to receive a patent for his invention," the court does not issue the patent itself; rather, its decision "authorize[s] the Director to issue such patent on compliance with the requirements of law." *Ibid.* Those aspects of the statutory text make clear that Section 145 affords an avenue for judicial review of the PTO's determination. Indeed, respondent acknowledges (Br. in Opp. 18) that, when a Section 145 plaintiff does *not* introduce new evidence, the district court must resolve the case by applying the deferential standards that govern review of agency action under the Administrative Procedure Act (APA), 5 U.S.C. 701 *et seq.* See *Dickinson* v. *Zurko*, 527 U.S. 150, 164 (1999).

The fact that new evidence is sometimes admissible in a Section 145 action does not alter the administrative-review character of the proceeding. In *Morgan*, the Court explained that the objective of an action under Revised Statutes § 4915 (1878) (R.S. 4915) (Section 145's predecessor) was to "set aside" the determination made by the "executive department[] * * * charged with the administration of the patent system." 153 U.S. at 124. The Court accordingly applied administrative-law principles in crafting a deferential standard to govern review of the Patent Office's decision. *Id.* at 124-125. The introduction of evidence not considered by the PTO does not alter the plaintiff's objective, or the fact that the ultimate question for the court is whether the PTO's decision should stand.

Respondent also argues (Br. in Opp. 11) that Section 145's use of the term "civil action" indicates that "Congress intended a *de novo* proceeding." That argument is likewise inconsistent with respondent's concession that a deferential standard applies when a Section 145 plaintiff does not introduce new evidence, and it is unpersuasive on its own terms, since Congress often authorizes district courts to exercise

original jurisdiction over suits for review of agency action. See, *e.g.*, *United States* v. *Carlo Bianchi & Co.*, 373 U.S. 709, 715 (1963); Pet. 16. Contrary to respondent's contention (Br. in Opp. 11-12), *Chandler* v. *Roudebush*, 425 U.S. 840 (1976), does not suggest that use of the phrase "civil action," without more, denotes an independent proceeding. Rather, the Court in *Chandler* relied on the statutory structure, rather than on the phrase "civil action," in concluding that Title VII authorized "trials *de novo*." See Pet. 15.[1]

Respondent also asserts (Br. in Opp. 14-15) that, because 35 U.S.C. 141 and 144 provide for a direct on-the-record appeal of the PTO's decision, Section 145 must be construed to permit the introduction of new evidence without limitation. That is a false dichotomy. To be sure, Section 144's express requirement that review in a Section 141 appeal be "on the record before the [PTO]," combined with the absence of similar language in Section 145, indicates that Section 145 plaintiffs are not wholly foreclosed from introducing evidence that was not before the agency. But the fact that Section 145 allows new evidence under *some* circumstances does not mean that the introduction of such evidence is unconstrained by background administrative-law principles. The approach advocated by the government and by the dissenters below, under which the plaintiff in a Section 145 action may introduce evidence that he had no reasonable opportunity to present to the PTO, preserves distinct roles for Sections 141 and 145 while respecting usual rules of agency exhaustion. See pp. 5, 7, 9-10, *infra*.

---

[1] If the use of the term "civil action," which refers to an action in district court, see Fed. R. Civ. P. 2, were sufficient to mandate a de novo proceeding, then numerous statutes authorizing administrative review in district court would require independent proceedings. See, *e.g.*, 42 U.S.C. 405(g).

B. Because a Section 145 plaintiff seeks to overturn the PTO's denial of his patent application, the admissibility of new evidence and the standard of review should be informed by the background principles that govern judicial review of agency action. Respondent's contrary arguments lack merit.

1. By allowing respondent to introduce evidence that he failed without cause to present to the PTO, the court of appeals condoned a flagrant breach of well-established exhaustion principles. See Pet. 14. Respondent argues (Br. in Opp. 22-23) that exhaustion rules forbid raising new *issues* but not new *evidence*. But the withholding of evidence from the PTO undermines the agency's ability to perform its statutory functions and deprives the reviewing court of the agency's expertise. See, *e.g.*, *Tagg Bros. & Moorhead* v. *United States*, 280 U.S. 420, 444-445 (1930). Contrary to respondent's suggestion (Br. in Opp. 22), the litigation conduct approved by the court of appeals directly implicates the concerns that underlie exhaustion requirements, even though respondent pursued an administrative appeal on the issue that he ultimately raised in court.

2. The court of appeals further held that, when a Section 145 plaintiff introduces evidence that was not before the agency, the court should resolve de novo all issues to which the new evidence pertains. As the petition explains (Pet. 16-18), that holding disregards administrative-deference principles, and it exacerbates the adverse effects of the court's admissibility ruling by encouraging patent applicants to withhold evidence from the PTO.

Respondent does not dispute that the decision below permits district courts to engage in de novo review not only of the PTO's subsidiary factual determinations, but also of its ultimate conclusions on questions of patentability. See Pet. 17. Instead, respondent argues (Br. in Opp. 29) that de

novo review is justified when an applicant presents new evidence because "there is no prior decision on that record for the district court to review." But even in such cases, the PTO *has* made a decision within its delegated authority on the ultimate question of patentability, and it has applied its expertise to the evidence before it. The presence of new evidence does not justify discarding the bedrock principle that a court should not overturn the agency's decision without a high degree of confidence that the agency erred. See *INS* v. *Orlando Ventura*, 537 U.S. 12, 16 (2002); *Morgan*, 153 U.S. at 125. Rather, when a remand to the agency is infeasible, the court may give the new evidence greater weight but should overturn the PTO's decision only upon a "thorough conviction" that the plaintiff is entitled to a patent. See Pet. 23-25; *Morgan*, 153 U.S. at 125.[2]

Contrary to respondent's contention (Br. in Opp. 28-29), the government raised the standard-of-review issue before the Federal Circuit. The government explained that the district court should not overturn the PTO's decision "based on evidence the agency never had the opportunity to consider unless that evidence 'in character and amount carries thorough conviction' that the agency's decision was mistaken." Pet. C.A. En Banc Br. 29 (quoting *Morgan*, 153 U.S. at 125). And the Federal Circuit squarely resolved the issue, holding that, "[w]hen new evidence is introduced" in a Section 145 suit, the court should "make de novo fact findings if the evidence conflicts with any related [PTO] find-

---

[2] Respondent relies in part (Br. in Opp. 29) on this Court's statement in *Zurko* that the presence of new evidence "makes a factfinder of the district judge." 527 U.S. at 164. That observation, however, does not imply any particular view as to the standard of proof the court should apply when a Section 145 plaintiff is allowed to introduce new evidence. The Court in *Zurko* had no occasion to address that issue.

ing." Pet. App. 32a; see *id.* at 73a-74a (Dyk, J., joined by Gajarsa, J., dissenting)

C. The Federal Circuit's decision departs from the judicial understanding of R.S. 4915 that prevailed in 1952, when Congress reenacted that provision as Section 145. In accordance with *Morgan*, appellate courts construed R.S. 4915 in light of administrative-law principles, limiting the admissibility of new evidence and evaluating that evidence under *Morgan*'s "thorough conviction" standard of review. See Pet. 18-23. When Congress reenacted the provision with "no fundamental change," S. Rep. No. 1979, 82d Cong., 2d Sess. 7 (1952), it ratified that prevailing understanding.

Respondent contends (Br. in Opp. 16-17) that, because this Court had construed R.S. 4915 to permit the introduction of new evidence, the 1952 reenactment of Section 145 reflected Congress's intent to allow such evidence to be introduced without limitation. The decisions on which petitioner relies, however, did not concern the nature of an R.S. 4915 action and had no occasion to address the circumstances under which new evidence would be admissible. See Pet. 21 n.4; *Butterworth* v. *United States ex rel. Hoe*, 112 U.S. 50, 61 (1884) (R.S. 4915 action is "heard upon all competent evidence"—that is, all admissible evidence.); *Gandy* v. *Marble*, 122 U.S. 432, 439 (1887); *In re Hien*, 166 U.S. 432, 439 (1897); see also *Hoover Co.* v. *Coe*, 325 U.S. 79, 83 (1945). Respondent identifies no reason to conclude that Congress would have viewed these decisions as holding that new evidence is admissible without limitation, or that it intended to adopt that understanding when it recodified R.S. 4915 shortly after it enacted the APA. The chain of inferences respondent asks this Court to draw is particularly unlikely given the *Morgan* Court's characterization of R.S. 4915 actions as suits to "set aside" administrative determinations, 153 U.S. at 124, and given the many interven-

ing appellate decisions that had imposed limits on new evidence and the scope of review.

Respondent dismisses (Br. in Opp. 21-22 n.14) as dicta the limitations on evidence not presented to the PTO that were articulated in pre-1952 decisions. In fact, the courts that issued those decisions applied the evidentiary limitations they announced. See, *e.g.*, *Globe-Union, Inc.* v. *Chicago Tel. Supply Co.*, 103 F.2d 722, 728 (7th Cir. 1939) (admitting evidence in absence of suggestion that applicant "did not exercise due diligence"); *Barrett Co.* v. *Koppers Co.*, 22 F.2d 395, 397 (3d Cir. 1927) (excluding evidence that was "wholly within [party's] possession and control at the interference proceeding"); *Knutson* v. *Gallsworthy*, 164 F.2d 497, 509 (D.C. Cir. 1947) (court could consider evidence that was not intentionally withheld). And even when courts admitted new evidence in R.S. 4915 proceedings, they applied *Morgan*'s deferential standard of review, requiring a "thorough conviction" that the Patent Office had erred. See Pet. 21-22 (citing cases).

II. THE QUESTIONS PRESENTED ARE IMPORTANT AND WARRANT REVIEW

A. The Federal Circuit's decision conflicts not only with the pre-1952 appellate decisions described above, Pet. 25-27, but also with the post-1952 decisions of the D.C. Circuit, the court that exercised jurisdiction over Section 145 appeals before the establishment of the Federal Circuit. That court held that evidence that reasonably could have been presented to the Patent Office was not admissible in a Section 145 suit, and that the Patent Office's decision could be overturned only upon a "thorough conviction" that the agency had erred. See *DeSeversky* v. *Brenner*, 424 F.2d 857, 858 n.5 (D.C. Cir. 1970); *California Research Corp.* v. *Ladd*, 356 F.2d 813, 820 n.18 (D.C. Cir. 1966). And while

the D.C. Circuit in *DeSeversky* and *Ladd* referred to the Section 145 proceeding as a "trial de novo" (see Br. in Opp. 23-24 n.17), the court evidently did not view that label as inconsistent with the administrative-law-based limitations that it imposed on new evidence and the scope of judicial review. See *Ladd*, 356 F.2d at 818 n.12.

B. The decision below subjects the PTO's decisions to an unprecedented form of heightened judicial scrutiny, cf. *Zurko*, 527 U.S. at 165, and establishes a regime that will undermine the PTO's effectiveness by encouraging patent applicants to withhold evidence. Respondent downplays the significance of the Federal Circuit's decision, arguing (Br. in Opp. 24) that Section 145 has long been understood to permit the introduction of new evidence. In holding that new evidence is admissible *without limitation*, however, and that administrative-law principles have little relevance to Section 145 actions, the Federal Circuit departed sharply from the established understanding of Section 145 and its predecessor R.S. 4915. See Pet. 18 n.2; 4 Donald S. Chisum, *Chisum on Patents* § 11.06[3][c][iii], at 11-625 to 11-627 (2005) (admissibility of new evidence is "tempered" by limitations on withheld evidence and judicial deference to PTO).

The decision below also creates a pronounced and unjustified disparity between the review afforded in Section 141 and Section 145 actions. And the promise of de novo review on any patentability issue to which new evidence is relevant provides a strong incentive to withhold evidence from the PTO in order to proffer it in a Section 145 action. As respondent observes (Br. in Opp. 26), certain countervailing incentives—*e.g.*, the applicant's desire to maximize his chances of success in the agency proceedings, and the added expense associated with Section 145 actions—may encourage applicants to present all their evidence to the

PTO and thereby mitigate the practical impact of the court's decision. But the existence of such incentives does not distinguish disappointed patent applicants from plaintiffs who challenge other types of agency action. Such plaintiffs likewise have an interest in prevailing before the agency and thereby avoiding the expense of a lawsuit, but those incentives are routinely supplemented by rules requiring exhaustion and timely presentation of evidence. In any event, a rule that rewards applicants for withholding evidence from the agency does substantial harm to the patent system even if it does not affect every applicant's behavior. The Federal Circuit's decision will create the strongest incentive "to bypass the PTO" in those "cases where the patent is commercially significant and the costs of a separate proceeding can be justified"—yet those are the cases in which "PTO review is most important." Pet. App. 79a-80a (Dyk, J., joined by Gajarsa, J., dissenting).

Respondent's policy arguments (Br. in Opp. 25-26) do not justify the Federal Circuit's rule. Contrary to respondent's suggestion (Br. in Opp. 25), the decision encompasses all new evidence that is material to patentability, not simply the background materials presented for the benefit of a non-expert judge. This case is a prime example, as the PTO examiner was unable to find support for the claims despite his expertise, and respondent's declaration would have been highly relevant to the examiner's written-description concerns. As the district court found, Pet. App. 187a-188a, respondent had ample opportunity to respond to the examiner's concerns before his claims were rejected, and he was on notice that he bore the burden of demonstrating error before the Board. See Pet. 5-6. By excusing non-compliance with the PTO's evidence-presentation rules, the court's decision disrupts the PTO's efforts to regulate its examination process.

C. The Court recognized in *Morgan* that suits challenging Patent Office denials of patent applications, like validity challenges raised as defenses to infringement actions, implicated generally applicable principles of deference to administrative authority and expertise. See 153 U.S. at 123-124; Pet. 29-30. In *Microsoft Corp.* v. *i4i Ltd. Partnership*, No. 10-290 (argued Apr. 18, 2011), this Court is considering the application of those principles to suits in which an alleged infringer argues that an issued patent is invalid. The Court's decision in *Microsoft* therefore may shed light on the proper resolution of this case, and the petition should be held for *Microsoft*. Ultimately, however, *Microsoft* is unlikely fully to resolve the questions presented here. See Pet. 31. Both questions are sufficiently important to warrant plenary review because the Federal Circuit has adopted a regime that disregards fundamental administrative-law principles and undermines the PTO's delegated authority to determine whether patents should issue.

CONCLUSION

For the foregoing reasons and those stated in the petition, the petition for a writ of certiorari should be held pending this Court's decision in *Microsoft* v. *i4i Ltd. Partnership*, No. 10-290 (argued Apr. 18, 2011).

Respectfully submitted.

NEAL KUMAR KATYAL
Acting Solicitor General

JUNE 2011

JOINT APPENDIX

No. 10-1219

In the Supreme Court of the United States

DAVID J. KAPPOS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR, UNITED STATES PATENT AND TRADEMARK OFFICE,
PETITIONER

v.

GILBERT P. HYATT

ON WRIT OF CERTIORARI TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

VOLUME I
JOINT APPENDIX

DONALD B. VERRILLI, JR.
Solicitor General
Department of Justice
Washington, D.C. 20530-0001
SupremeCtBriefs@usdoj.gov
(202) 514-2217

Counsel of Record for Petitioner

AARON M. PANNER*
Kellogg, Huber, Hansen, Todd, Evans & Figel, P.L.L.C.
1615 M Street, N.W.
Suite 400
Washington, D.C. 20036
apanner@khhte.com
(202) 723-6871

GREGORY L. ROTH
5712 Parkwest Circle
La Palma, CA 90623
(714) 723-6871

* *Counsel of Record for Respondent*

PETITION FOR A WRIT OF CERTIORARI FILED: APR. 7, 2011
CERTIORARI GRANTED: JUNE 27, 2011

TABLE OF CONTENTS

Page

VOLUME 1

Court of appeals docket entries 1
District court docket entries 4
In re Application of Gilbert P. Hyatt:
Specification (June 6, 1995) 9

VOLUME 2

Specification Diagrams (June 6, 1995) 146

VOLUME 3

Amendment Under 37 C.F.R. § 1.111 (Oct. 15, 1996) 263
Final Office Action (July 30, 1997) 365
Appeal Brief (Sept. 2, 1998) 393

VOLUME 4

Examiner's Answer (Aug. 13, 1999) 541
Reply Brief Under 37 C.F.R. § 1.193(b) (July 31, 2000) 588
Request for Rehearing (Sept. 30, 2002) 670

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

No. 2007-1066

GILBERT P. HYATT, PLAINTIFF-APPELLANT

v.

DAVID KAPPOS, DIRECTOR, PATENT AND TRADEMARK OFFICE, DEFENDANT-APPELLEE

DOCKET ENTRIES

DATE	PROCEEDINGS
3/12/2007	Brief for Plaintiff-Appellant Gilbert P. Hyatt. BY Gilbert P. Hyatt (Appellant). SERVED BY Mail ON 3/12/2007. FILED ON 3/12/2007. (NON- CONFIDENTIAL)
	* * * * *
9/11/2007	Brief for Appellee-Director of The United States Patent and Trademark Office. BY Jon W. Dudas, Director, Patent and Trademark Office (Appellee). SERVED BY Mail ON 9/11/2007. FILED ON 9/11/2007. (CONFIDENTIAL & NON-CONFIDENTIAL VERSIONS)
	* * * * *

DATE	PROCEEDINGS
11/13/2007	Reply Brief for Plaintiff-Appellant Gilbert P. Hyatt. BY Gilbert P. Hyatt (Appellant). SERVED
	* * * * *
12/17/2007	Supplemental Joint Appendix. BY Gilbert P. Hyatt (Appellant). SERVED BY Mail ON 12/14/2007. FILED ON 12/17/2007. (NON-CONFIDENTIAL)
	* * * * *
2/1/2008	Joint Appendix (Four Volumes). BY Gilbert P. Hyatt (Appellant). SERVED BY Mail ON 11/27/2007. FILED ON 2/1/2008. (NON-CONFIDENTIAL)
	* * * * *
3/31/2010	Brief of Plaintiff-Appellant Gilbert P. Hyatt on Rehearing En Banc. BY Gilbert P. Hyatt (Appellant). SERVED BY Mail ON 3/31/2010. FILED ON 3/31/2010. (NON-CONFIDENTIAL)
	* * * * *

DATE	PROCEEDINGS
5/3/2010	Brief for the Director of the United States Patent and Trademark Office on Rehearing En Banc. BY David Kappos, Director, U.S. Patent and Trademark Office (Appellee). SERVED BY Mail ON 5/3/2010. FILED ON 5/3/2010. (NON-CONFIDENTIAL)
	* * * * *
5/20/2010	Reply Brief of Plaintiff-Appellant Gilbert P. Hyatt on Rehearing En Banc. BY Gilbert P. Hyatt (Appellant). SERVED BY Mail ON 5/20/2010. FILED ON 5/20/2010. (NON-CONFIDENTIAL)
	* * * * *

UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF COLUMBIA

No. 1:03-cv-00901-HHK

GILBERT P. HYATT, PLAINTIFF

v.

JAMES E. ROGAN, HON. UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE, DEFENDANT

DOCKET ENTRIES

DATE	DOCKET NUMBER	PROCEEDINGS
		* * * * *
04/16/2003	3	COMPLAINT against JAMES E. ROGAN (Filing fee $ 150.), filed by GILBERT P. HYATT. (bcs,) (Entered: 04/25/2003)
		* * * * *
07/17/2003	13	ANSWER to Complaint and Affirmative Defense by JAMES E. ROGAN. (Ball, David) (Entered: 07/17/2003)
		* * * * *

DATE	DOCKET NUMBER	PROCEEDINGS
12/30/2003	23	MOTION for Summary Judgment by JAMES E. ROGAN. (Attachments: #1 #2 #3 #4) (//Fields, Rhonda) (Entered: 12/30/2003)
12/30/2003	24	MOTION for Partial Summary Judgment by GILBERT P. HYATT. (Lewis, Wilma) Additional attachment(s) added on 1/9/2004 (bcs,). Additional attachment(s) added on 1/9/2004 (bcs,). Additional attachment(s) added on 1/30/2004 (bcs,). Modified on 1/27/2005 (lc,). (Entered: 12/30/2003)
	* * * * *	
01/05/2004	27	MEMORANDUM of points and authorities in support of defendant's motion 22 for summary judgment from JAMES E. ROGAN. "FILED UNDER SEAL" (bcs.) (Entered: 01/09/2004)
	* * * * *	

DATE	DOCKET NUMBER	PROCEEDINGS
01/27/2004	29	Memorandum in oppostion to motion re 24 filed by JAMES E. ROGAN. (Fields, Rhonda) (Entered: 01/27/2004)
		* * * * *
01/29/2004	31	Memorandum in opposition to motion re 23 for summary judgment filed by GILBERT P. HYATT. (Attachments # 1 Affidavit in Support of Opposition # 2 Supplement Statement of Material Facts #3 Exhibit 1 #4 Exhibit 2 #5 Exhibit 3 #6 Exhibit 4 #7 Exhibit 5 #8 Exhibit 6 #9 Exhibit 7 #10 Exhibit 8 #11 Exhibit 9 #12 Exhibit 10 #13 Exhibit 11) (Lewis, Wilma) (Entered: 01/29/2004)
		* * * * *
03/01/2004	35	ADMINISTRATIVE RECORD Joint Submission by GILBERT P. HYATT. (Lewis, Wilma) (Entered: 03/01/2004)
		* * * * *

DATE	DOCKET NUMBER	PROCEEDINGS
03/01/2004	37	REPLY to opposition to motion re 23 Reply to Hyatt's Opposition to Defendant's Motion for Summary Judgment filed by JAMES E. ROGAN. (Fields, Rhonda) (Entered: 03/01/2004)
03/01/2004	38	REPLY to opposition to motion re 24 Partial Summary Judgment filed by GILBERT P. HYATT. (Attachments: #1 Exhibit 9 #2 Exhibit 10) (Lewis, Wilma) (Entered: 03/01/2004)
		* * * * *
03/23/2004	40	REPLY to opposition to motion re 23 summary judgment filed by GIBERT P. HYATT. (Lewis, Wilma) (Entered; 03/23/2004)
		* * * * *

DATE	DOCKET NUMBER	PROCEEDINGS
09/30/2005	46	Memorandum granting 23 Motion for Summary Judgment, denying 234 Motion for Partial Summary Judgment (Kennedy, Henry) (Entered; 09/30/2005)
09/30/2005	47	JUDGMENT in favor of defendant against plaintiff (Kennedy, Henry) (Entered: 09/30/2005)
	* * * * *	
11/21/2006	56	NOTICE OF APPEAL to USCA for the Federal Circuit as to 55 Order on Motion for Reconsideration, 46 Order on Motion for Summary Judgment, Order on Motion for Partial Summary Judgment, 47 Judgment by GILBERT P. HYATT. Filing fee $ 0.00. Fee Status: No Fee Paid. Parties have been notified. (lc,) Modified on 11/27/20116

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The field of the present invention is memory systems and, in particular, integrated circuit RAMs for digital systems.

PRIOR ART

The prior art in memory systems includes integrated circuit, core, bubble, CCD, and other types of memory systems. The most pertinent prior art is integrated circuit RAM systems. The prior art provides RAMS having tristate control for memory data lines to permit bussing of memory data lines and to facilitate bidirectional communication to the RAM for reading and writing of information from the bus. The prior art provides double buffer memories which require double the memory capacity of single buffer memories.

SUMMARY OF THE INVENTION

The present invention is generally directed to improved memory architecture. Speed improvement is obtained by a combination of addressing the memory at a relatively low rate and scanning information out of the memory at a relatively high rate. This may be characterized as a multi-dimensional memory architecture, where the addressing logic forms a first dimension and the scanout logic forms a second dimension. This speed improvement can be implemented by using the memory tristate control logic for data scanout operations in conjunction with addressing logic to provide both, re-addressing and scanout of memory data. Additional speed improvement is obtained by a multiple buffer arrange-

ment for storing information and for processing this information with a multiple processing of the same information in different relationships, such as with a spatial filter.

BRIEF DESCRIPTION OF THE DRAWINGS

A better understanding of the present invention may be obtained from a consideration of the detailed description hereinafter taken in conjunction with the drawings, which are briefly described below.

Fig 1 is a block diagram representation of an arrangement for implementing the system of the present invention.

Fig 2 is a block diagram representation of an arrangement for implementing the addressing and architecture of the memory of the present invention.

Fig 3 is a diagram of an address generator partitioned into an X-address component and a Y-address component.

Fig 4 is a diagram of an address generator concatenating an X-address component and a Y-address component.

Fig 5, comprises Figs 5A to 5D: where Fig 5A is a block diagram representation of a spatial filter arrangement; Fig 5B is a block diagram representation of a sum-of-the-products arrangement that can be used with the arrangement of Fig 5A; Fig 5C is a block diagram of a 3-channel sum-of-the-products. arrangement; and Fig 5D is a block diagram of a multiple channel buffer memory.

Fig 6, comprises Figs 6A to 6AF: where Fig 6A is a block diagram representation of a system configuration

for implementation of the present invention; Fig 6BF a detailed is schematic diagram of clock steering logic; Fig 6C is a detailed schematic diagram of clock gating logic; Fig 6D is a detailed schematic diagram of control logic; Fig 6E is a block diagram of a configuration for implementing the memory of the present invention; Fig 6F is a detailed schematic representation of logic for addressing and scanning-out memory information in accordance with the the memory of Fig 6E; Figs 6G to 6J are detailed block diagram representations in accordance with the memory of Fig 6E; Figs 6K to 6N are detailed schematic diagram representations in accordance with the memory of Figs 6F and Figs 6G to 6J; Figs 6O and 6P are detailed schematic diagram representations of one configuration of an address generator that can be used in the system of the present invention; Figs 6Q and 6R are detailed schematic diagram representations of another configuration of an address generator that can be used in the system of the present invention; Fig 63 is a detailed schematic diagram representation of a video DAC channel; Fig 6T is a detailed schematic diagram representation of a video synchronization pulse generator and clock pulse generator; Fig 6U is a detailed schematic diagram representation of joystick interface logic; Fig 6V is a detailed schematic diagram representation of joystick analog to digital converters; Fig 6W is a detailed schematic diagram representation of an address counter arrangement for loading a multiple buffer memory and related logic; Fig 6X is a detailed schematic diagram representation of an address counter arrangement for unloading a multiple buffer memory and related logic; Fig 6Y is a detailed schematic diagram representation of a first channel address multiplexer and RAM arrangement for a multiple channel buffer memory; Fig

6Z is a detailed schematic diagram representation of a first channel RAM input/output multiplexer arrangement for a multiple channel buffer memory; Fig 6AA is a detailed schematic diagram representation of a second channel address multiplexer and RAM arrangement for a multiple channel buffer memory; Fig 6AB is a detailed schematic diagram representation of a second channel RAM input/output multiplexer arrangement for a multiple channel buffer memory; Fig 6AC is a detailed schematic diagram representation of a third channel address multiplexer and RAM arrangement for a multiple channel buffer memory; Fig 6AD is a detailed schematic diagram representation of a third channel RAM input/output multiplexer arrangement for a multiple channel buffer memory; Fig 6AE is a detailed schematic diagram representation of a forth channel address multiplexer and RAM arrangement for a multiple channel buffer memory; Fig 6AF is a detailed schematic diagram representation of a forth channel RAM input/output multiplexer arrangement for a multiple channel buffer memory; Fig 6AG is a detailed schematic diagram representation of a 9-pixel kernel register arrangement for spatial processing; Fig 6AH is a detailed schematic diagram representation of a weight RAM arrangement for spatial processing.

Fig 7 is a detailed flow diagram representation of the BASIC PROGRAM LISTING FTR.ASC for filtering images.

To facilitate disclosure of the illustrated embodiments, the components shown in Figs 1 to 7 of the drawings have been assigned reference numerals and a description of such components is given in the following detailed description. The components in the figures

have in general been assigned reference numerals, where the hundreds digit of each reference numerals corresponds to the figure number. For example, the components in Fig 1 had reference numerals between 100 and 199 and the components in Figure 2 have reference numerals between 200 and 299, except that a component appearing in successive drawing figures has maintained the first reference numeral.

GRAPHICS PROCESSOR

A graphics processor architecture can be implemented with a address generator and control logic generating graphics vectors for storing into image memory. Image memory can then be scanned out, such as in a raster scan form to refresh a display. In one configuration, graphics vectors can be written into image memory on an offline basis and can be used to refresh the display on an online basis. Alternately, graphics, vectors can be written into image memory on an online basis time shared with refreshing of the display on an online basis.

One arrangement of the graphics system of the present invention is shown in Fig 1. Supervisory processor 115A loads graphics commands into address generators 115B. Address generators 115B generate addresses of graphics vectors for loading into image memory 115C and for raster scanning image memory 115C. The raster scan addresses scan-out the image in image memory 115C through the CRT interface 115D to refresh CRT 115E.

An experimental system has been constructed to demonstrate operation of the graphics display capability. The arrangement shown in Fig 1 has been implemented in hardware for refreshing the display in real time. A

program, such as the BASIC PROGRAM LISTING GRAPH.ASC, can be used to control that experimental hardware for refreshing the display. In this experimental system, the graphics vectors are loaded in an offline manner with the LD.ASC Basic program set forth in the BASIC PROGRAM LISTING LD.ASC herein; emulating hardware loading of graphics vectors in an online manner. In this experimental system, graphics operation is initiated each frame with supervisory processor 115A and hardware refresh is performed with address generators 115B and image memory 115C.

In a hardware configuration, graphics vector generation can be performed in real time using the software emulated vector generation capability implemented in hardware form; In one hardware configuration, graphic vectors can be generated cotemporaneously with refresh, such as with one set of address generators (i.e., the XR-address generator and the YR-address generator shown in Figs 6Q and 6R) generating graphics vectors into image memory while a second set of address generators (i.e., the XP-address generator and the YP-address generator shown in Figs 6O and 6P) are generating the raster scan addresses for scanning-out image memory for display. In this configuration, image memory can be implemented as a dual-ported image memory for simultaneously loading vectors into image memory and scanning out image memory. In an alternate hardware configuration, graphic vectors can be generated and loaded into image memory during the vertical sync pulse period when the raster scan is blanked; time sharing the logic and memory between raster scanout and graphics generation. In this configuration, during the vertical sync period, the address generators can generate graphic vector addresses for loading the graphic

vectors into image memory and, after the vertical sync period, the address generators can generate the raster scan addresses for scanning-out image memory for display.

The address generators can be used to generate graphic vectors and windows. For example, the LD.ASC program set forth in the BASIC PROGRAM LISTING LD.ASC herein has been used to load graphic vectors into image memory. This is achieved by using the address generators to generate the addresses of a vector and by strobing the color intensity of the vector into image memory.

Periods of time exist when the address generators are in a stand-by condition. For example, in a configuration where the address generators are scanning out image memory to refresh a display; the address generators may not be used during the vertical blanking period and therefore may be available for graphic generation. Also, in a configuration where the address generators are not used during the horizontal blanking period, the address generators and therefore may be available for graphic generation during the horizontal-blanking period. For example, a vertical blanking period of 1-millisecond will permit the address generators to draw about 5,000-graphic vector pixels operating at a 5-MHz pixel rate. Consequently, a meaningful number of graphic vector pixels can be generated during standby periods, permitting time sharing of the address generators for both, scanning-out an image to refresh a display and graphic vector generation.

A vector memory can be implemented to store parameters associated with the vectors to be generated. Vector memory can be loaded from various sources, such as

from the supervisory processor that initializes the address generators, from a host processor, or from other sources. The vector memory can contain the start point coordinates and the vector deltas for the address generators and a quantity parameter or distance-to-go (DTG) parameter related to the quantity of vector steps to be generated for the particular vector. During image processing standby periods, graphic vector-parameters can be loaded from the vector memory for generating the vectors with the address generators, similar to that performed with the LD.ASC program. After various standby periods, such as the horizontal and vertical synchronization periods; the address generators can be reinitialized; thereby overcoming the need to buffer scanout parameters. However, if the address generators will not be reinitialized following vector generation, it may be necessary to buffer the scanout address parameters in a buffer memory for reloading the pixel address generators after vector generation.

In the LD.ASC program, the number of steps for a vector are counted under program control in the supervisory processor. In a hardwired implementation, the number of steps for a vector can be counted with a hardware counter circuit. For example, the quantity or DTG parameter from the vector memory can be loaded into a 74LS169 counter as a parallel load parameter and the counter can be decremented in the count-down mode for each pixel step during vector generation. Generation of the vector can be terminated by detecting the underfloor signal from the counter at the zero count.

Loading of the address generators from the vector memory can, be performed in a manner similar to loading the address generators from the supervisory proces-

sor, as shown in the LD.ASC program listing herein and as discussed relative to the supervisory processor interface herein. Setting of the vector color intensity from the vector memory can be performed in a manner similar to setting of the vector color intensity from, the supervisory processor in the LD.ASC program. Selecting of the write-mode for the image memory can be performed in a manner similar to setting of the write-mode with the load command signal DOA6 by the supervisory processor in the LD.ASC program.

Window generation can be implemented with parameters for a plurality of images stored in a window buffer memory and selected as the address generators scan across window boundaries during scanout and refresh of the CRT monitor. When the address generators cross window boundaries, the previous display parameters can be buffered in the buffer memory and the display parameters associated with the new image can be loaded from the window buffer memory into the address generators. Loading of display parameters associated with the new image from the window buffer memory can be accomplished as discussed above for loading of vector parameters during graphic vector generation. Storing of display parameters associated with the prior image into the window buffer memory can be accomplished by reversing the vector generation loading operation to obtain a window generation store operation.

SPATIAL FILTERING

General

Display systems can be implemented with spatial filters for anti-aliasing, pattern recognition, enhancement, and other purposes. A spatial filter arrangement will now be discussed with reference to Figs 5A to 5C.

Fig 5A shows an arrangement of a display system. Address generator 520A generates pixel addresses to access a plurality of pixels, such as a 9-pixel kernel 520H, from image memory 520B. Pixel information can be latched in registers to provide parallel pixel words or can be accessed sequentially as provided with the BASIC PROGRAM LISTING FTRASC herein. Weight table 520C supplies a plurality of kernel weights appropriate to spatial filtering of the pixel kernel, such as a kernel of 9-weights 52oI, from weight table 520C. Weight information can be latched in registers or in the weight table to provide parallel pixel words or can be accessed sequentially as provided with the BASIC PROGRAM LISTING FTR.ASC herein. The pixel intensities I0 to I8 are each applied to a corresponding multiplier 520E and the weights W0 to W8 are each applied to a corresponding multiplier 520E for multiplying the corresponding intensity and weight together to generate product signals 520J. Product signals 520J are summed together with summer 520F to generated a weighted and mixed pixel intensity, which is converted to analog signal form with DAC 520G to excite a CRT display.

The arrangement discussed with reference to Fig 5A is representative of a single color channel, such a single channel of a multiple color pixel; i.e., a red, green, or blue channel; and such as a monochromatic single channel. Intensity information INT and weight information WT can be input to multipliers 521A for weighting the pixel intensities, which in turn can be input to adders 521B and 521D for generating weighted and summed signal 521D. Three channels of the arrangement discussed with reference to Fig 5B can be combined to provide a 3-channel color spatial filter. For example, as shown in Fig 5C, 3-channels of intensity and weight in-

formation 521E are processed with sum-of-the-products logic 521F to generate 3-channels of signals 521G; such as red, green, and blue signals 521D.

The sum-of-the-products processing discussed above can be implemented with commercially available integrated circuit components, such as multiplier chips and adder chips. For example, multiplier chips are manufactured by TRW and adder chips are manufactured by Texas Instruments.

Description of Fig 7 and the FTR.ASC Listing

A filter processor can be emulated in software to illustrate operation of a hardware configuration. One filter processor configuration is shown in the BASIC PROGRAM LISTING FTR.ASC a provided herewith and is shown in flow diagram form in Fig 7. This program provides for accessing of pixels from the database, filtering the pixels, and storing the filtered pixels in another file in the database. The unfiltered file is defined as UNFILTER.ASC and the filtered filed is defined as FILTERED.ASC. In this configuration, the database is constructed as 8-stripes, each stripe having 64-lines, and each line having 512-pixels. This comprises an image 512-lines by 512-pixels per line. The image database is constructed as a packed byte per pixel with 128-pixels stored in a sector on the disk. The Basic program FTR.ASC accesses the binary file as a Basic random file and unpacks the pixels for filtering under the Basic program. For convenience of implementation, 2-pixels at a time are unpacked for filtering and 2-pixels at a time are packed after filtering.

The filtering program will now be discussed with reference to the flow diagram in Fig 7. The program is implemented with a plurality of loops. The outer loop KRLP1 defines the vertical coordinate of the pixel kernel. The next inner loop KPLP1 defines the horizontal coordinate of the pixel kernel. The next inner loop OUTLP1 defines the vertical coordinate of the pixel line in the kernel. The next inner loop KPLP1 defines the horizontal coordinate of the pixel pair on the pixel line in the kernel. The program processes 3-pixels per line in the kernel with 2-iterations through the inner loop INLP1, then processes 3-lines in the kernel with 3-iterations through the next outer loop OUTLP1, then processes 512-kernels per line with 512-iterations through the next outer loop KPLP1, and then processes 64-lines of. kernels per stripe with 64-iterations through the outer loop KRLP1.

The flow diagram (Fig 7) is drawn with elements having descriptive labels that correspond with the program operations. The line numbers associated with these operations are listed. above the elements for convenient cross-referencing to the Basic program FTR.ASC. Reference numerals 760A to 760AB are shown with connecting lines to the elements for convenient cross-referencing in the description.

Execution commences by generating initial conditions in element 760A. Operation then proceeds to the outer loop KRLP1 760B to address the first kernel position at the top edge of the kernel array and then proceeds to the next inner loop KPLP1 760C to address the first kernel position at the left edge of the kernel line. Operation then proceeds to element 760D to initialize the KPLP1 loop by generating the initial conditions KB, YB,

KB, YE, and BDC. Operation then proceeds to the next inner loop OUTLPI 760E to address the top line of pixels in the kernel. Operation then proceeds to element 760F to access a database record corresponding to the top line of pixels in the kernel. Operation then proceeds to the inner loop INLP1 760G to address the pair of pixels at the leftmost side of the kernel in the selected line.

Operation then proceeds to element 760H to access and unpack a pixel pair and then to element 760X to select the weights for the selected pixel line. Operation then proceeds to element 760Y to test the S1-flag for processing of either the first pixel pair or the second pixel pair. If the S1-flag is 0-set, indicative of processing of the first pixel pair; operation proceeds along the 0-path to element 760AA to weight the first pair of. pixels and to sum the weighted pixels in a partial summation. Operation then proceeds to element 760AB to 1-set the S1-flag, indicative of the need to process the second pixel pair on the next iteration. In element 760Y, if the S1-flag is 1-set, indicative of processing the second pixel pair; operation proceeds along the 1-path to element 760Z to weight the second pair of pixels and to sum these weighted pixels with the partial sum previously generated with the first pair of weighted pixels. Only the first pixel of the second pair of pixels is processed, where a 3-pixel line for a kernel is implemented with both pixels of the first pixel pair and the first pixel of the second pixel pair.

Operation then proceeds to element 760J to define the next pixel pair on the selected line of pixels and then to element 760K to determine if the last pixel pair per pixel line in the kernel has been processed. If the last pixel pair of the kernel has not been processed, operation

branches along the Y-path looping back in the INLP1 loop to access the next pixel pair on the selected line of pixels. If the next pixel pair of the kernel has been processed, operation branches along the N-path to exit the INLP1 loop, then to element 760L to 0-set the S1-flag, and then to element 760M to determine if the last pixel line of the kernel has been processed. If the last pixel line of the kernel has not been processed, operation branches along the Y-path looping back in the OUTLP1 loop to access the next line of pixels in the kernel and to iterate through the INLP1 loop to access the kernel pixels on that line and to filter these kernel pixels. If the last pixel line of the kernel has been processed, operation branches along the N-path to exit the OUTLP1 loop and then to element 760N to test the S2-flag.

The S2-flag identifies whether the filtered pixel is the first or second pixel in a pixel pair. If the pixel is the first pixel in a pixel pair identified by the S2-flag being 0-set, operation branches along the 0-path to element 760P to 1-set the S2-flag indicative of the first pixel pair being processed and then to element 760Q to scale the filtered pixel and to buffer the filtered pixel. If the pixel is the second pixel in a pixel pair identified by the S2-flag being 1-set, operation branches along the 1-path from element 760N to element 760R to scale a second filtered pixel and to element 760S to store the filtered pixel pair in the database and to 0-set the S2-flag as indicative of the first pixel of the next pixel pair pending processing.

Operation then proceeds to element 760U to determine if the last kernel per kernel line has been processed. If the last kernel per line has not been processed, operation branches along the Y-path looping

back in the KPLP1 loop to process the next kernel along the line of kernels. If the last kernel per line has been processed, operation branches along the N-path to element 760V to determine if the last line of kernels has been processed. If the last line of kernels has not been processed, operation branches along the Y-path looping back in the KRLP1 loop to process the next line of kernels. If the last line of kernels has been processed, operation branches along the N-path to element 760W to exit the filtering of the stripe.

Filtering of Images

Image processing can be performed on digitized images stored in the database. A stored image can be loaded from the database into image memory for image processing online with a hardware-implemented image processor. A stored image can be preprocessed, such as offline in the database and such as online with a preprocessor. Offline processing can be performed during database generation, such as filtering database images before storing the images in the database. Online preprocessing can be performed during system operation, such as by accessing database images and preprocessing the accessed database images with compression and filtering, prior to loading into image memory. Offline preprocessing can be performed for filtering of images, which is illustrative of other forms of offline preprocessing and is also illustrative of online preprocessing. For example, other forms of offline preprocessing includes data compression, image enhancement, and other forms of filtering. Also, other forms of online preprocessing includes data decompression, image expansion, image compression, and filtering.

Offline filtering and the other preprocessing operations illustrated therewith is shown in the BASIC PROGRAM LISTING FTR.ASC provided herein.

For this example, the image is constructed in database memory as 512-lines and 512-pixels per line. Each pixel is implemented with an 8-bit byte having the least significant 3-bits representing green intensity, the next more significant 2-bits representing red intensity, the next more significant 2-bits representing blue intensity, and the most significant bit being presently unused. The image is divided into 8-subimages; where each subimage contains 64-lines in a stripe. The stripes are identified as stripe-0 to stripe-7. For example, the lake image has the topmost stripe stored as the LAKE50.BIN file, the next lower stripe stored as the LAKE51.BIN file, the other stripes stored in the ascending LAKE5n.BIN files and the lowest stripe stored in the LAKE57.BIN file. The filter program accesses each stripe in sequence, filters the stripe, buffers the stripe as the FILTERED.BIN file, and stores the stripe as the FLAKE5n.BIN file. The filtering operation accesses a 'kernel of pixels surrounding the center pixel and consequently overlaps stripes for the first line and the last line in a stripe. Therefore, filtering of each stripe is implemented by accessing the particular stripe as the PRESENT.BIN file, accessing the previous stripe as the PRIOR.BIN file, and accessing the subsequent stripe as the NEXT.BIN file.

In this example, filtering is implemented with a 9-pixel kernel organized in a 3-pixel by 3-pixel array. This filtering is performed by multiplying each of 9-kernel pixels by the corresponding one of 9-kernel weights, summing the weighted pixel intensities, and then scaling

to normalize the filtered intensity. This processing is performed for each of the 3-color components of the kernel pixels. Weights can be assigned to the particular kernel positions, selectable under operator control with the menu. Kernel weights No. 1 and kernel weights No. 2 are shaded, where the weights are decreasing from the kernel center towards the kernel periphery. Kernel weights No. 3 are unshaded. Additional kernel weights can be defined by the operator under control.

MEMORY ARCHITECTURE

General

The memory architecture of the present invention has important advantages in implementing digital systems. It is applicable to special purpose systems; such as display systems, array processors, and pipeline processors; and is applicable to general purpose systems; such as general purpose digital computers. It incorporates various features that may be used individually or in combinations to enhance performance and efficiency. One feature provides for accessing of memory at a relatively slow addressing rate and at a relatively fast scanout rate. Another feature provides a buffer memory to permit accessing of memory at .a lower rate and higher duty cycle for information that is utilized at a higher rate and lower duty cycle. Various other features are also discussed herein.

Memory speed is an important consideration for design of digital systems; such as display systems, array processing systems, and pipeline systems. A configuration is discussed herein where system speed can be implemented to be significantly faster than implied by memory speed considerations. This configuration uses a combination of novel architectural features for output-

ting of relatively high bandwidth information with a relatively low bandwidth memory.

Brief Description

A memory architecture in accordance with the present invention will now be discussed with reference to Figs 1 and 2. Alternate configurations can be provided to implement the system of the present invention. However, this configuration is exemplary of the system of the present invention. Input device 115A generates input information under control of input clock 115G. Address generator 115B generates addresses for memory 115C under control of input clock 115G, such as for storing information from input device 115A into memory 115C or for accessing information from memory 115C under control of input device 115A. Memory 115C outputs information accessed with address generator 115B under control of input clock 115G. Buffer 115D receives information accessed from memory 115C for buffering therein under control of input clock 115G and generates information buffered therein under control of output clock 115F. Output device 115E, such as a display monitor, receives buffered information from buffer 115D under control of output clock 115F. This permits information to be accessed from memory 1150 asynchronous with information to be output to output device 115E. Hence, buffer 115D can input information under control of input clock 1156 and can output information under control of output clock 115F for resynchronizing of information flow, averaging of information rate, reorganizing of information into groups, and for other purposes.

In an alternate configuration, information from memory 115C can be output directly to output device 115E under control of input clock 115G, such as with input

clock 115G and output clock 115F being the same clock and being connected theretogether.

A multi-dimensional address configuration is shown in Fig 2. Address generator 115B generates an address word having a readdressing portion 215E, a Y-scanout portion, 2156, and an Xscanout portion 215F. This arrangement has particular advantages because the X-scanout signal 215F and the Y-scanout signal 215G can be generated more rapidly than re-addressing signal 215E to access or to write into memory 115C.

Memory 115C is shown partitioned onto 2-boards, 215B and 215D. RAMs on the 2-boards can be addressed with re-addressing logic 215E. The RAMs are shown organized in an x-y array of rows and columns. The X-scanout signals are decoded into a plurality of row signals shown radiating horizontally right from t.he X-scanout line 115F. The Y-scanout signals are decoded into a plurality of column signals shown radiating vertically up from the Y-scanout line 115G. The decoded row and column line signals enabled 1-row and 1-column as a function of the X-scanout and Y-scanout address portions, respectively. Consequently, 1-RAM at the intersection of the row and column enable signals is enabled to output the information addressed with re-addressing signal 215E and all other RAMs are disabled from outputting the information addressed with re-addressing signal 215E.

Various address register configurations will now be discussed with reference to Figs 3 and 4. Fig 3 shows a dual address register configuration having an X-address register and a Y-address register. This arrangement is particularly applicable to display systems having a 2-dimensional memory map and generating vectors for

storing into an image memory or for reading out of an image memory. The X-address register and the Y-address register can be separately controlled to generate a 2-dimensional vector for accessing a pixel in the memory. Actually, the 2-address registers can be considered to be concatenated to form a single address parameter for memory accessing. However, two separate 2-dimensional address registers are a convenient way of visualizing a single dimensional memory configured into a 2-dimensional memory map. In a configuration discussed for the experimental system herein, the 6-most significant bits of each register are combined for an 11-bit re-addressing word and a 1-bit board select signal while the 3-least significant bits of each register are separately decoded to select one of 8-rows and one of 8-columns on each board in accordance with. the X-scanout signal 215F and Y-scanout signal 215G discussed with reference to Fig 3.

Fig 4 shows a single address register configuration. which can be implemented by concatenating the X-register and Y-register shown in Fig 3 or, alternately, may be conceptually defined as a single register, a quadruple register, or other configurations. Selected bits of this single address register may be used to control re-addressing and row and column select for the memory in accordance with Fig 2. Many configurations of signal groupings can be implemented; such as using signals XA0, XA1, XA4, XA6, YA3, YA4, and YA6 for re-addressing; signals XA3, XA7, YA5, and YA8 for X-scanout decoding; and signals YA0, YA1, YA2, XA2, XA5, XA8, and YA7 for Y-scanout decoding as an alternate to the above configuration discussed with reference to Fig 3.

Memory addressing may be configured in a multi-dimensional form; such as 2-dimensional, 3-dimensional, or 4-dimensional form. For example, address generation may be performed with a plurality of different address generators; such as an X-address generator for one portion of a 2-dimensional address and a Y-address generator for the other portion of a 2-dimensional address, as discussed for a 2-dimensional memory map configuration herein. Also, addresses that are generated with a single address generator can be partitioned into multidimensional addresses; such as a 16-bit computer instruction address being partitioned into a W-dimension address for the most significant 4-bits, an X-dimension address for the next less significant 4-bits, a Y-dimension address for the next less significant 4-bits, and a z-dimension address for the least significant 4-bits. Also, a multi-dimensional address, such as the X-dimensional address and Y-dimensional address, for a display configuration, can be concatenated into a single address by combining the different portions thereof; such as combining the Y-address dimension as the most significant portion of the address word and the X-address dimension as the least significant portion of the address word.

In describing the novel architecture of the memory of the present invention, the word "dimension" and words relating thereto have been adapted to mean the different forms of addressing the RAMs. For example, the RAMs are addressed with a re-addressing portion of the address and a scanout portion of the address, which may be considered to be 2-dimensional addressing, and the scanout portion of the address are divided into row select signals to the G-bar pins and column select signals to the S-bar pins of the RAMs, which may be considered

to be 2-dimensional scanout addressing. A memory having an address with the combination of a 1-dimensional re-addressing portion and a 2-dimensional scanout portion may be considered to be a 3-dimensional memory. This terminology is different from terminology associated with 2-spatial dimensions of an image, such as implemented in a memory map, and 2-spatial dimensions of an image, such as displayed on a monitor.

The memory arrangement discussed herein can be applied to a display system, as discussed in greater detail herein. Image pixels can be accessed in sequence for output to a display monitor. The memory can be configured in a 2-dimensional form, such as 1-dimension being the data block address and the other dimension being the pixel address within a block. Alternately, the address can be partitioned into a plurality of bytes from a least significant byte to a most significant byte and each byte can be used to address a 'different dimension of the memory. Image memory scanout can be implemented by scanning sequential addresses at a higher rate and by re-addressing the memory at a lower rate, such as with a gated clock. A gating signal can be used to gate the memory access clock without gating the output clock, such as a DAC clock; permitting display operations to proceed under control of the non-gated output clock without being affected by gating of the memory clock. An output buffer memory can be used to temporarily store pixel information to reduce sensitivity of the display to gating of the memory clock. A buffer memory also permits accessing of the image memory at a relatively high duty cycle even though the information may be output to the display, at a lower duty cycle, or at a relatively low portion of the time that the memory information is available, or by not utilizing the information

immediately after the information becomes available from the image memory. A buffer memory also permits accessing of image memory substantially as fast as image memory can be accessed, reducing constraint from output speed considerations.

The memory arrangement discussed herein can also be applied to a correlator processor memory. Data can be accessed in sequence for execution by the correlator. The memory can be configured in a 2-dimensional form, such as 1-dimension being the data block address and the other dimension being the data address within a block. Alternately, the address can be partitioned into a plurality of bytes from a least significant byte to a most significant byte and each byte can be used to address a different dimension of the memory. Data scanout can be implemented by scanning sequential addresses at a higher rate and by readdressing the memory at a lower rate, such as with a gated clock. A gating signal can be used to gate the memory access clock without gating the output clock, permitting correlator operations to proceed under control of the non-gated output clock without being effected by gating of the memory clock. A buffer memory can be used to temporarily store correlation information to reduce sensitivity of the correlator to gating of the memory clock. A buffer memory also permits accessing of the correlator data at a relatively high duty cycle even though the information may be processed at a lower duty cycle, or at a relatively low portion of the time that the memory information is available, or by not utilizing the information immediately after the information becomes available. A buffer memory also permits accessing of correlator data substantially as fast as the data memory can be accessed, reducing constraints from output speed considerations.

The memory arrangement discussed herein can also be applied to memory. Data can be accessed in sequence for execution by the FFT processor. The memory can be configured in a 2-dimensional-form, such as 1-dimension being the data block address and the other dimension being the data address within a block. Alternately, the address can be partitioned into a plurality of bytes from a least significant byte to a most significant byte and each byte can be used to address a different dimension of the memory. Data scanout can be implemented by scanning sequential addresses at a higher rate and by readdressing the memory at a lower rate, such as with a gated clock. A gating signal can be used to gate the memory access clock without gating the output clock, permitting FFT operations to proceed under control of the non-gated output clock without being effected by gating of the memory clock. A buffer memory can be used to temporarily store FFT information to reduce sensitivity of the FFT processor to gating of the memory clock. A buffer memory also permits accessing of the PVT data at relatively high duty cycle even though the information may be processed at a lower duty cycle, or at a relatively low portion of the time that the memory information is available, or by not utilizing the information immediately after the information becomes available. A buffer memory also permits accessing of FFT data substantially as fast as the data memory can be accessed, reducing constraints from output speed considerations.

The memory arrangement discussed herein can also be applied to general purpose computer memory. Instructions can be accessed in sequence for execution by the computer arithmetic and control logic. The memory can be configured in a 2-dimensional form, such as

1-dimension being the instruction or data block address and the other dimension being the instruction or data address within a block. Alternately, the address can be partitioned into a plurality of bytes from a least significant byte to a most significant byte and each byte can be used to address a different dimension of the memory. Instruction and data scanout can be implemented by scanning sequential addresses at a higher rate and by re-addressing the memory at a lower rate, such as with a gated clock. A gating signal can be used to gate the memory access clock without gating the output clock, permitting processing to proceed under control of the non-gated output clock. without being effected by gating of the memory clock. A buffer memory can be used to temporarily store computer instructions and data to reduce sensitivity of the computer to gating of the memory clock. A buffer memory also permits accessing of the computer instructions and data at a relatively high duty cycle even though the information may be processed at a lower duty cycle, or at a relatively low portion of the time that the memory information is available, or by not utilizing the information immediately after the information becomes available. A buffer memory also permits accessing of computer instructions and data substantially as fast as the memory can be accessed, reducing constraints from output speed considerations.

Memory architectural features pertaining to high speed scanout in conjunction with re-addressing can provide speed enhancement, such as a 3-fold improvement in speed. These feature are particularly pertinent to RAMs having multiple tristate control signals; such as the Mitsubishi Electric M58725P RAMs. RAMs having a single tristate control signal can also tie used with

this configuration, but may involve additional decoder logic to decode scanout address signals, such as with linear select architecture consistent with a single tristate control signal.

The memory architecture of the present invention may be discussed in the content of a display application for purposes of illustration. However, this memory architecture is applicable to computer main memories, 'buffer memories, signal processing memories, and other memory applications in addition to display memories.

Re-Addressing And Scanout Memory Architecture

Multiple dimension image memory architecture, as previously discussed, involves simultaneous accessing of multiple pixels, such as in a 2-dimensional X/Y array, to increase effective memory speed. Such a configuration is appropriate for a 2-dimensional horizontal and vertical scanout for refreshing a display monitor and is also appropriate for other applications; such as general purpose computers and special purpose processors. Such a memory architecture may need buffer registers for temporary storage of accessed information, such as for temporary storage of accessed pixels so that a new memory access cycle may be initiated while the previously accessed pixels are being output to refresh the display monitor. An alternate configuration is discussed herein where a block of pixels is simultaneously accessed and is scanned-out without the need for buffer registers or overlapping memory accesses. This configuration can involve a multiple access period, where stored information is scanned out from an accessed block at high rate (shorter period) and a new block of stored information is accessed at a lower rate (lower period). A buffer

memory, such as a FIFO or a double buffer memory, can be used to equalize these rate and period differences.

A novel memory architecture will now be discussed which enhances memory speed and economy. This architecture can be characterized as a multi-dimensional memory architecture that is divided into 2-address portions, a high speed address portion and a slow speed address portion. Another characteristic is a combination scanout and re-addressing architecture. Another characterization is use of tristate memory control logic to reduce the need for buffer registers and multiplexing logic. This can be accomplished by taking advantage of certain features of RAMs.

Conventional RAMs have a plurality of input address lines for addressing stored information, tristate output data direction control logic for selecting data input for writing and data output for reading, and tristate chip select logic for gating output-information onto a bus. Use of these circuit features in a novel form implemented in the memory architecture described herein provides important advantages. For example, tristate data input and output control logic can be used in conjunction with tristate chip select logic to provide a high speed 2-dimensional scanout for rapid accessing of RAMs. The 2-dimensional scanout arrangement reduces auxiliary decoding and selection logic, reduces output buffer logic, is compatible with 2-dimensional memory map architectures, and facilitates relatively high speed operation with relatively low speed RAMs.

Higher speed scanout can be used in conjunction with slower speed addressing of the RAMs to provide an average access rate that is significantly higher than the addressing rate. For example, the Mitsubishi Electric

M58725P RAMs have a 200-ns address period, and a 100-ns scanout period. Assuming that a system will scanout 4-parameters before re-addressing is necessary and assuming that re-addressing is implemented with 3-scanout clock periods, 5-parameters can be accessed in 7-clock periods; 4-parameters times 1-clock period per parameter plus 1-parameter times 3-clock periods per parameter; in comparison to conventional re-addressing, where 5-parameters can be accessed in 15-clock periods (5-parameters times 3-clock periods/parameter). This scanout and re-addressing example yields an average of 1.4-clock periods per pixel for the scanout and re-addressing configuration compared to 3-clock periods per pixel for the readdressing configuration, yielding an improvement of about 2-times in speed for this example.

RAMs are conventionally addressed with a number of address lines, such as 11-address lines for a 2,048 word RAM. Address signals typically propagate through the memory array and consequently can have relatively long propagation delays. RAMs conventionally have tristate enable signals to permit bussing of output signals and to select data input for storing and data output for accessing of data. The tristate enable signals can be used to gate the RAM outputs and consequently can have relatively short propagation delays.

The present multi-dimensional memory configuration uses less frequent accessing of data with the slower address signals (readdressing) and uses more frequent accessing of data with the faster scanout control signals. Therefore, the average propagation delay is reduced, being a weighted average of several shorter scanout propagation delays and a single longer address propagation delay.

Speed is enhanced by changing the clock period to be a function of the addressing operation, such as a longer clock period for re-addressing and a shorter clock period for scanout. A buffer memory; such as a FIFO, double buffer, cache, or scratchpad memory; can be used to buffer output information from the memory for providing a constant memory output clock period in response to the variable memory input clock period.

A specific example will now be provided to illustrate use of relatively longer propagation delay address signals to select a single block of 64-pixels and using relatively shorter propagation delay tristate control signals to select a pixel from the selected block. Each address generator generates a concatenated address having a 3-bit tristate control signal portion and a 6-bit address signal portion. The 3-bit tristate control signal address can be implemented with the least significant bits (LSBs) of the address word and the 6-address bits can be implemented with the most significant bits (MSBs) of the address word. The address generators can be implemented to update the address, where the LSBs can be updated more frequently than the MSBs and where the addresses can scan through a block of pixels as the LSBs are updated and change to a different block of pixels when the MSBs are updated. Updating of the MSBs can be detected with an overflow from the LSBs to the MSBs in the address generator. Therefore, the LSBs can be updated relatively rapidly to scanout with the faster tristate control signals through the pixels within a block and the MSBs can be updated relatively slowly to change the selected block.

For purposes of illustration, an experimental configuration with an image memory having 262,144-pixels ar-

ranged in a 512-by-512 pixel memory map was implemented. Also for simplicity, Mitsubishi 58725P RAMs, Texas Instruments 7400 series TTL logic, and Intel logic is used. The Mitsubishi RAMs have 2K-words by 8-bits per word. Therefore, 128-RAMs are used to provide 262,144-pixels. For efficiency of implementation, the RAMs are 'arranged in two 2-dimensional boards each having a binary quantity (i.e., 8) RAMs for each dimension. Consequently, the 128-RAMs are arranged on.2-boards each having 64-RAMs, arranged in an 8-by-8 block of RAMs per board.

Each RAM has an 11-bit address for accessing one of 2048- words. Another address bit is used in this configuration for selecting one of the two RAM boards. For convenience of discussion, the 11-bit address and the 1-bit board select signals are organized in a 6-bit X-address dimension and a 6-bit Y-address dimension to select one block of 64-pixels out of 4096 blocks of 64-pixels. This arrangement is shown in the memory diagrams and tables included herewith. The memory map contains a 64-by-64 array of blocks for a total of 4096 blocks. The 12-address bits are organized into a 6-bit Y-axis address and a 6-bit X-axis address for a 64-by-64 array of blocks. The 6-bit X-axis address is divided into a 5-bit X-axis address to each RAM and a 6th X-axis address bit to select one of the two 64-RAM boards. Use of the X-address bit as a board select bit causes the 64-by-64 array of RAMs to have alternate X-dimension columns to be selected from different boards. Alternately, use of the most significant X-address bit for the board select bit would cause the 64-by-64 array of RAMs to have all of the X-dimensional RAMs in one board adjacent to each other and all of the X-dimensional RAMs in the other board adjacent to each other.

Each of the 4096-blocks of pixels can be configured in an 8-by-8 array of 64-pixels. One of the 8-by-8 arrays of 64-pixels is Shown in the image memory diagrams and tables included herewith. The 8-by-8 array can be addressed with a 2-dimensional 3-bit by 3-bit address organized in a 3-bit X-address and a 3-bit Y-address format. Each of the two 3-bit address portions can be decoded into 8-address lines, yielding an 8-by-8 array of address lines. If one of the first group of 8-address lines is excited to select a row of pixels and the second group of 8-address lines is excited to select a column of pixels, then the one pixel at the intersection of the row address line and column address line is selected out of the 64-pixels per block.

The memory scanout and re-addressing architecture can be implemented for cutting across image memory lines to generate a vector drawn at an angle to the raster lines and can be efficiently used in a raster scan image memory. For example, raster scan outputs proceed on a line-by-line basis; consistent with the line organization of the image memory. In such an arrangement, a single tri-state control signal can be used for scanout as the line progresses, with re-addressing being performed at block boundaries. In this configuration, a block may be a 1-dimensional line of pixels; in contrast to the above described 2-dimensional array of pixels per block. Block traversing in a 1-dimensional memory system is more nearly constant than in a multi-dimensional memory system. For example, a linear block along a scanline can have all pixels in the block accessed frame-after-frame independent of vector considerations. This may be different from a system having a 2-dimensional scanout block with vectors because a 2-dimensional scanout block may have different numbers of pixels traversed

within a block as a function of the vector parameters. For example, the number of pixels traversed may be a function of the pixel entry point to the block and a function of the scanout vector angle through the block, where the pixel entry point may be a function of vector position and the scanout angle may be a function of vector slope.

The maximum, typical, average, and minimum number of pixels scanned in a block can be different for different configurations. For example, in a raster scan arrangement; all pixels in a block may be scanned for each traverse of the linear block. Therefore, in a 1-dimensional block configuration; the maximum, typical, average, and minimum number of pixels scanned in a block may be the same; which is the total number of pixels per block. In a 2-dimensional block configuration having vector directions, the maximum number of pixels may be the number of pixels along the diagonal of the block; the minimum number of pixels may be a single pixel, such as a scan clipping the corner of a block; and the typical number and average number may be in between the maximum and minimum, such as determined by typical and average block geometry relationships. Consequently, in a linear block raster scanout configuration, greater average scanout rates may be obtained due to the scanout of more pixels per block.

A buffer memory configuration can have the ,form of a multiple buffer, such as a double buffer. Alternately, the memory configuration discussed herein having gated clocks and a plurality of clock periods can be implemented with a smaller buffer memory to average a plurality of clock periods. For example, a 16-word FIFO can be used for loading at an input word rate under con-

trol of the gated clock pulse having a plurality of clock periods and for unloading at a clock rate consistent with the output word rate. The FIFO may be implemented with the S/N 74LS222, S/N 74L6224, or S/N 745225 circuits which provide 16-words having 4-bits or 5-bits. These FIFOs can be configured in parallel to provide the 8-bits per word, as shown for the experimental configuration, or can provide other word sizes.

Memory Enhancement

The output of memory in the experimental configuration can be implemented to propagate down a datapipe to a buffer memory without communication with the front end control logic and address generators. Therefore, it can be considered to be implemented in a pipeline form. This pipeline permits intrducing clock skew, where the clock to the output data pipe can be skewed ahead of the clock to the input at the data pipe. This permits greater speed in view of propagation delay considerations. For example, in the experimental configuration, the output registers are clocked with the 180-degree-phase clock and, consequently, provide a 1.5-clock period for propagation delay. One design consideration for this configuration is that propagation delay through the memory is less than 1/2-clock period or the newer high speed information from the next clock may be clocked into the datapipe with the 1.5-clock period clock.

Memory Map Display Architecture

An architecture of one form of memory map for a display will now be discussed. This memory map stores an image as a 2-dimensional array of pixels. In a monochromatic configuration, each pixel contains 1-intensity parameter. In a color configuration, each pixel contains

3-intensity parameters; red, blue, and green intensity parameters. Additional information can be contained in a pixel word; such as other parameters, flags, and control information. All information for a particular pixel can be packed together in a pixel word. Accessing of a pixel word can be implemented to access all information pertaining to the particular pixel word with .one access or, alternately, can access portions of the pixel word for each of multiple accesses per pixel word. For simplicity of discussion herein, operations on a pixel word may-be discussed as operations on a pixel.

Memory map configurations having 1-dimensional and multi-dimensional architectures have been discussed. Multi-dimensional architectures provide enhanced performance and flexibility, such as by accessing multiple pixels simultaneously.

Multi-dimensional architecture provides important advantages. It provides high speed, because of the addressing of 64-pixels in parallel and because the tristate select signals have shorter propagation delays than the address signals. It provides flexibility, because the tristate select signals can traverse the 64-pixel block at any vector angle and through any continuous sequence of pixels. It provides circuit efficiency because much of the address decode and tristate logic is implemented on the memory chips, because a multi-dimensional addressing arrangement is more efficient than a 1-dimensional addressing arrangement, and because the tristate logic, reduces the need for output registers.

A configuration for simultaneous accessing. of an 8-by-8 2-dimensional array of 64-pixels is shown in Pigs 6E to 6N. A pixel address selects 64-pixels at a time out of the total array of pixels, such as out of 262,144-pixels

in a 512-pixel by 512- pixel array. A subset of the 64-pixel block is then addressed with tristate enable signals, such as chip select and output select signals. Tristate select signals can be used to scan through a 64-pixel block to select a sequence of pixels therefrom.

The experimental configuration has been constructed having a 512-pixel by 512-pixel memory map. For convenience of experimentation, static 16K-RAM chips are used for memory map implementation. Typical circuits are. the TMS-4016 RAM from Texas Instruments Inc. and the M58725P static RAM from Mitsubishi Electric. These circuits are configured in the form of a 2K-word by 8-bit static RAM having an 11-bit address, a tristate chip select, and a tristate output enable. Conventionally, the chip select and output-enable are used to provide output bussing and to reduce the need for an output register. In the present configuration, the chip select and output enable signals are used to provide 2-additional dimensions of memory addressing. For example, the 11-address lines are used to select a block of 64- pixels out of 262,144-pixels; the chip select signal is used to select a column of 8-pixels out of the selected block of 64-pixels; and the output enable signal is used to select a row of 8-pixels out of the selected block of 64-pixels. The selection of a column of 8-pixels and a row of 8-pixels with the chip select signal and the output enable signal selects a single pixel at the intersection of that column and row from the selected block of 64-pixels. Consequently, a 3-dimensional architecture having address selection of a 64-pixel block, chip selection of an 8-pixel column in that block, and output enable selection of an 8-pixel row in that block uniquely selects a single pixel out of 262,144-pixels.

Memory chips have particular characteristics that can be adapted to memory architectures which are particularly appropriate for the systems discussed herein. For example, memory circuits conventionally have address lines and tristate select lines. The address lines are typically used to select a pixel per chip and the tristate select lines are typically used to disconnect undesired chips from the output bus and to reverse data direction for read and write operations. However, use of the address lines to select a block of pixels and use of the tristate select lines to scan through the block of pixels provides particular advantages. The access time from the address select is significantly greater than the access time from the chip select or the output enable select. Therefore, accessing with the chip select and output enable signals can proceed at a significantly faster rate than accessing with the address select.

The address select lines can be excited with the most significant bits (MSBs) of thelt-address and Y-address generated with the address generators. The chip select and output enable signals can be excited with the decoded least significant bits (LSBs) of the X-address and Y-address generated with the address generators. For a 512-pixel by 512-pixel memory map having block of 64-pixels, the 6-MSBs of the Y-address and the 6-MSBs of the X-address can be combined into a 12-bit address to select one 41 4096 blocks of 64-pixels. The 3-LSBs of the Y-address and the 3LSBs of the X-address can be used to select one of 8-rows and one of 8 columns, respectively. As the address generation proceeds within a block of pixels, the address proceeds along a line at the appropriate vector angle through the block as the 3-LSBs of the X-address and the 3-LSBs of the Y-address are updated. When the address update progresses into

the MSBs of either the X-address or Y-address, such as with an overflow; a new block of pixels is accessed and the address generation then proceeds within this new block of pixels along a line at the appropriate angle through the block.

The time period for memory accessing of a new block of pixels can be implemented to be longer than the time period for scanning pixels within a previously accessed block of pixels. This can be provided by scanning the pixels within a block at a higher rate and then accessing a new block at a lower rate. This can be implemented by using a higher clock rate to scan pixels within a block, to detect an overflow condition in the X-address and Y-address generators from the LSBs to the MSBs as being indicative of the need to access a new block of pixels, and to switch over to a lower clock rate for accessing of the new block of pixels.

The arrangement discussed with reference to Figs 6E to 6N illustrates 64-RAM chips-in an 8-by-8 array of chips. Two of these 8x8 arrays of chips are used for a 512-pixel by 512-pixel memory map that is implemented in 64-pixel blocks with 2K-by-8 static RAMs. Each 2K-block array of pixels is selected with 11-bits of the 12-bit address. The particular one of the two 64-chip boards is selected with the remaining bit of the 12-bit address. This is shown with the 5-bits from the X-address and the 6-bits from the Y-address being bussed to all 128-chips of both boards and with 1-bit of the X-address being used to select one of the 2-boards in the uncomplemented state and the other of the 2-boards in the complemented state. The row select and the column select are each implemented by decoding 3-bits with a decoder to generate one of 8-signals to select one of 8-rows and

one of 8-columns, respectively. The 11-address lines are bussed to the address input lines of each RAM chip. The 8-data lines are bussed from the data output lines of each RAM chip. Each column select line is bussed to all 8-chips in the related column for each of the two blocks. Each row select line is bussed to all 8-chips in the related row for each of the 2-boards.

Consequently, the 11-address lines select 2-boards of 64-chips each, the twelfth address line selects one of 2-boards, and the 6 "scanout" lines select one of 64-pixels per board.

Image Memory

An image memory for a display in accordance with the present invention can take various forms; such as being implemented with static RAMs, dynamic RAMs, CCDs, ROMs, and other memory devices. The memory architecture can be a random access, sequential access, block access, or other form of architecture. The image memory can be implemented in an unbuffered form, or in a buffered form; such as with a double buffer, in conjunction with various line buffers, and in conjunction with frame buffers. These various alternatives can be adapted to operate with the present invention based upon the teachings herein showing a detailed design of a RAM image memory using static RAMs and accessed in a block oriented scanout arrangement. This configuration will now be discussed in detail with reference to Figs 6E to 6N.

Address generators for use with the memory arrangement shown in Figs 6E to 6N are discussed with reference to Figs 6O to 6R. The address generators can generate sequential addresses at the appropriate vector angle through image memory. Multiple RAM chips, in

this example all RAM chips, are addressed with the more significant bits of the same address word for simultaneously accessing the corresponding word in each of the multiple RAM chips. The less significant bits of the address word are used to select which of the chips is to be enabled for outputting onto the output bus. The chip enable control is a higher speed control and hence permits higher speed memory operations when scanning out within a memory block and the chip address control is a lower speed control and hence involves lower speed memory operations when re-addressing. Therefore, two types of addressing will be described with reference to Figs 6E to 6N, which are readdressing with the more significant address bits and scanout with the less significant address bits.

Re-addressing is performed with fanout buffers U19A for the Y-address bits and U19D for the X-address bits. These buffers generate the drive current necessary to fanout to a large number of RAM chips. In this configuration, 64-RAM chips are grouped on each of two image memory boards with each board having replicated buffers to facilitate increased speed and modularity. The buffer outputs are applied to the address inputs of the RAM chips. During scanout, the addresses are maintained constant. During readdressing, the addresses are changed.

Scanout is performed with decoders U19B, U19C, and U19E. The less significant address bits are applied to these decoders and decoded into X-address and Y-address signals. The X-address signals select rows of RAM chips and the Y-address signals select columns of RAM chips in a 2-dimensional configuration on each board. Replicating memory address logic on each board

facilitates increased speed and modularity. Each row and each column is composed of 8-RAM chips for an 8-by-8 array of RAM chips per board.

The Y-axis decoder U19B is addressed with the less significant Y-address bits YA0, YA1, and YA2 for decoding of column signals. The decoded column signals are applied to the RAM chip select pin, pin 18, to select the column of RAM chips and are applied to the Intel 8216 bus interface chips associated with that column for outputting to the memory output bus.

Selection of one of the 2-boards is provided with the fourth from the least significant X-address bit XA3 applied to U19B-6 and to the Intel 8216 chip select logic. XA3-bar is used to select memory board-1, XA3 is used to select memory board-2. Therefore, as the scanout proceeds in the X-direction, the same block on alternate boards are selected without re-addressing; effectively providing a 16-column by 8-row aspect ratio of RAM chips. Enabling of U19B with XA3 or XA3-bar to pin-6 is an optional control; where selection of one of two memory boards is performed with the Intel 8216 bus interface logic, as described below. Gating the column addresses U19E-6 with-the XA3 and XA3-bar signals reduces memory power consumption.

The X-axis decoders U19C and U19E are addressed with the least significant X-address bits XA0, XA1, and XA2 for decoding of row signals. Decoder U19C is used for read operations, where the decoded row signals are applied to the RAM data enable pin, pin 20, to select the row of RAM chips for read operations. The RAM data enable control, pin 20, is conventionally used for selecting data direction during read and write operations. However, in this configuration; it is also used to facili-

tate 2-dimensional scanout capability. Decoder U19E is used for write operations, where the decoded row signals are applied to the write control pin, pin 21, to select the row of RAM chips for write operations. The DIEN-bar signal is generated from the computer run/load-bar signal DOA6; enabling U19C-6 for read operations during the run mode when DIEN-bar is 1-set, disabling U19C-6 for read operations during the load mode when DIEN-bar is 0-set, enabling U19E-5 for.wTite operations during the load mode when DIEN-bar is 0-set, and disabling U19E-5 for write operations during the run mode when DIEN-bar is 1-set. Therefore, during the run mode, U19C is enabled for reading image memory and U19E is disabled for preventing writing into image memory. Also, during the load mode, U19C is disabled to prevent reading of image memory and U19E is enabled for permitting writing into image memory. 'Enabling of U19E enables the write pulse W-bar input to U19E-4 to be steered to the appropriate row of RAM chips for writing into the RAM chip that is enabled with the chip select column signal to pin 18.

The RAM chip data lines carry the output byte from the selected RAM chip during read operations and carry the input byte to the selected RAM chip during write operations. A shared bidirectional bus structure is used for bi-directional communication with the RAM chips. Intel 8216 bus interface circuits are used for bi-directional communication between a read bus and a write bus and the RAM chip. Each Intel 8216 can accommodate 4-lines, where Intel 8216 chips are used in pairs; U17A and U18A, U17B and U18B, U17C and U18C, and U17D and U18D; to accommodate the 8-lines of a RAM data byte. As can be seen in the memory schematics (Figs 6E to 6N); on the system bus side, the 8-input uni-

directional lines for each pair of Intel 8216s are connected to different lines on the system write bus and the output unidirectional lines for each pair of Intel 8216s are connected to different lines on the system read bus. On the memory side, the bi-directional input and output buffers of the 8216s are internally connected together to provide 8-bi-directional lines connecting to the 8-lines for each RAM chip associated with the particular pair of Intel 8216s. The design connects the data buses for a pair of columns of RAM chips to a single pair of Intel 8216s. This facilitates a tradeoff of the number of Intel 8216 chips used and the speed of operation.

A pair of NAND-gates U17E and U18E are used to OR the two column select signals associated with the pair of Intel 8216s and to AND the board select signal XA3 or XA3-bar for selection of the pair of Intel 8216s as a function of the selected board and the selected column pair of RAMS on that board. The selected pair of Intel 8216s connect the selected RAM to the input bus or output bus under control of the above described signals.

The run/load-bar signal applied as the DIEN-bar signal on pin 15 of the Intel 8216s selects the direction of data communication. If the DIEN-bar signal is 1-set, indicative of the run mode of operation; the 1-set signal applied to pin-15 of an Intel 8216 commands data output from the RAM data bus to the memory output data bus for reading of RAM. If the DIEN-bar signal is 0-set, indicative of the load mode of operation; the 0-set signal applied to pin-15 of an Intel 8216 commands data input to the RAM data bus from the memory input data bus for writing into RAM.

During read operations, all RAM chips are addressed with the same address signals and one of the RAM chips is selected with a combination of a column select signal and a row select signal. The selected RAM chip will have its output data lines enabled to be applied to the output data bus through the Intel 8216 bus interface chips. The column select signal also selects the Intel 8216 bus interface chips associated with selected column for applying the column-related RAM bus to the data bus for reading.

During write operations, all RAM chips are addressed with the same address signals and one of the RAM chips is selected with a combination of a column select signal and a row-selected write pulse for writing the information from the data lines into the selected RAM chip. The column select signal also selects the Intel 8216 bus interface chips associated with the selected column for applying the input data from the data bus to the RAM chips for writing.

Improved IC Memory Chip

An improved IC memory chip, can be implemented in accordance with the teachings of the present system and can provide important advantages over conventional memory chips. This improved memory chip can have multiple tristate control chip select inputs, similar to the 2-dimensional arrangement of the chip select and data enable signals. Also, each memory chip can have an output register to latch the accessed data, where the output register has an output tristate select with multidimensional selection. The data can be latched for scanout and new data can be accessed with a changing address. The data can be strobed into the output register before re-addressing the RAM, such as with a data hold strobe.

Multiple dimensions of tristate output select, can be implemented, exemplified by the 2D tristate control of the system disclosed herein. 2D, 4D, and other multi-dimensional tristate controls can provide further advantages in decoding and scanning-out from image memory.

Memory Logical Design

The memory implemented for the experimental configuration is implemented in a multiple board arrangement, where each board contains 64-RAMs organized in a logical 8-RAM column by 8-RAM row 2-dimensional array. All RAMs receive the same address. All 8-RAMs in an 8-RAM row receive the same X-select signal, which is different from the X-select signal for all other rows. All 8-RAMs in an 8-RAM column receive the same Y-select signal, which is different from the Y-select signal for all other columns. The input data and output data signals are bussed together for groups of 16-RAMs and interfaced with Intel 8216s for connecting to the system databus.

The regular array of RAMs lends itself to a tabular wire list type of documentation. MEMORY TABLE-A to MEMORY TABLE-D list the interconnections for the 64-RAM array on a board. The RAMs are organized in a physical 4-row by 16-column array comprising row-A to row-D and column-1 to column-8. Each RAM is identified by the physical row-and column designation; where RAM U1A is the RAM that occupies the row-A and column-1 position, RAM U6C is the RAM that occupies the row-C and column-6 position, and the other RAMs occupy the other positions in row-A to row-D and column-1 to column-16.

MEMORY TABLE-A lists the connections for pin-1 to pin-12 of the first group of 32-RAMs. MEMORY

TABLE-B lists the connections for pin-1 to pin-12 of the second group of 32-RAMs. MEMORY TABLE-C lists the connections for pin-13 to pin-24 of the first group of 32-RAMs. MEMORY TABLE-0 lists the connections for pin-13 to pin-24 of the second group of 32-RAMs.

The address connections are the same for all RAMs; where pins 1 to 8, 19, 22, and 23 are connected to an 11-wire address bus; where each bus wire connects the same pin on each RAM. The vertical scanout pin, pin 18, for all 8-RAMs in a logical column are connected together and are connected to the vertical scanout signal from U19B corresponding to the particular logical column. The horizontal scanout pin, pin 20, for all 8-RAMs in a logical row are connected together and are connected to the horizontal scanout signal from U19C corresponding to the particular logical row. The horizontal write pin, pin 21, for all 8-RAMs in a logical row are connected together and are connected. to the horizontal write signal from U19E corresponding to the particular logical row.

The databus connections are the same for all RAMs in a double logical column or single physical column array; where pins 9 to 11 and 13 to 17 are connected to an 8-wire data bus connecting all 16-RAMs in the double logical column or single physical column group. A pair of Intel 8216s connect each 16-RAM databus to the system databus with bi-directional read and write signal paths. Four pairs of Intel 8216s bi-directionally connect all 64-RAMs to the system databus.

Other Memory Configurations

Various configurations of the memory of the present invention have been described, to illustrate how the various features and devices of the memory of the present

invention can be used to implement a system. These configurations are illustrative of a large number of other configurations that can be implemented from the teachings herein.

The memory configuration of the present invention has been discussed relative to implementing a 2D memory map for an image processing system and has briefly been discussed for other applications. It is herein intended that the memory architecture of the present invention be usable with other types of display systems and with other systems, such as computer systems and signal processing systems, that are not display systems.

The memory configuration of the present invention has been discussed in memory map form with an address derived from an X-axis address component and a Y-axis address component. Alternately, other addressing configurations can be implemented; such as a single address component for what may be considered to be a 1D memory, a 3-address component for what may be considered to be a 3D memory map, and other memory addressing configurations.

The memory configuration of the present invention has been discussed with reference to an integrated circuit RAM of the Mitsubishi M58725P-type. However, the teachings of the present invention are also appropriate for other integrated circuit RAMs and are also appropriate for integrated circuit ROMs and other memory technologies.

The memory configuration of the present invention has been discussed for a RAM component having 2-tristate control signals for controlling the tristate input and output of the RAM. Alternately, other numbers of tristate control signals can be accommodated; such as 1-

tristate control signal, 3-tristate control signals, 5-tristate control signals, and other quantities of tristate control signals. The architecture for 2-tristate control signals permits implementation of what may be termed a 2-dimensional scanout arrangement having X-scanout control signals and Y-scanout control signals. Alternately, for a configuration having RAMs with 1-tristate control signal, a memory architecture that may be termed a 1-dimensional scanout arrangement can be implemented having 1-scanout signal to each RAM. The 1-scanout signal may be a single dimensional decode of the scanout portion of the address; such as 6-scanout bits being decoded to 64-RAM control signals with a different one of the 64-control signals going to each RAM tristate control signal input. Alternately, for a configuration having RAMs with more than 2-tristate control signals; such as 3-tristate control signals; a memory architecture that may be termed a multi-dimensional scanout arrangement; such as a 3D scanout arrangement; can be implemented with multiple scanout signals to each RAM; such as 3-scanout signals to each RAM. For example, the scanout portion of the address word can be divided into 3-groups of scanout signals, similar to the 2-groups of scanout signals for the arrangement discussed with reference to Figs 6E to 6N, and 1-signal from each of the 3-groups of scanout signals can be applied to a different one of the 3-tristate control inputs to the RAM for what may be considered to be a 3D-scanout control arrangement.

The memory configuration of the present invention has been discussed for an arrangement that applies the same re-addressing portion of the address word to all RAMs. Alternately, the readdressing portion of the address word can be partitioned to different RAMs; such

as with decoding of a portion of the address and selecting blocks of RAMs with the decoded signals, such as to the chip select pin of the RAMs.

The multi-dimensional memory addressing arrangement discussed herein has been illustrated with reference to RAMs having 2-tristate control pins. Such multi-dimensional addressing can be implemented with a memory having a single tristate control pin, as discussed above, with digital logic to convert the single tristate control pin to a multi-dimensional scanout addressing arrangement. For example, the single tristate control pin, if implemented in complement logic form for selecting with a complement signal, can be accessed with a 2-dimensional scanout arrangement by NANDing the 2-scanout address signals, such as the row select signal and the column select signal, with a NAND-gate to control the single tristate pin of the RAM. Similarly, multiple dimensional scanout control signals can be combined with logic external to the RAM to adapt the external scanout control signals to the particular capabilities of the RAM. For example, a a 6-dimensional scanout arrangement can be adapted for a 3-dimensional tristate controlled RAM by combining the 6-dimensional scanout signals into pairs processed with two input NAND-gates to control the 3-tristate pins. Alternately, this 6-dimensional scanout arrangement can be adapted for a 2-dimensional tristate controlled RAM by combining the 6-dimensional scanout signals into groups of 3-signals processed with 3-input NAND-gates to control the 2-tristate pins.

The memory configuration of the present invention has been discussed for an arrangement that pre-buses the data lines of 16-RAMs into a pre-databus and then

further buses the 16-RAM pre-bused signals together onto a system databus. Other partitioning of bused data signals can be provided. For example, all data signals can be bused together onto the system databus without the intervening pre-busing of the 16-RAM data outputs. Alternately other combinations of RAMs than 16-RAMs can have the data lines pre-bused, such as pre-busing of the data lines of 8-RAMs together.

BUFFER MEMORY

General

A buffer memory can provide important capabilities, such as discussed herein. For example, in a display application; a buffer memory permits the output pixel rate to be independent of the input pixel rate, such as for inputting at a rate consistent with the image processor and image memory characteristics and outputting at a rate consistent with CRT monitor characteristics. Further, it permits the CRT monitor to be relatively independent of discontinuities in the image processor, such as permitting the image processor to change the image processing clock period, without causing an undesirable transient on the CRT monitor. Still further, it permits the image processor to operate for the full blanked and unblanked line periods even though the CRT monitor may only be displaying information during the unblanked period; such as by loading the buffer memory during both, the blanked and unblanked periods, and unloading the buffer memory only during the unblanked periods. Yet further, it permits a multi-pixel kernel to be available to a spatial filter without requiring the image processor to make multiple redundant memory accesses of kernel pixels.

A buffer memory can be implemented in between an image memory and a display monitor to provide various, capabilities. For example, in a spatial filtering arrangement; a buffer memory can provide a 2-dimensional kernel of 9-pixels for each center pixel without the need to provide 9-pixel accesses from the image memory for each center pixel. Also, a buffer memory can provide greater pixel resolution by permitting accessing of a slower image memory during the full line period, blanked and unblanked, at a lower pixel rate and accessing the faster buffer memory during the unblanked line period at a higher pixel rate. Further, a buffer memory permits use of a slower speed image memory because of the ability to access the image memory during the full line period, blanked and unblanked, and the ability to use the block partitioning arrangement of image memory with a high speed scanout implementation. Still further, a buffer memory permits the image memory to be accessed at a rate different from the display pixel rate and permits the image memory to be accessed at a non-constant rate and an asynchronous rate relative to the display monitor refresh rate; such as for equalizing different rate pixel output periods from the image memory caused by a fast scanout rate and a slower block transition rate.

The memory architecture discussed herein has many advantages. For example, a memory configuration is provided for high resolution pixel rates to a display monitor using slow RAMs for image memory. Also, a configuration is provided for generating a kernel of 9-pixels to be available in parallel for image processing using an image memory that is accessed at a lower rate. Also, a configuration is provided for buffering of accessed information that is to be used a plurality of times as an alter-

nate to multiple accesses for information that is to be used a plurality of times.

A first-in first-out (FIFO) memory can be used as a buffer memory. This permits substantially simultaneous loading and unloading of the buffer memory and permits time sharing of a single buffer memory between loading and unloading operations. Contention between loading and unloading operations can reduce effective speed. For example, with unloading requirements determined by the display monitor pixel rate and with image quality effected by changes in the output pixel period, the memory speed can be kept relatively high and the output pixel period can be kept constant. This can be accomplished by resolving contention in favor of the output accessing of the FIFO, effectively reducing the input rate due to contention. A multiple buffer arrangement, such as a double buffer arrangement, can be used for a buffer memory. A multiple buffer is configured with redundant memory circuits, where one buffer is being loaded while another buffer is being unloaded, consequently reducing contention therebetween. Therefore, loading and unloading of the buffer memory can proceed at the write and read rates, respectively, for the memory circuits without reducing the rates as a result of contention. An advantage over a FIFO can be obtained with a multiple buffer because a FIFO involves both read and write operations in the same memory at substantially the same time while a multiple buffer arrangement permits either read operations for outputting from the buffer without write operations or permits write operations for inputting to a buffer without read operations; thereby permitting slower RAM circuits and greater pixel rates.

A double buffer memory can be implemented with the required buffer being replicated with double the amount of RAM circuitry. For example, a 1-line buffer configuration would be implemented with a double 1-line buffer for storing of an image in a first line-buffer while accessing a 1-line image from a second line-buffer. Similarly, a 3-line buffer configuration would be implemented with a double 3-line buffer for storing of a 3-line image in a first 3-line buffer while accessing a 3-line image from a second 3-line buffer. An alternate configuration provides a multiple buffer, such as a double buffer, without the need to double all of the buffer memory capability. For example, a system having a 3-line buffer for convenient generation of a 9-pixel kernel can be implemented with a 3-line buffer for the output buffer and a 1-line buffer for the input buffer and having precession or commutation of line buffers between input and output operations. This can reduce memory requirements, such as reducing requirements from a 6-line full double buffer to a 4-line improved buffer; yielding a reduction in memory circuit requirements by one-third.

Memory architecture pertaining to a buffer memory provides further speed enhancement in addition to the scanout and readdressing features discussed above. For example, in a display application image memory can be accessed during the full line period, blanked and unblanked portions, and pixels can be output to the monitor during the unblanked portion and not during the blanked portion. This provides a meaningful speed advantage, such as a 16%-speed advantage for a configuration having 53-microseconds per line unblanked period and 63-microseconds per line blanked plus unblanked periods. This buffer memory feature is relatively independent of the type of memory chips available and rela-

tively independent of the scanout and re-addressing arrangement.

Memory architectural features of sequentially accessing a scanline of pixels and buffering the scanline of pixels for multiple operations at different times for each pixel, such as kernel processing, provide a memory bandwidth enhancement. These features utilize several characteristics of the experimental configuration. Pixels can be accessed from image memory in an ordered form, such as in a scanline form consistent with the ordered form of pixels in a raster scan CRT monitor. The number of pixels to be buffered may be a relatively small percentage of the total image memory capacity, such as 3-scanlines out of 512-scanlines, about 1/2% of the image memory capacity.

The memory configuration in the experimental display system has significant advantages over other memory architectures. For example, it provides more than a 10-MHz rate for a kernel of 9-pixels, which is equivalent to a pixel access rate of more than 90-MHz (10-MHz kernels times 9-pixels/kernel). It performs this function using 200-ns RAM chips, implying only a 5-MHz pixel rate (1/200-ns = 5-MHz). Therefore, it provides about an 18-times advantage in memory access rate (90-MHz/5-MHz = 18-times). Alternately, accessing each of the kernel pixels at the implied 5-MHz access rate provides a kernel access rate of 0.55-MHz (5-MHz/9-pixels) instead of the 10-MHz kernel rate in the above example. Such an 0.55-MHz rate may be further degraded because the 200-ns access time of the RAM may be degraded by additional propagation delays, such as address input and data output logical propagation delays.

Consequently, an advantage of about 20-times in memory bandwidth can be obtained.

Speed advantages can be obtained by accessing information from memory at a higher duty cycle, and lower clock rate and outputting information at a lower duty cycle and higher clock rate by buffering accessed information with a buffer memory. For example, in a display system; pixels can be accessed from image memory at a slower clock rate during the full line period, blanked and unblanked line period portions, and pixels can be output to the display interface at a higher clock rate during the unblanked portion of the line and not during the blanked portion of the line.

Important speed and memory access advantages can be obtained by buffering of information that will be used a plurality of times, such as by buffering pixel information that will be used 9-times for a 9-kernel pixel. In this configuration, each pixel can be used to generate 9-output pixels, where a pixel will be used at each of 9-kernel positions for generating 9-adjacent pixels. Therefore, buffering the output pixels can reduce memory access bandwidth by a factor related to the number of times the pixel is used, 9-times in this example.

A system requiring a 13-MHz pixel rate during the unblanked period of a line and requiring accessing of 9-pixels from image memory for each output pixel implies a memory access rate of 117-MHz (13-MHz times 9-input pixels for each output pixel). However, accessing of memory during the full line period (both blanked and unblanked portions) can provide an improvement of 1.24-times by accessing of pixels at about a 10.5-MHz rate during the full line period, blanked and unblanked portions, (13-MHz times 53-microseconds unblanked

period divided by 67-microsecond for the blanked and unblanked period). Further, the buffer memory arrangement discussed herein overcomes the need to access 9-pixels from image memory to generate a single output pixel with a novel buffer memory configuration. Consequently, the buffer memory arrangement discussed herein can provide an improvement over 11-times (1.24 times 9) over a non-optimized arrangement.

FIFO Buffer Memory Architecture

The arrangement discussed above for generating a sequential line of pixels can be adapted to provide a triple line of pixels for spatial processing. A single line of pixels can be converted to a triple line of pixels with a look-ahead buffering arrangement. For example, if the memory map scanout is performed a line ahead of the display refresh and if 3-scanlines of scanned-out pixels are buffered, then the 9-pixels for a particular kernel, which is centered about the present pixel being displayed, is available in the 3-scanline buffer. The 3-scanline buffer can be implemented in various arrangements, such as with a double buffer arrangement and with a FIFO arrangement. A FIFO arrangement will now be discussed with reference to Fig 5D.

The arrangement shown in Fig 5D comprises 3-scanline buffers 513H implemented as FIFOs and an output register array 513A implemented to provide a 9-pixel kernel in parallel for spatial processing. The FIFOs are shown connected in serial form so that the next line of pixels being accessed are shifted into the lower FIFO channel 513E the present line of pixels, which is being shifted out of the lower FIFO channel 513E, is recirculated and shifted into the middle FIFO channel 513D; and the present line of pixels, which is

being shifted out of the middle FIFO channel 513D, is recirculated and shifted into the upper FIFO channel 2610C. Consequently, the lower FIFO channel 513E contains the next line of pixels, the middle FIFO channel 513D contains the present line of pixels, and the upper FIFO channel 513C contains the prior line of pixels. The parallel shifting of all three FIFO channels 513H makes available the next line, present line, and prior line of pixels; which can be shifted into the parallel register array 513A for spatial processing with processor 513B.

FIFOs can be implemented with RAMs, where the next address to be loaded is generated with a write address counter 513I and the next address to be accessed is generated with a read address counter 513F. As pixels are shifted into the FIFO, the write address counter 513I is incremented to the next available FIFO address. As pixels are shifted out of the FIFO, the read address counter 513F is incremented to the next FIFO address to access the next pixel in sequence. The read address counter can be incremented at a rate consistent with the display refresh requirements, which can be a constant rate along a scanline and a zero rate during line retrace and frame retrace. The write address counter can be incremented at a rate consistent with the scanout of pixels from the image memory, which can be a constant rate within a block and a lower rate between blocks. Therefore, the FIFO permits interfacing of two circuits operating asynchronously relative to each other. Comparator 513G can be implemented to compare the read address and the write address from read address counter 513F and from write address counter 513I, respectively. In normal operation, the write address is ahead of the read address. However, if the FIFO gets overloaded, the read address counter can be advanced up to

and past the write address counter; thereby overwriting important data. Comparator 513G detects such an overwrite condition and generates an error signal 513J, such to alert the operator or to override input operations.

The line buffer can be initialized by initiating image memory scanout prior to the first line to be displayed in order to load the 3-lines into the line buffer. This can be achieved with a look-ahead executed during the end of the previous frame, such as during the frame retrace period. Also, the system can be configured so that the average scanout rate from image memory is greater than the refresh rate of the display. Therefore, the line buffer will have sufficient pixels for refreshing the display. If the line buffer becomes fully loaded, detected by the read address approaching the write address; a disable signal can be generated to disable scanout from image memory until the display refresh has vacated capacity in the line buffer.

The parallel registers 513A can be implemented in a 3-pixel by 3-pixel array so that each row of three registers receives 3-pixel words from the corresponding line buffer channel. For example, the top row of registers 0, 1, and 2 receives prior pixel words from the top line buffer channel; the middle row of registers 7, 8, and 3 receives present pixel words from the middle line buffer channel; and the bottom row of registers 6, 5, and 4 receives next pixel words from the bottom line buffer channel. Implementation of the parallel registers to transfer in the row direction toward the right permits pixel words to be shifted into the register rows from the line buffer and to be shifted along the register row toward the right as the scanline progresses. Therefore, only a single pixel need be shifted out of each line buffer

channel for a particular pixel period; where the three rows of pixels are shifted toward the right to cause the kernel to shift toward the right along the scanlines.

The intensities for the 9-pixels stored in registers 513A can be output to the weighting multipliers and adders 513E for sum of the product processing for spatial filtering.

Kernel Memory Operations

Image processing may involve processing of a plurality of pixel intensities to generate a single pixel intensity for display. For example, an output pixel to a display monitor may be a convolved sum of the weighted intensities of a kernel of pixels. A kernel of pixels may be a 3-pixel by 3-pixel kernel, a 5-pixel by 5-pixel kernel, or other kernels. The need to process multiple pixels to generate each output pixel implies that image memory must be accessed a plurality of times for a plurality of pixels that are to be convolved for each output pixel. For example, in a configuration that processes a 9-pixel kernel to generate an output pixel, image memory would be accessed 9-times for a 9-pixel kernel for each output pixel period. This imposes a memory bandwidth requirement of 9-times the output pixel rate for the image memory access rate. Therefore, a system using such a configuration would require very high speed image memories or alternately would have relatively low resolution; either spatial resolution, or temporal resolution, or both; or alternately would have a combination of high image memory speed requirements and low output resolution. For example, a system having a 10-MHz output pixel requirement and a 9-pixel kernel spatial filtering output processing requirement would appear to need a 90-MHz memory pixel access rate. However, 90-MHz

RAM chips may have poor availability and may be relatively expensive compared to slower speed RAM chips.

An arrangement is provided herein using a buffer memory to store pixels accessed from image memory at the output pixel rate and providing a kernel of 9-pixels to the output filter. This configuration permits accessing of a 9-pixel kernel at more than a 10-MHz rate, yielding an equivalent pixel rate of more than 90-MHz (9-pixel kernel times 10-MHz). However, this configuration uses RAM chips having a 200-ns access time, implying an equivalent pixel access rate of about 5-MHz. This yields an improvement of about 18-times (90-MHz/5-MHz) in memory access bandwidth and permits use of less expensive lower speed RAMs to obtain relatively high resolution and to support multiple pixel kernel spatial filtering.

Blanked and Unblanked Memory Operations

A video signal can be generated with a plurality of line synchronization signals having a blanked portion for horizontal retrace and having an unblanked portion for displaying a line of the image. For example, the line rate may be about 15,750-Hz; yielding about a 63-microsecond line period. Approximately 10-microseconds of this line period may be blanked, yielding about a 53-microsecond unblanked line period. In a system having a direct output from the image memory to the display monitor, the image memory may be accessed during the unblanked period and the image memory may not be accessed during the blanked period. However, important advantages can be obtained by accessing image memory during the full line period, during both blanked and unblanked portions of the line period. This can be implemented with a buffer memory that stores pixels

during the blanked and unblanked portions of the line period and accesses pixels for display during the unblanked portion of the line period.

The number of pixels that are input to the line buffer from image memory may be the same as the number of pixels that are output from the line-buffer to the display monitor. The output period can be implemented to be the unblanked portion of the line period and the input period can be implemented to be the blanked plus unblanked portions of the line period. Therefore, because the output period is shorter than the input period; the output rate can be greater than the input rate. Consequently, the image memory generating the input rate can be slower than the output pixel rate and, hence, the output pixel rate can be greater than indicated by image memory speed. For example, in a system having a 63-microsecond line period and a 53-microsecond unblanked portion of the line period, a 10-MHz buffer input rate can be buffered to provide about a 12-MHz output rate because of the greater input period for loading the buffer; i.e., 63-microseconds; compared to the output period for unloading the buffer; i.e., 53-microseconds. This permits relatively slower speed RAMs to be used for image memory, which may be a larger memory (i.e.; a 265,000 pixel image memory) in conjunction with a higher speed buffer memory, which may be a smaller memory (i.e.; a 512-pixel line buffer memory); thereby efficiently providing high pixel rates with relatively slow speed image memory RAMs.

4/3rds Buffer Memory Architecture

The buffer memory features discussed herein are illustrated with a novel buffer memory, herein called a 4/3rds buffer memory, that provides double buffer mem-

ory capabilities. A double buffer memory duplicates the buffer memory requirements so that a first buffer memory can be in the process of being loaded while a second buffer memory is in the process of being unloaded. The 4/3rds buffer memory is more efficient than a full buffer memory because it replicates only 1/3rd of the redundant buffer memory; where 3-lines are being simultaneously unloaded while a 4th-line is being loaded. This 3-line multiple buffer, implemented as a 4/3rds line buffer, is illustrative of other multiple buffer type configurations that are optimized to reduce the amount of memory from double to less than double. For example, the improved multiple buffer memory can be implemented in the form of a 3/2's buffer, a 5/3rds buffer, and other optimized multiple buffer configurations.

The optimized multiple buffer is exemplified with a precession technique. For example, a fractional portion of the buffer is replicated for loading while a full buffer is being unloaded. Then, the newly loaded portion of the buffer is precessed into the output buffer, the output buffer is precessed within the output buffer, and part of the output buffer is precessed to the input buffer. For example, in the 4/3rds buffer arrangement discussed herein; line buffers, line buffer-1 to line buffer-4, are shared between input and output buffers; where the input line buffer uses a 1-line buffer and the other line buffer uses a 3-line buffer. Line buffers, line buffer-1 to line buffer-4, may be precessed in sequence; where each line-buffer is sequentially switched to the input line buffer, output line-buffer channel-1, output line-buffer channel-2, output line-buffer channel-3, and then back to input line-buffer in sequence. When line buffer-1 is in the input line buffer position, line buffer-2 is in the channel-1 position, line buffer-3 is in the channel-2 posi-

tion, and line buffer-4 is in the channel-3 position. During the next line operation, line buffer-1 is switched to the channel-1 position, line buffer-2 is switched to the channel-2 position, line buffer-3 is switched channel-3 position, and line buffer-4 is switched to the input buffer position. The 4-line buffers precess in sequence through the input buffer; output buffer channel-1, output buffer channel-2, and output buffer channel-3, and input buffer positions. Consequently, a new line of information is being loaded into the line-buffer in the input buffer position, the most recent line of information is being output in the output buffer channel-1 position, the next most recent line of information is being output in the output buffer channel-2 position, and the oldest line of information is being output in the output buffer channel-3 position. Hence, output buffer channel-1 provides kernel pixels 1, 2, and 3; output buffer channel-2 provides kernel pixels 8, 9, and 4; and output buffer channel-3 provides kernel pixels 7, 6, and 9. For the next line condition, each line is shifted end around; where the most recent line of information loaded in the line-buffer in the input position is switched to the output buffer channel-1 position, the line-buffer in the output buffer channel-1 position is switched to the output buffer channel-2 position, the line-buffer in the output buffer channel-2 position is switched to the output buffer channel-3 position, and the line-buffer in the output buffer channel-3 position (which is the oldest information and is no longer needed) is switched to the input buffer position for loading of a new line of information. This end-around shifting of lines of information causes a precession of the 4-line buffers to the 4-buffer positions to provide for inputting of a new line of information and for simultaneously outputting each of the last 3-lines of information

for-implementing a parallel 3-line 9-pixel kernel for spatial filtering.

Other Buffer Configurations

Various configurations of the buffer of the present invention have been discussed above to illustrate how the various features and devices of the buffer of the present invention can be used to implement a system. These configurations are illustrative of a large number of other configurations that can be implemented from the teachings herein.

The buffer of the present invention has been described in combination with other novel features of the present invention, such as a novel memory architecture. However, the buffer of the present invention can be used with other systems having other configurations, where the buffer of the present invention is not constrained to use only with the other elements of the system of the present invention.

The buffer of the present invention has been described for implementation with Integrated circuit RAMs. Alternately, the buffer teachings of the present invention can be implemented with other memories; such as CCD memories, core memories, and other types of memories. Also, many of the teachings associated with the buffer memory of the present invention can be utilized with ROMs.

The weight memory of the present invention is described herein for implementation with integrated circuit RAMs. Alternately, the weight memory teachings of the present invention can be implemented with other memories; such as CCD memories, core memories, ROMs, PROMs, EROMs, and other types of memories.

For example, the weight memory can be implemented as a weight ROM in place of the weight RAM.

The buffer of the present invention has been discussed in the form of a 4/3-buffer as an improvement on a double buffer. Other non-integer or fractional multiple buffers can be implemented, such as a 5/3-buffer instead of a 4/3-buffer, for replacing other integer multiple buffers, such as a triple buffer instead of a double buffer.

The buffer of the present invention has been discussed in conjunction with a 9-pixel kernel spatial filter. However, the buffer of the present invention can be implemented with other post processor arrangements with a kernel processor and can be implemented with other kernel processors, such as a 25-pixel kernel or a 48-pixel kernel processor.

EXPERIMENTAL SYSTEM

EXPERIMENTAL SYSTEM ARCHITECTURE

General Description

An experimental system is configured with a host computer, a display processor, memory, and a color monitor. The host computer is implemented with an S100 bus configuration using S100 compatible boards, such as Compupro boards; together with disk drives, printers, and other peripherals. The CRT monitor is a conventional color monitor having an analog RGB input, shown with monitor documentation included herewith. The display processor and memory arrangement is configured with a plurality of wire wrap boards. These boards include a logic board, BL1; 2-memory boards, BM1 and BM2; a rear-end board, BR1; and a buffer board, BB1.

Operation of hardware and software in the experimental system discussed herein in conjunction with a color monitor demonstrates operation of the system, meeting of system objectives, and providing actual reduction to practice. For example, information has been loaded into image memory and has been display processed and displayed to demonstrate operation.

Supervisory Processor Interface

The interface between the supervisory processor and the display processor comprises input synchronization signals from the display processor to the supervisory processor to synchronize the supervisory processor with the display processor operations and output commands from the supervisory computer to initialize the display processor.

Synchronization signals include a frame synchronization signal and a line synchronization signal. The frame synchronization signal occurs during vertical retrace and vertical blanking of the video signal. The line synchronization signal occurs during horizontal retrace and horizontal blanking of the video signal. An interlaced scan arrangement is used for the experimental system, although other scan arrangements can readily be accommodated. A field identification signal is provided that identifies whether the field is a first field or a second field of the interlaced scan.

Communication between the supervisory processor and the display processor is performed with a 3-port parallel interface to a Compupro Interfacer-II board under program control. Each port has 8-parallel input lines and 8-parallel output lines. The port assignments are listed in the COMPUTER PORT TABLE included herein. Output signals are defined as DO signals and

input signals are defined as DI signals. Port identification; A, B, or C; follows the DO or DI symbol. Signal line identification follows the port identification; i.e , DOA7 identifies output line-7 in port-A.

Signal DOA5 controls loading in sequential and random access form. Sequential loading is selected when DOA5 is high and random access loading is selected when DOA5 is low. When DOA5 is high, an output strobe on DOA7 causes the pixel address registers to be updated with the related slope parameters on the falling edge of the strobe. This insures compatibility with the DOA7 strobe used as a write-bar signal to write the previous pixel information into the previously addressed pixel in image memory.

Signal DOA6 controls loading and running operations. Running is selected when DOA6 is high and loading is selected when DOA6 is low. In general, DOA6 is high during displaying of images and DOA6 is low during loading of images into memory.

Signal DOA7 strobes the information output with Port-B and Port-C into the destinations. DOA7 is normally low, where DOA7 is pulsed high and then pulsed low under program control to form an output strobe.

Signal DIA0 inputs the frame sync pulse from the CRT monitor interface. This frame sync pulse is the blanking pulse that blanks the CRT monitor during the vertical retrace period and during a predetermined number of lines prior to and subsequent to the vertical retrace period. This frame sync pulse occurs once per field, twice per frame, in the interlaced scan system as implemented with the demonstration system. The rising edge of the frame sync pulse, detected under program control, initiates loading of the parameters for a new

field from the supervisory processor into the display processor.

Signal DIA2 inputs the line sync signal from the CRT monitor interface, which is implemented for hardware control but not software control in the experimental system.

Signal DIA4 inputs the frame identification signal from the CRT monitor interface. DIA4 is high during the field-1 period and low during the field-2 period.

Signals DOB0 through DOB7 output the information to be loaded into the destination identified with Port-C. This information can be delta information to be loaded into the delta registers, pixel address information to be loaded into the pixel address registers, and pixel data to be loaded into image memory.

Signals DOC0 through DOC7 output the address of the destination to be loaded with the Port-B output signals. The various destinations are listed in the TABLE OF DESTINATION SELECT ASSIGNMENTS included herein; including the 4-delta registers each having an MSH and an LSH, 2-address registers each having an MSH and an LSH, data to be written into image memory, and weights to be written into a weight table memory.

Image Loading

Loading of an image into memory is performed by loading the XP and YP-address registers with the address of each pixel to be loaded, then outputting the pixel information to be loaded with Port-B, and then strobing the pixel information into image memory with the DOA7 signal. A sequential load feature is provided under control of the DOA5 signal. When the DOA5 sig-

nal is high, a vector can be loaded; where the previously loaded pixel address is incremented with the related delta parameter to obtain the next pixel address to reduce software overhead and thereby speedup loading of image memory.

Loading of image memory with the supervisory processor is performed with a 3-port output arrangement having 8-bits per port. The first port, Port-A, communicates control signals between the supervisory processor and the display processor. The second port, Port-B, communicates address and data information to be loaded into the display processor between the supervisory processor and the display processor. The third port, Port-C, selects the register or memory in the display processor for loading. The protocol involves outputting of the destination address on Port-C, outputting of information to be loaded into the display processor on Port-B, and then outputting of a data strobe on Port-A. The data strobe loads the output information into the selected destination.

A program to load vectors into memory is provided herein as the BASIC PROGRAM LISTING LD.ASC and is briefly discussed in the section entitled Software herein.

Software

Programs have been developed to operate the experimental system and are included herein in the tables. BASIC PROGRAM LISTINGS. These programs are source programs, that are compiled with a Basic compiler and linked with a Basic linker to obtain compiled Basic programs. Compiled Basic programs run significantly faster that interpretive Basic programs, which maintains real time synchronization between the display

processor and the supervisory processor. The source listings may be readily compiled and linked by one skilled in the art to provide the compiled Basic programs executed to perform the image loading and image processing operations. The programs are programmed to be menu driven, prompting the operator to select various operator-selectable options.

The Basic listings included herein have extensive annotation to teach one skilled in the art the features implemented therein.

The BASIC PROGRAM LISTING LD.ASC provided herein teaches loading of vectors into memory. The BASIC PROGRAM LISTING GRAPH.ASC provided herein teaches refreshing of a CRT monitor from memory. These listings are clearly coded and amply annotated to teach one skilled in the are [*sic*] how to operate the experimental system disclosed herein under program control.

Circuit Boards

The experimental system is implemented with wire wrap circuit boards consisting of 2-Memory Boards (BM1 and BM2), 1-Logic Board (BL1), 1-Buffer Board (BB1), and 1-Rear End Board (BR1). Each board is constructed with a Vector board, manufactured by Vector Electronic Company of Sylmar CA, having 1/10th inch hole spacings on a 17-inch by 8 1/2-inch board. Wire wrap DIP sockets cable connectors are inserted into the Vector board and interconnected with wire wrap interconnections. Information on the DIPs plugged-in to the DIP sockets is provided for selected boards in the printout of the TABLE OF DIP LAYOUT ON BOARDS included herewith. Information on the cable connectors is

provided for each cable in the printout of the CABLE CONNECTION TABLE included herewith.

DIP assignments are provided for selected boards in the TABLE OF DIP LAYOUT ON BOARDS included herewith, for each board. DIPs are arranged on the boards as rows identified with alphabetical symbols; i.e., A to E; and as columns identified with numerical symbols; i.e., 1 to 23. Each DIP position on a board is identified with a U symbol followed by the column and row symbols (i.e., U3A).

Logical schematic diagrams showing implementation of the experimental system are provided herewith, such as shown in Fig 6. These logical diagrams show standard commercially available integrated circuits; such as TTL series 7400 ICs, Mitsubishi M58725 RAMs, and 8216 bi-directional bus drivers, and Sygnetics 8T97 buffers. Specifications for these integrated circuits are available in catalogs and specification sheets from the abovementioned manufacturers and are well known in the art.

The schematic diagrams show the logical function in symbolic form, identify the type of IC, identify the DIP numbers and pin numbers, and show wiring interconnections between DIP and pin numbers. Device types are often shortened, such as shortening the name 74LS02 to LS02. DIP assignments are identified with U numbers, such as U20C representing the DIP at row-20 column-C on the subject circuit board. For example, a NOR-gate is shown at the top portion of Fig 68 identified with the designation LS02 as being a 74LS02 quad NOR-gate integrated circuit, identified with the designation U21C as being located on the BL1 circuit board at row-C column-21, and having 2-input signals on pin-11 and pin-

12 of the DIP and one output signal on pin-13 of the DIP. The input to pin-11 is shown connected to the output of DIP U228 Pin-3, the input to pin-12 is shown connected to the output of DIP 0208 pin-12, and the output from pin-13 is shown connected to DIP U7D pin-9. For convenience of documentation, interconnections may be designated by the DIP identification number and pin number separated by a dash; i.e., U21C-13 representing pin-13 of DIP U21C. For convenience of discussion, logical circuits may be designated by the DIP identification number and the output pin number separated by a dash; i.e., U21C-13 representing pin-13 of DIP U21C.

Cable List

A cable list is provided in the CABLE CONNECTION TABLE included herewith. This cable list identifies the cables between the various Vector boards and between the Vector boards and the supervisory processor. Each cable between display processor boards is implemented with a 50-pin ribbon cable having odd pins connected to ground for signal isolation. Each cable between the Vector boards and the supervisory processor is implemented with an RS-232 type 25-pin ribbon cable, consistent with the signal representations for the CompuPro Interfacer-II board. The cable list identifies the pin associated with a signal, a symbol associated with the signal, a description of the signal, a representative source of the signal and a representative destination of the signal.

S-100 Bus System

The experimental system has been implemented with an S-100 bus based system performing supervisory processor functions in conjunction with the novel software and hardware, as discussed herein. Two S-100 bus

based systems have been configured, the Camille system and the Murphy system. The configuration of the Camille system will be discussed in detail hereinafter The Camille system comprises a computer, a pair of floppy disk drives, a terminal, and printers as discussed below.

The floppy disk drives are implemented with a pair of 8-inch disk drives in an enclosure and operating in conjunction with a DMA controller in the computer. The disk drives are manufactured by Siemens as the FDD 100-B; the drive enclosure is manufactured by International Instrumentation, Incorporated; and the DMA Controller is manufactured by Compupro as the Disk 1 DMA Controller; all described in detail in the referenced manuals.

The terminal is manufactured by Applied Digital Data Systems, Inc. (ADDS) as the Model Viewpoint/3A Plus; described in detail in the referenced manual.

The printers include a dot matrix printer manufactured by Star Micronics, Inc. as the Gemini-10, a dot matrix printer manufactured by Epson as the FX-100, and a daisywheel printer manufactured by Smith-Corona as the TP-I; all described in detail in the referenced manuals.

The computer is implemented with a cabinet manufactured by Fulcrum Computer Products as the 18080 Microcomputer System Cabinet and having a backplane S-100 board manufactured by CPA which is described in detail in the referenced CPA manual.

The computer is implemented with various S-100 boards manufactured by CompuPro including the 0085-8080 CPU board, RAM 16 and RAM 17 memory boards,

a System Support board, and a pair of Interfacer 2 boards. One Interfacer 2 board is used to interface to the terminal and printers. The other Interfacer 2 board provides the 3-channel parallel interface to the control logic. These boards are described in detail in the referenced manuals.

The joysticks are implemented with the Computer Compatible Joystick; described in the referenced applications notes.

The operating system is CP/M 80, which is described in detail in the referenced documents.

The applications program runs under Basic, which is described in detail in the referenced documents.

The following documents provide supplemental data on the computer system and are herein incorporated by reference.

1. Technical Manual, Siemens, OEM Floppy Disk Drive FDD 100-8, Technical Manual, Model 100-80,

2. Manual, International Instrumentation, Incorporated, Universal Disk Enclosures, General Information/Pricing, 1982.

3. User Manual, CompuPro Division of Godbout Electronics, Disk 1 Arbitrated 24 Bit DMA Floppy Disk Controller, 1981.

4. User's Manual, Applied Digital Data Systems, Inc., Viewpoint/3A Plus, 518-31100.

5. Operation Manual, Star Micronics, Inc., Gemini-10 printer.

6. Operation Manual, Epson, FX Printer, 1983.

7. Operator's Manual, Smith-Corona, TP-I.

8. Functional Description, CP-A, Revision 1.

9. Technical Manual, CompuPro Division of Godbout Electronics, 8085/8088 CPU Dual CPU, 2/83.

10. Technical Manual, CompuPro Division of Godbout Electronics, RAM 16 Static Memory, 4/82.

11. Technical Manual, CompuPro Division of Godbout Electronics, RAM 17 64K Static Memory, 9/82.

12. User's Manual, CompuPro Division of Godbout Electronics, System Support 1, 8/81.

13. Technical Manual, CompuPro Division of Godbout Electronics, Interfacer 2, 4/82.

14. The CP/M Handbook with MP/M, by Rodnay Zaks, published by Sybex, 1980.

15. CP/M Primer, by Stephen Murtha and Mitchell Waite, published by Howard W. Sams & Co., Inc., 1980.

16. An Introduction to CP/M Features and Facilities, published by Digital Research, January 1978.

17. Microsoft Basic Reference Book, published by Microsoft, 1979.

18. Microsoft Basic Compiler Documentation, published by Microsoft.

19. The Basic Handbook (2nd Edition), by David Lien, published by Compusoft Publishing, 1981.

20. Microsoft Basic (2nd Edition), by Ken Knecht, published by Dilithium Press, 1983.

21. Basic Basic (2nd Edition), by James Coan, published by Hayden Book Company, Inc., 1978.

22. Computer Compatible Joystick Instruction, applicable to: Apple-II.

LOGIC BOARD

Control Logic

Various control arrangements can be provided for controlling operation. For example; counter, ROM, and logical control arrangements of synchronous or asynchronous design can be used. A gated clock arrangement has been implemented for control, which is illustrative of other forms of gated clock control logic and other non-gated clock control logic implementations. This gated clock control arrangement will now be discussed with references to Figs 6B to 6D.

The gated clock control logic shown in Figs 6B to 6D controls the clock pulses to various logic devices; such as address generators, memories, and other devices; to clock the various operations associated therewith. For example, the write strobe W-bar to the memories is generated with U22C-11 and clocks to various registers are gated with circuits U21C, U20C, U19C, 19D, U18C, U9A, and U10A (Fig 6B). Several different types of clocks are generated at different times and are controlled to be non-conflicting with other clocks. Load clocks are generated under computer control to load computer generated parameters into various registers. Address generator clocks can be generated under control of external sync pulses. High speed clocks can be generated under control of various signals to generate addresses that are not in contention with other signals generating clocks and are not generated at times that such addresses are not needed.

The logic composed of U18D-6, U22B-3, U21E-6, U19B, U20B, and U21D-6 (Fig 6B) is controlled by the computer for generating strobe signals and control signals for loading computer information into the address

generators and for disabling operations during loading of computer information. Logic gates U20C and U21C (Fig 6B) gate the computer strobe to load delta registers. Logic gates U19C, U19D, and U18C (Fig 6B) gate various clock signals to load and update R-registers. Logic gates U9A and U10A (Fig 6B) gate various clock signals to load and update P-registers. Flip-flops U22E and associated logic U20D-4, U22A-4, U18D-8, U21E-4, U15A-3, U22C-3, U20D-13, U18D-2, U21E-10, U18E-6, U20D-1, U21E-12, U19D-4, U18E-3, U21D-8, U20E-6, U17A-8, U17A-11, U22A-2, U13A-8, U21E-2, U20E-3, and other related elements (Fig 6D) synchronize and process the sync signals CFS and CLS to generate clock and control signals for processor operation. Logic gates and flip-flops U12A, U21D-8, U18E-3, U14A-2, U14A-4, U16A-3, U17A-3, U16A-6, U17A-6, U13A-6, U23C-10, U14A-6, U20E-11, U21B-5, U15A-11, U21B-2, U21E-8, and related gates (Fig 6C) control the gated clock pulses for address generation operations.

The computer interface signals are defined in the tables of computer interface signals; PORT-A, PORT-B, AND PORT-C. Port-A input and output signals are control signals. Port-B output signals are address and data signals to load into the selected destination. Port-C output signals are destination select signals.

Computer load logic will now be discussed with reference to Fig 6B. Computer control signals DOA6 and DOA7 control loading of initial conditions. When DOA6 is 1-set, run operation is commanded and loading of initial conditions from the computer with the load strobe DOA7 is disabled with gate U22B-3. When DOA6 is 0-set, run operation is disabled and load operation is enabled through inverter U18D-6 by enabling gate U22B-3

to pass an inverted computer strobe D0A7 as signal U22B-3. This gated strobe is used to clock the selected register, steered with the register address decoders U19B and U20E to gates U21C, U20C, U19C, and U19D. The inverted DOA6 signal U18D-6 is inverted with U21E-6 to generate the DIEN-bar signal for memory read and write operations. When DOA6 is high, defining the run mode; DIEN-bar is high establishing the memory read mode. When DOA6 is low, defining the load mode; DIEN-bar is low establishing the memory write mode. DIEN-bar control operations are discussed in detail with reference to Figs 6E to 6N for the memory logic.

Write signals U22C-6 and U22C-8 control writing into a peripheral RAM by enabling write pulses W2 and W3 when addressed through U19B-10 and U19B-9 respectively.

Gate U22C-11 is an OR-gate that is enabled with the address of the memory U19B-11 to load data into the memory for steering of the computer strobe U22B-3 to generate a write strobe to load the computer generated parameter into memory.

Gates U20C and U21C are NOR-gates that are enabled with the destination register address signals from U19B and U20b to select the delta register to be loaded by steering of the computer strobe U22B-3 to clock the appropriate delta register to load the computer generated parameter into the selected register.

A master clock, shown as CPE-bar (Fig 6D), is fanned-out, gated, and applied to the synchronous elements. The CPE-bar clock is derived from a clock pulse generator and communicated to the logic board on cable C4-6. Alternately, clock CPE-bar can be generated with

a self-contained clock generating operating asynchronously with reference to the external clock to permit optimization of clock periods for system operation. For example, the external clock may be constrained to a clock frequency consistent with the requirements of a sync generator for the CRT monitor, which may not be an optimum clock frequency for the address generators. Therefore, a separate clock can be provided having a clock frequency that is optimum for the address generators in place of the external clock.

Clock logic will now be discussed with reference to Fig 6D. The clock CPE-bar is logically processed to clock synchronous elements in the address generators at the same time. For convenience of definition, clocking occurs at the rising edge of the delayed clock pulse CPD, which is delayed by 2-gate propagation delays after the early clock CPE-bar and one inversion of the early clock CPE-bar. For example, CPE-bar propagates through inverter U21E-2 and non-inverting AND-gate U20E-3 to provide one inversion and 2-delays to generate delayed clock CPD prior to being used to synchronously clock register U22E. Similarly, clock CPS-bar is delayed by gating logic U12A-8 and U12A-6 (Fig 6C). providing one stage of delay and one stage of inversion, and by non-inverting gates U9A-6, U9A-8, U10A-6, and U10A-8 (Fig 6B) to provide the 2-propagation delays and the single inversion from the early clock CPE-bar to the clock signals for registers U8D, U9D, U5D, U8E, U5E, and U9E.

In one display configuration, register U22E is used to. synchronize operation of the logic with a frame sync, signal CFS and a line sync signal CLS. A short synchronous pulse is generated in conjunction with the line sync

signal CLS. CFS is synchronously clocked into flip-flop U22E-10 and CLS is synchronously clocked into flip-flop U22E-12 to latch these signals as CFSR1 and CLSR1 respectively synchronous with the address generator clock. Latched line sync signal CLSR1 is then latched in flip-flop U22E-15 one clock period later for a delayed line sync signal CLSR2. The delayed line sync signal CLSR2 U22E-5 is inverted with inverter U21E-10 and NANDed with the non-delayed line sync signal CLSR1 with NAND-gate U18E-6 to generate a short inverted pulse bracketing the first clock period of line sync signal CFSR1.

Clock signal CPE-bar (Fig 6D) is gated with NAND-gates U12A-8 and U12A-6 (Fig 6C) to generate a gated clock signal for address generation; which is performed with registers U8D, U9D, U5D, U8E, U9E, and U5E. Gating of the clocks to these registers with AND-gates U9A-6, U9A-8, U10A-6, and U10A-8 gates address generator operations.

Control logic for a display configuration will now be discussed with reference to Fig 6D. Signal U13A-8 is a clock gate control signal for gating the address generator clock, as described herein with reference to Fig 6C. This gate signal is comprised of three components; U17A-8, U17A-11, and U22A-4. These components cause the clock to be generated at the appropriate time in conjunction with the display sync signals. Gate U20D-4 ORs together the field sync and frame sync signals to enable the address generator clock through U22A-4 and U13A-8 when neither a frame sync signal CFSR1 nor a line sync signal CLSR1 is present. Gate U20E-6 ANDs together the inverted frame sync signal CFSR1 through inverter U18D-8 and the line sync sig-

nal. Gate U17A-8 NANDs together U20E-6 and the delayed line sync signal CLSR4 to enable the address generator clock through U13A8. Gate U17A-11 NANDs together U20E-6 and the undelayed inverted. line sync signal CLSR1 through inverter U22A-2 to enable the address generator clock through U13A-B.

The ELS signal U15A-3 controls multiplexers U10D, U11D, U12D, U10E, U11E, and U12E (Fig 6D). During the appropriate portions of the load mode, the address generator P-registers are loaded from the address generator R-registers under control of the ELS signal. During other periods of time, the address generator P-registers are updated from the related delta registers under control of the ELS signal. The ELS signal is. disabled by the sequential load control signal DOA5 inverted with U21E-4. This permits the P-registers to be updated from the delta registers to generate vectors into memory, such as for a display configuration. The ELS signal is strobed with a short pulse U19D-4 during the load mode DOA6 as controlled with U22C-3. During the load mode, the ELS signal is enabled with DOA6 enabling U22C-3 to pass the short pulse U22C-2. The short pulse is generated by the early line sync signal CLSR1 U22E-12 and the thrice delayed line sync signal CLSR4 U22E-7 for a 3-clock period transfer pulse to transfer information from the R-registers to the P-registers. The 3-period pulse U19D-4 is generated when CLSR4 U22E-7 is low and when CLSR1 U22E-10 is high, as inverted with U21E-12 to define the period that the undelayed line sync signal CLSR1 has gone high and before the delayed line sync signal CLSR4 has gone high; indicative of the first 3-clock periods at the start of a line sync pulse.

The XA3 and XA3-bar signals are shown gated with U19A-1 to disable both the XA3-bar signal and hence memory board-1 and the XA3 signal and hence memory board-2 with gates U19C-13 and U19C-4 respectively. This provides for blanking of the display and clearing of the buffer memory by outputting zeros from the disabled memory board when either the frame sync signal CFSR1 or the sequential load signal DOA5 are true. U19C-1 disables the memory boards during-sequential loading with DOA5 U19A-3 and during the vertical blanking period with the inverted CFSR1 signal from inverter U18D-8.

Registers U22E and U23C are used to latch signals. U23C-2 and U23C-5 latch signals C2-30 and C2-32 to provide latched signals C4-32 and C4-36 respectively. U23C-10 is used in the clock gating logic, as discussed with reference to Fig 6C. U22E10 and U22E-12 latch signals CFS and CLS respectively. U22E-15, U22E-2, and U22E-7 provide 1-clock delay, 2-clock delays, and 3-clock delays respectively for the CLSR1 signal.

Gated clock operations will now be discussed with reference to Fig 6C. Gated clock signals U12A-8 and U12A-6 each gate early clock CPE-bar with DOA6 from U21E-6 so that address generation will only be performed when the run/load-bar signal DOA6 is high, indicative of run operations. Gated clock signals U12A-8 and U12A-6 also gate early clock CPE-bar with U13A-8, which is composed of 3-gating conditions; U17A-8, U17A-11, and U22A-4; discussed in greater detail with reference to Fig 6D. Gated clock signal U12A-8 also gates early clock CPE with U14A-6, which enables high clock rate memory scanout operations within a block. Gated clock signal U12A-6 also gates early clock CPE-

bar with 13213-2, which enables low clock rate memory block re-addressing operations. Consequently, when memory-operations are proceeding within a block of 64-pixels, the address generator clock is generated as shorter period clock signal U12A-8 and, when memory operations are making a transition between blocks and need additional clock time for re-addressing, the address generator clock is generated, as longer period clock signal 1312A-6.

Determination of whether memory scanout or re-addressing is being performed for the particular clock period is determined by detecting an overflow of an address generator, as indicative of re-addressing, or detecting of a non-overflow of all address generators, as indicative of scanout. Overflow for this condition is defined as an overflow for a positive delta condition and an underflow for a negative delta condition. Therefore, detection of a carry condition for a positive delta or detection of a non-carry condition for a negative delta represents an overflow condition for gating a clock. An overflow condition on either the X-address generator or the Y-address generator causes a re-addressing condition.

As shown in Fig 6C, a re-addressing condition is detected with NAND-gate U13A-6 from any one or combination of the 4-conditions U16A-3, U17A-3, U16A-6, and U17A-6. U16A-3 compares the inverted overflow bit C1-bar U15E-9 of the Y-address generator with the non-inverted sign bit SN1 U14E-6 of the Y-delta register to detect a Y-negative overflow condition. U17A-3 compares the overflow bit C1 U15E-9 of the Y-address generator with the inverted sign bit SN1 U14E-6 of the Y-delta register to detect a Y-positive overflow condition.

U16A-6 compares the inverted overflow bit C2-bar U15D-9 of the X-address generator with the non-inverted sign bit SN2 U14D-6 of the X-delta register to detect an X-negative overflow condition. U17A-6 compares the overflow bit C2 U15D-9 of the X-address generator with the inverted sign bit SN2 U14D-6 of the X-delta register to detect a X-positive overflow condition. An overflow signal U13A-6 is latched and delayed with flip-flop D23C-10 for enabling of the scanout clock U12A-8 for scanout, in the absence of an overflow condition. Flip-flop U23C-10 provides a one-clock period delay so that an extended re-addressing clock period occurs in the clock period following the overflow condition, which is the clock period during which the re-addressing is performed. Latched overflow signal U23C-10 is inverted with inverter U14A to form a non-overflow signal U14A-6 and used to enable the scanout clock U12A-8.

Latched overflow signal U23C-10 is also processed with flip-flops U21B-5 and U21B-2 to provide a triple clock period for an overflow. These flip-flops are clocked with the non-gated delayed clock pulse CPD U20E-3 to control non-gated clock period time delays. If clocked with the gated clock pulse, such as with U15A-8; then the gating clock logic could cause the clock signal to lock-up.

A triple clock period for re-addressing will now be discussed with reference to Fig 6C. Detection of an overflow condition U23C-10 with gate U20E-11 sets flip-flop U21B-5 on the first clock period and sets flip-flop U21B-2 on the second clock period, which adds 2-clock periods to the basic single clock period; yielding a triple clock period to facilitate readdressing. At the completion of the third clock period, the 1-set signal U21B-2

enables a single clock signal U21B-6 and is inverted to a 0-set signal U21E-8 to reset U21B-5 through U20E-11 and to reset U21B-2 through U15A-11 on the next clock to clock flip-flops U21B-5 and U21B-2, respectively. This triple clock period logic is designed to operate for a single overflow condition surrounded by non-overflow conditions, or for two overflow conditions immediately following each other, and for many overflow conditions immediately following each other. For a single overflow condition; scanout clock U12A-8 has a series of single period clocks and has 3-clock periods missing that are coincident with overflow conditions and re-addressing clock U12A6 has a single clock coincident with the overflow condition. For multiple sequential overflow conditions; scanout clock U12A-8 has a series of single period clocks with a series of triple clock periods missing that are coincident with the multiple sequential overflow conditions and re-addressing clock 012A-6 has multiple sequential clocks each separated by 2-clock periods.

The scanout clock U12A-8 and the re-addressing clock U12A-6 are generated separately for gating purposes. They are ORed together with gate U21D-8 for loading the buffer memory with signal C3-22 and for clocking register U23C-9. This causes the pipeline from the memory output through the buffer memory to be clocked by an out-of-phase signal, yielding a 1.5 clock period proppgation delay time for the memory. The design is carefully configured so that the pipeline propagation delay is greater than the 0.5 clock periods and less than the 1.5 clock periods to facilitate proper clocking of the memory output signal into the buffer memory with a propagation delay that can approach the 1.5 clock period. The clock signals to the address generation registers are implemented as the logical-OR of a plurality of

different clock signals. In order to equalize clock delays so that each clock is twice delayed, including the once inverted CPE-bar signal with U12A-8 and U12A-6, the two address generator clocks U12A-8 and U12A-6 are separately ORed together with each of the address generator clock gates U5A-6, U9A-8, U10A-6, and U10A-8 (Fig 6B) rather than using the pre-Ored clock signal U21D-8 in order to reduce clock skew.

Clock gating logic will now be discussed in greater detail with reference to Fig 6B. Address decoders U20B and U19B decode the destination address DOC0 to DOC7 to generate a decoded address signal at the outputs of U19B and U20B to select the gated clock channel. This steers the computer load strobe U22B-3 to the addressed register to load that register. The address assignments are set forth in the table entitled DESTINATION SELECT ASSIGNMENTS. The most significant 16-address block is decoded using block decode logic U21D-6 to enable decoders U19B and U20B when the 4-MSBs DOC4, DOC5, DOC6, and DOC7 are all 1-set. The block enable signal U21D-6 enables U19B and U20B with the E1-bar inputs. The most significant address signal DOC3 enables U20B when low, indicated by the E2-bar input, and enables U19B when high, indicated by the E3 input. Consequently, U203 generates the LSH addresses and U19B generates the MSH addresses. One of the 8-addresses for the selected. half is selected with the 3-least significant address bits DOC0, DOC1, and DOC2 which go to each address decoder U19B and U2DB. The address decoder that has been selected with the DOC3 to DOC7 address signals has one of 8-address output lines low, as determined by the DOC0 to DOC2 least significant address bits. The low output line enables the register clock gating logic to

steer the clock to the addressed register. The clock is the negative going strobe U22B-3 generated under computer control. Effectively, the decoded address signals steer the computer strobe to the appropriate register clock input to clock the computer output data word into that register.

Control logic for a display configuration will now be discussed with reference to Fig 6D. Signal U20D-1 is a single pulse clock signal occurring at the leading edge of the line sync signal except when a frame sync pulse or a computer load signal is generated. This clock pulse is generated by U18E-6, as previously described. Disabling of this clock pulse during the frame sync pulse and the computer load period is performed by ORing together the computer load signal DOA6-bar U20D-12 and the synchronized frame sync signal CFSR1 U20D-11. When either the computer load signal DOA6-bar the computer frame sync signal CFSR1 are high, NOR gate U20D-13 and inverter U18D-2 apply a high signal to U20D-2, which causes U20D-1 to be low independent of the line sync clock pulse. Only when the computer load signal is in the run state (DOA6-bar is low) and the frame sync signal CSFR1 is low can the line sync clock U20D-1 go high to generate a clock pulse.

The line sync clock U20D-1 is generated from the line sync signal CLS. The CLS signal is latched in flip-flop U22E-12 to generate a resynchronized line sync signal CLSR1. The resynchronized line sync signal CLSR1 is delayed one clock period by latching in flip-flop U22E-15 to generate a delayed resynchronized line sync signal CLSR2. NAND-gate U18E-6 generates a one clock period negative pulse when the resynchronized line sync signal CLSR1 U22E-12 is high and when the delayed

resynchronized line sync signal CLSR2 U22E-15 is still low, indicative of the first clock period of the resynchronized line sync signal. Inverter U21E-10 inverts the delayed line sync signal CLSR2 U22E-15 for NANDing with the non-delayed line sync signal CFSR1 U22E-12 for generation of the one clock period signal U18E-6. Therefore, U20D-1 is a one clock period positive pulse that occurs at the leading edge of each line sync pulse that is disabled by the computer being in the load mode or that is disabled by the frame sync signal. This clock U20D-1 is used to clock the R-registers for updating with the delta parameter at the positive edge and to transfer the updated number in the R-registers to the R-registers at the negative edge.

The computer strobe DOA7 is generated under software control. It is a short positive pulse, typically about 3-microseconds in width. It is NANDed with the computer run signal DOA6 using inverter U18D-6 and NAND-gate U22B-3 to generate a short negative pulse when enabled by the DOA6 run/load-bar signal being low, as indicative of a load command. The negative pulse U22B-3 is used to clock the register that is addressed with the computer destination address signal with decoders U19B and U20B to load data from the computer into that selected register.

Address generator clock gating logic will now be discussed with reference to Fig 6B. This logic is composed of gates U19C, U19D, U18C, U8A, U9A, and U10A. This logic comprises 4-channels of clock logic for the address generation registers, where the clock gating logic for each channel is similar to the clock gating logic for the other 3-channels.

R-register gating logic will now be discussed with reference to Fig 6B.

Gate U19C-1 steers the load strobe 022B-3 to clock the register with the computer generated strobe to load the computer generated parameter into the related register. Steering signal U19C-3 steers the computer pulse U19C-2 to the input of gate U18C-1. Gate U18C-3 combines the two mutually exclusive clock signals, the computer strobe and the line sync strobe to clock the XR-register CXRM with signal U18C-3 for the computer strobe and on the rising edge of the line sync pulse.

Gate U19C-10 steer the load strobe U22B-3 to clock the register with the computer generated strobe to load the computer generated parameter into the related register. Steering signal U19C-9 steers the computer pulse 019C-8 to the input of gate U18C-9. Gate U18C-8 combines the two mutually exclusive clock signals, the computer strobe and the line sync strobe to clock the XR-register CXRL with signal U18C-8 for the computer strobe and on the rising edge of the line sync pulse.

Gate U19D-1 steers the load strobe U22B-3 to clock the register with the computer generated strobe to load the computer generated parameter into the related register. Steering signal U19D-3 steers the computer pulse U19D-2 to the input of gate U18C-4 Gate U18C-6 combines the two mutually exclusive clock signals, the computer strobe and the line sync strobe to clock the YR-register CYRM with signal U18C-6 for the computer strobe and on the rising edge of the line sync pulse.

Gate U19D-13 steers the load strobe U22B-3 to clock the register with the computer generated strobe to load the computer generated parameter into the related register. Steering signal U19D-12 steers the computer

pulse U19D-11 to the input of gate U18C-12. Gate U18C-11 combines the two mutually exclusive clock signals, the computer strobe and the line sync strobe to clock the YR-register CYRL with signal U18C-11 for the computer strobe and on the rising edge of the line sync pulse.

P-register clock logic will now be discussed with reference to Fig 6B.

The XP-register clock signal U9A-6 to XP-register CXPM is generated from the inverted XR-register clock signal CXRM U8A-2, the gated write signal U18E-11, the re-addressing clock U12A-8, and the scanout clock U12A-6. The inverted R-register clock signal U8A-2 causes the XP-register CXRM to be clocked with the computer strobe and with the trailing edge of the line .sync signal, the inverted clock signal from U18C-3. The gated write signal U18E-11 clocks the XP-registers for each write strobe U22C-11 that loads a parameter into memory in order to advance the address generators to the next address. The gated re-addressing clock signal 012A-6 and the gated scanout signal U12A-8 have been discussed above with reference to Fig 6C.

The XP-register clock signal U9A-8 to XP-register CXPL is generated from the inverted XR-register clock signal CXRL U8A-4, the gated write signal U18E-11, the re-addressing clock U12A-8, and the scanout clock U12A-6. The-inverted R-register clock signal 08A-4 causes the XPs-register CXRL to be clocked with the computer strobe and with the trailing edge of the line sync signal, the inverted clock signal from U18C-8. The gated write signal U18E-11 clocks the XP-registers for each write strobe U22C-11 that loads a parameter into memory in order to advance the address generators to

the next address. The gated readdressing clock signal U12A-6 and the gated scanout signal U12A-8 have been discussed above with reference to Fig 6C.

The YP-register clock signal U10A-6 to YP-register CYPM is generated from the inverted YR-register clock signal CYRM U8A-6, the gated write signal 018E-11, the re-addressing clock U12A-8, and the scanout clock U12A-6. The inverted YR-register clock signal USA-6 causes the YP-register CYRM to be clocked with the computer strobe and with the trailing edge of the line sync signal, the inverted clock signal from U18C-6. The gated write signal U18E-11 clocks the YP-registers for each write strobe U22C-11 that loads a parameter into memory in order to advance the address generators to the next address. The gated readdressing clock signal U12A-6 and the gated scanout signal U12A-have been discussed above with reference to Fig 6C.

The YP-register clock signal U10A-8 to YP-register CYPL is generated from the inverted YR-register clock signal CYRL U8A-8, the gated write signal 018E-11 the re-addressing clock U12A-8, and the scanout clock U12A-6. The inverted YR-register clock signal U8A-8 causes the YP-register CYRL to be clocked-with the computer strobe and with the trailing edge of the line sync signal, the inverted clock signal from U18C-11. The gated write signal U18E-11 clocks the YP-registers for each write strobe U22C-11 that loads a parameter into memory in order to advance the address generators to the next address. The gated readdressing clock signal U12A-6 and the gated scanout signal U12A-8 have been discussed above with reference to Fig 6C.

Gates U22C-11, U18D-12, and U18E-11 provide a write strobe to clock the address registers to advance

the address in the address registers in accordance with the delta parameters loaded in the delta registers. This write clock clocking of the address registers is used for writing a sequence of words into memory without the need to reload the address registers, where the address registers are incremented with the write strobe to advance the address from the initially loaded address in accordance with the delta parameters. This write strobe is gated with the DOA5 signal with gate U18E-11 to enable advancing the address generators during the load mode and to disable advancing the address generators during the run mode.

Address Generators

Two address generator configurations are shown in Figs 6O to 6R. The address generators shown in Figs 6O to 6R provide for overflow detection to gate a clock in accordance with the arrangement shown in Fig 6C. The address generators shown in Figs 6O to 6R do not provide for such overflow detection. In this configuration, overflow detection is enhanced by arranging the adder logic so that the overflow from an adder chip coincides with the desired position of overflow detection. In order to provide this feature, an extra adder chip is used in the address generators of Figs 6O and 6P. The address generators shown in Figs 6Q and 6R do not have such overflow detection and consequently can be implemented with one less adder chip.

The XP-address generator will now be discussed with reference to Fig 6O. Register U8D, U9D, and U5D store the address parameter. Register U17D and U7D store the delta parameter for updating the address parameter. Adders U13D to U16D and U6D add the delta parameter to the address parameter to obtain an up-

dated address parameter. Multiplexers U10D to U12D provide for loading initial conditions into the address register during the load mode and provide for updating the address parameter in the address register in response to the delta parameter in the delta register in the run mode.

The delta parameter initial condition is loaded into the delta register from the computer output port. The 6-LSBs from the computer output byte are applied to the D-inputs of delta register U17D and U7D. The CXPB clock provides a clock pulse at the appropriate time, as described with reference to Fig 6B, to clock the initial conditions into the delta registers.

The address parameter initial condition is loaded into 'the address register from the computer output port. The 6-LSBs from the computer output byte are applied to the D-inputs of address register U8D, U9D, and U5D. The CXPM and CXPL clocks provide clock pulses at the appropriate times, as described with reference to Fig 6B, to clock the initial conditions into the address register.

In the run mode, the address register is clocked with the CXPM and CXPL clocks to update the address parameter in response to the delta parameter. The output of the address register; the Q-outputs of the U8D, U9D, and USD register; are applied to the A-inputs of adder circuits U13D to U16D and U6D. The output of the delta register; the 0-outputs of the U17D and U7D register; are applied to the B-inputs of adder circuits U13D to U16D and U6D. The output of the adder circuits on the summation lines is the binary sum of the A-inputs from the address register and the B-inputs from the delta register, providing an updated address parameter

that is input to the address register through the multiplexers to the D-inputs of the address register. Consequently, each time the address register is clocked, the updated address is loaded into the address register and the updated address that is loaded into the address register is output on the Q-lines from the address register to again be added to the delta parameter with the adders to provide the next updated address to the address register.

The multiplexers U10D, U11D, and U12D multiplex the updated address parameter from the adders into the address register to load the initial conditions into the address register at the beginning of the load mode and to load the updated address parameter from the adders thereafter. The ELS signal from U15A-3, as described with reference to Fig 6D, controls the multiplexer to load initial conditions at the start of a line sync pulse and to enable updating of the address parameter with the delta parameter thereafter.

The adders are connected with the carry output from the preceding stage connected to the carry input of the next subsequent stage for a rapid carry propagating through the adder. The adders are arranged so that the overflow from U15D-9 coincides with the point that divides the scanout bits and the re-addressing bits, where the scanout bits are the three less significant bits and the re-addressing bits are the six more significant bits. The next most significant bit XA3 for the XP address generator is used as the board control bit instead of a re-addressing bit for the XP-address generator. The overflow signal U15D-9 is input to U16A-5 and U17A-5 (Fig 6C) for controlling gating of the clock.

The YP-address generator will now be discussed with reference to Fig 6P. Register U8E, U9E, and U5E store the address parameter. Register U17E and U7E store the delta parameter for updating the address parameter. Adders U13E to U16E and U6E add the delta parameter to the address parameter to obtain an updated address parameter. Multiplexers U10E to U12E provide for loading initial conditions into the address register during the load mode and provide for updating the address parameter in the address register in response to the delta parameter in the delta register in the run mode.

The delta parameter initial condition is loaded into the delta register from the computer output port. The 6-LSBs from the computer output byte are applied to the D-inputs of delta register U17E and U7E. The CYPS clock provides a clock pulse at the appropriate time, as described with reference to Fig 6B, to clock the initial conditions into the delta registers.

The address parameter initial condition is loaded into the address register from the computer output port. The 6-LSBs from the computer output byte are applied to the D-inputs of address register U8E, U9E, and U5E. The CYPM and CYPL clocks provide clock pulses at the appropriate times, as described with reference to Fig 6B, to clock the initial conditions into the address register.

In the run mode, the address register is clocked with the CYPM and CYPL clocks to update the address parameter in response to the delta parameter. The output of the address register; the Q-outputs of the U8E, U9E, and USE register; are applied to the inputs of adder circuits U13E to U16E and U6E. The output of the delta

register; the Q-outputs of the O17E and U7E register; are applied to the B-inputs of adder circuits U13E to U16E and U6E. The output of the adder circuits on the summation lines is the binary sum of the A-inputs from the address register and the B-inputs from the delta register, providing an updated address parameter that is input to the address register through the multiplexers to the D-inputs of the address register. Consequently, each time the address register is clocked, the updated address is loaded into the address register and the updated address that is loaded into the address register is output on the Q-lines from the address register to again be added to the delta parameter with the adders to provide the next updated address to the address register.

The multiplexers U10E, U11E, and U12E multiplex the updated address parameter from the adders into the address register to load the initial conditions into the address register at the beginning of the load mode and to load the updated address parameter from the adders thereafter. The ELS signal from U15A-3, as described with reference to Fig 6D, controls the multiplexer to load initial conditions at the start of a line sync pulse and to enable updating of the address parameter with the delta parameter thereafter.

The adders are connected with the carry output from the preceding stage connected to the carry input of the next subsequent stage for a rapid carry propagating through the adder. The adders are arranged so that the overflow from U15E-9 coincides with the point that divides the scanout bits and the re-addressing bits, where the scanout bits are the three less significant bits and the re-addressing bits are the six more significant bits.

The overflow signal U15E-9 is input to U16A-2 and U17A-2 (Fig 6C) for controlling gating of the clock.

The XR-address generator will now be discussed with reference to Fig 6Q. Register U8B, U9B, and U5B store the address parameter. Register U17B and U7B store the delta parameter for updating the address parameter. Adders U13B to U15B and U6B add the delta parameter to the address parameter to obtain an updated address parameter. Multiplexers U10B to U12B provide for loading initial conditions into the address register during the load mode and provide for updating the address parameter in the address register in response to the delta parameter in the delta register in the run mode.

The delta parameter initial condition is loaded into the delta register from the computer output port. The 6-LSBs from the computer output byte are applied to the D-inputs of delta register U17E and U7B. The CXRS clock provides a clock pulse at the appropriate time, as described with reference to Fig 6B to clock the initial conditions into the delta registers.

The address parameter initial condition is loaded into the address register from the computer output port. The 6-LSBs from the computer output byte are applied to the D-inputs of address register U8B, U9B, and U5B. The CXRM and CXRL clocks provide clock pulses at the appropriate times, as described with reference to Fig 6B, to clock the initial conditions into the address register.

In the run mode, the address register is clocked with the CXRM and CXRL clocks to update the address parameter in response to the delta parameter. The output of the address register; the Q-outputs of the U9B, U9B,

and U5B register; are applied to the A-inputs of adder circuits U13B to U15B and U6B. The output of the delta register; the Q-outputs of the U17B and U7B register; are applied to the B-inputs of adder circuits U13B to U15B and U6B. The output of the adder circuits on the summation lines is the binary sum of the A-inputs from the address register and the B-inputs from the delta register, providing an updated address parameter that is input to the address register through the multiplexers to the D-inputs of the address register. Consequently, each time the address register is clocked, the updated address is loaded into the address register and the updated address that is loaded into the address register is output on the D-lines from the address register to again be added to the delta parameter with the adders to provide the next updated address to the address register.

The multiplexers U10B, U11B, and U12B multiplex the updated address parameter from the adders into the address register to load the initial conditions into the address register during the load mode and to load the updated address parameter from the adders during the run mode. The DOA6-bar signal from U18D-6, as described with reference to Fig 6B, controls the multiplexer to load initial conditions in the load mode and to enable updating of the address parameter with the delta parameter in the run mode.

The adders are connected with the carry output from the preceding stage connected to the carry input of the next subsequent stage for a rapid carry propagating through the adder.

The YR-address generator will now be discussed with reference to Fig 6R. Register U8C, U9C, and O5C store the address parameter. Register U17C and U7C store

the delta parameter for updating the address parameter. Adders U13C to U15C and U6C add the delta parameter to the address parameter to obtain an updated address parameter. Multiplexers U10C to U12C provide for loading initial conditions into the address register during the load mode and provide for updating the address parameter in the address, register in response to the delta parameter in the delta register in the run mode.

The delta parameter initial condition is loaded into the delta register from the computer output port. The 6-LSBs from the computer output byte are applied to the D-inputs of delta register U17C and U7C. The CYRS clock provides a clock pulse at the appropriate time, as described with reference to Fig 6B, to clock the initial conditions into the delta registers.

The address parameter initial condition is loaded into the address register from the computer output port. The 6-LSBs from the computer output byte are applied to the D-inputs of address register U8C, U9C, and U5C. The CYRM and CYRL clocks provide clock pulses at the appropriate times, as described with reference to Fig 6B, to clock the initial conditions into the address register.

In the run mode, the address register is clocked with the CYRM and CYRL clocks to update the address parameter in response to the delta parameter. The output of the address register; the Q-outputs of the U8C, U9C, and U5C register; are applied to the A-inputs of adder circuits U13C to U15C and U6C. The output of the delta register; the Q-outputs of the U17C and U7C register; are applied to the B-inputs of adder circuits U13C to U15C and U6C. The output of the adder circuits on the

summation lines is the binary sum of the A-inputs from the address register and the B-inputs from the delta register, providing an updated address parameter that is input to the address register through the multiplexers to the D-inputs of the address register. Consequently, each time the address register is clocked, the updated address is loaded into the address register and the updated address that is loaded into the address register is output on the Q-lines from the address register to again be added to the delta parameter with the adders to provide the next updated address to the address register.

The multiplexers U10C, U11C, and U12C multiplex the updated address parameter from the adders into the address register to load the initial conditions into the address register during the load mode and to load the updated address parameter from the adders during the run mode. The DOA6-bar signal from U18D-6, as described with reference to Fig 6B, controls the multiplexer to load initial conditions in the load mode and to enable updating of the address parameter with the delta parameter in the run mode.

The adders are connected with the carry output from the preceding stage connected to the carry input of the next subsequent stage for a rapid carry propagating through the adder.

Output of the address signals will now be discussed with reference to Figs 6O and 6P. The Q-outputs of the XP-address register and YP-address register are routed to the memory for. accessing and for loading of information. The address connections between the memory and the address generators are listed in the CABLE CONNECTION TABLE here under the heading CABLE-I BM1,2/BL1 (C1). The Y-address bits Y0 to Y8 and the

X-address bits X0 to X8, including the complemented and uncomplemented X3 memory board address select bit, are listed therein together with source circuits on the control logic board and destination circuits on the memory boards.

In the run mode, the XP-address register and YP-address register are continually clocked with the gated clock, as discussed with reference to Fig 6B); resulting in the address parameters being continually updated with the delta parameters and resulting in the memory being continually addressed by the update address parameters. The XA3 and XA3-bar memory board select signals are gated with U19A-1 in order to blank the CRT monitor and clear the buffer, as discussed with reference to Fig 6D herein.

MEMORY BOARDS

A detailed design of one configuration of the memory of the present invention is shown in Figs 6E to 6N. The architecture of one of the memory boards is shown in block diagram form in Fig 6E, is shown in detailed block diagram form in Figs 6F to 6J, and is shown in detailed logical-diagram form in Figs 6K to 6N. Commonality of symbols and features in these diagrams provide for cross referencing to different levels of detail between these diagrams. This memory uses Mitsubishi M58725P RAMs having 16,384 (16K) bits per RAM, organized in a 2,048 (2K) words by 8-bits per word configuration. Logical diagrams of RAM chips are shown in Figs 6K to 6N. Each RAM chip comprises 11-address lines A0 to A10, 8-data lines DQ1 to DQ8, a chip select line S-bar, an output enable line OE-bar, and a write pulse line W-bar. The address lines address 1-word out of 2K-words stored in the memory chip. The data lines output the

addressed word in the read mode and input a word for storage in the write mode. The data lines are tristate line a that, when in the read mode, output the addressed information when enabled with the chip select line S-bar and, when in the write mode, store the data in the addressed location. The output enable signal G-bar controls inputting and outputting of data from the RAM. When disabled with the chip select line or the output enable line, the data lines are in the floating tristate condition.

The memory control logic is comprised of circuits U19A to U19E, as shown in Fig 6F. Buffers U19A and U19D are non-inverting buffers that buffer the address signals for fanout to the RAMs. In this configuration, 11-address signals YA3B to YA8B and XA4B to XABB are fanned out to the address inputs A0 to A10 of the RAMs. Decoders U19B, U19C, and U19E decode the scanout portion of the address word for control of the tristate data lines of the RAMs. Decoder U19B decodes the Y-scanout portion YA0 to YA2 of the scanout portion of the Y-address. Decoders U19C and U19E decode the X-scanout portion XA0 to XA2 of the X-scanout portion of the address. Decoder U19C is enabled for read operations and decoder U19E is enabled for write operations. Each of decoders; U19B, U19C, and U19E; receive 3-input scanout address lines and generate 8-decoded scanout control lines in response to the decoding. Decoded signals MY0-bar to MY7-bar from U19B generate Y-control signals to select one column of 8-RAMs with the chip select pin S-bar. Decoded signals MX0R-bar to MX7R-bar from U19C generate X-control signals in the read mode to select one row of 8-RAMs with the output enable pin G-bar. Decoded signals MX0W-bar to MX7W-bar from U19E generate X-control signals in the

write mode to select one row of 8-RAMs with the output enable pin G-bar. Therefore, selection of a column of 8-RAMs with the Y-scanout signals and selection of a row of 8-RAMs with the X-scanout signals selects a single RAM common to both the selected row and the selected column for read and write operations.

The decoders have gating signals E1-bar E2-bar, and E3. Signals E1-bar and E2-bar are permanently enabled on decoders U19B and U19C with a ground connection and signal E3 is permanently enabled on decoder U19E with a pullup connection. Signal E3 on decoder U19B is used to place the RAMs on the non-selected memory board in the standby mode for reduced power consumption. This is achieved by disabling U19B on the non-selected board and enabling U19B on the selected board with the XA3 and XA3-bar signals, which select the board to be utilized. Disabling U19B on the non-selected board disables the Y-scanout signals to the chip select pin S-bar, which in turn places the non-selected RAMs into the standby mode for reduced power consumption. The XA3 and XA3-bar gating of the U19B decoder is not necessary for-memory operation, but is used for reduction of power consumption. Pin E3 on decoder U19C and pin E2-bar on decoder U19E are controlled with the DIEN-bar signal which is derived from the computer run/load mode signal for enabling decoder U19C in the run mode to read from memory, to disable decoder U19E in the run mode to prevent writing into memory, to enable decoder U19E in the load mode to write into memory and to disable decoder B19C in the load mode to read from memory. When decoder U19E is enabled in the load mode, the write pulse W-bar controls decoder U19E; where decoder U19E effectively steers the W-bar write pulse to the one of eight decoded

signal lines MX0W-bar to MX7W-bar under control of the XA0, XA1, and XA2 scanout address signals.

A discussion will now be provided relative to Figs 6G to 6N to illustrate the logical design of the memory. Figs 6G to 6K each show 16-RAMs organized in 2-logical columns and constructed on one row on a memory board, where each memory board has 4-groups of 16-RAMs each shown in one of Figs 6G to 6J. The manner in which these 4-pairs of logical columns connect together is shown in Fig 6E and is shown by the interconnections between Figs 6G to 6J and Figs 6K to 61x1 and by the discussions hereinafter.

All RAMs are addressed by the same 11-address lines; shown as the address bus to the A-input of each RAM in Figs 6G to 6J and shown in greater detail as the address bus to the AU to A10 inputs of RAMs U8 and 016 for each pair of logical columns in Figs 6K to 6N. The addresses are placed on the address bus by O19A and U19D (Fig 6F) and are routed to all 16-RAMs on each of the RAM groups (Figs 6G to 6J) to excite the RAM address inputs A (Figs 6G to 6J) and A0 to A10 (Figs 6K to 6N).

Each logical column of RAMs is selected by a single one of the eight Y-scanout signals from U19B (Fig 6F), shown connected to the S-bar pin of each RAM in the logical column in Figs 6G to 6J and shown in greater detail to the S-bar inputs of RAMs U8 and U16 for each pair of logical columns in Figs 6K to 6N.

Each logical row of RAMs is selected by a single one of the eight X-scanout signals; MX0R to MX7R in the read mode to the output enable pin G-bar and MX0W to MX7W in the write mode to the W-bar from U19C and U19E respectively (Fig 6F). Each of these signals are

shown connected to the pair of RAM in the logical row for each pair of logical columns in Figs 6G to 6J and shown in greater detail for RAMs U8 and U16 for each pair of logical columns in Figs 6K to 6N. Each of these X-scanout signals enable the same pair of RAMs in each of the 4-pairs of logical columns (Figs 6G to 6J and Figs 6K to 6N).

All RAMs in the pair of columns shown in each of Figs 6G to 6J and Figs 6K to 6N have the corresponding data bus pins A collected together; shown as the data bus to the D-input of each RAM in Figs 6G to 6J and shown in greater detail as the data bus to the D0 to D7 pins of RAMs U8 and U16 for each pair of logical columns in Figs 6K to 6N. The data bus and control signals are connected to a pair of Intel 8216 bus interface chips for each pair of logical columns, as shown in simplified form in Figs 6G to 6J and in detailed form in Figs 6K to 6N. The operation of the data bus interface is discussed in greater detail hereinafter.

In view of the above, all RAMs are addressed with the same address signals and one RAM that is at the intersection of the enabled X-row scanout signal and the enabled Y-column scanout signal alone is permitted to place the addressed word on the data bus in the read mode and alone is written into at the addressed location from the data bus.

In the read mode, one RAM is enabled to output the addressed word onto the system data bus. This can be implemented by busing together the corresponding 8-data lines from each RAM. However, busing together a large number of RAM data lines, such as 128-RAM data lines in this configuration, can result in reduced RAM speed, such as due to bus and chip capacitance. There-

fore, Intel 8216 bi-directional bus drivers are provided to isolate groups of RAMs from the system data bus and from other groups of RAMs.

The system data bus interface will now be described with reference to Figs 6K to 6N. Fig 6K shows the data bus interface for row-A on each of the two memory boards. Fig 6L shows the data bus interface for row-B on each of the two memory boards. Fig 6M shows the data bus interface for row-C on each of the two memory boards. Fig 6N shows the data bus interface for row-D on each of the two memory boards.

For this configuration, 16-RAMs are bused together through each system data bus interface circuit, comprising two Intel 8216 components. The bi-directional signals DB0, DB1, DB2, and DB3 are connected to the RAM data bus and the uni-directional signals DI0 and DO0, DI1 and DO1, DI2 and DO2, and DI3 and DO3 are connected to the uni-directional system bus for reading from RAM through the DO0 to D03 unidirectional outputs and for writing into RAM on the DIO to DI3 unidirectional inputs. A pair of Intel 8216 4-bit bus drivers are used to control the 8-data bus lines for the RAM data bus.

The Intel 8216s are controlled with the board select signal XA3 or XA3-bar and the scanout address select signals for the 2-columns of RAMs associated with the Intel 8216 circuits. The board select signal, XA3-bar for memory board-1 and XA3 for memory board-2, control all of the Intel 8216s on the board. Therefore, the Intel 8216s on the enabled board are partially enabled to connect the RAM databases on that board to the system bus and the Intel 8216 on the disabled board are fully art disabled to disconnect the RAM on that board from the

system bus. Similarly, the column select signals for the 2-columns of RAMs connected to the particular Intel 8216s are controlled with the column select signals so that the column select signal enabling a column of RAMs will also partially enabled the Intel 8216s associated with that column to connect the selected column data bus to the system data bus. Because 2-columns of RAMs are connected to each Intel 8216 circuit, the related column select signals are ORed together with a NAND gate; where the column select signals are in complement logic form and consequently a NAND gate can perform an OR function; and are then ANDed with the board select signal XA3 or XA3-bar in a second NAND gate in non-complement logic form to generate the control signal in complement logic form as needed for the Intel 8216 chip select. The Intel 8216 circuits are steered with the DIEN-bar control, which is connected to the DIEN signal generated with U21E-6 (Fig 6B). Therefore, in the run mode; the DIEN signal controls the Intel 8216s to connect the RAM data bus through the DO0 to DO3 buffers to output the RAM signals onto the system output data bus and, in the load mode; the DIEN signal controls the Intel 8216s to connect the RAM data bus through the DI0 to DI3 buffers to input the write signals from the system data bus to the RAMs.

Row A on the board has 2-logical columns of RAMs (Figs 6G and 6K), comprising the first column with RAMs UA to U8A and the second column with RAMs U9A to U16A. As shown in greater detail with reference to Figs 6K to 6N; the first column is selected with the MY0-bar column select scanout signal and the second column is selected with the MY1-bar column select signal. The 2-column select signals are ORed together with

U18E-3 and are ANDed with the board select signal with U18E-6 to enable U17A and U18A.

Row B on the board has 2-logical columns of RAMS (Figs 6H and 6L), comprising the third column with RAMs U1B to U8B and the fourth column with RAMs U9B to D16B. As shown in greater detail with reference to Figs 6K to 6N; the third column is selected with the MY2-bar column select scanout signal and the fourth column is selected with the MY3-bar column select signal. The 2-column select signals are ORed together with U18E-8 and are ANDed with the board select signal with U18E-11 to enable U17B and U18B.

Row C on the board has 2-logical columns of RAMs (Figs 6I and 6M), comprising the fifth column with RAMs U1C to U8C and the sixth column with RAMS U9C to U16C. As shown in greater detail with reference to Figs 6K to 6N; the fifth column is selected with the MY4-bar column select scanout signal and the sixth column is selected with the MY5-bar column select signal. The 2-column select signals are ORed together with U17E-3 and are ANDed with the board select signal with U17E-6 to enable U17C and U18C.

Row D on the board has 2-logical columns of RAMs (Figs 6J and 6N), comprising the seventh column with RAMs U1D to U8D and the eighth column with RAMs U9D to U16D. As shown in greater detail with reference to Figs 6K to 6N; the seventh column is selected with the MY6-bar column select scanout signal and the eighth column is selected with the MY7-bar column select signal. The 2-column select signals are ORed together with U17E-8 and are ANDed with the board select signal with U17E-11 to enable U17D and U18D.

BUFFER BOARD

General

The buffer board is implemented with a buffer to buffer the outputs of image memory and to apply these outputs to the rear-end board (Fig 6A). The buffer can be implemented with various forms of buffer memories, such as double buffers and FIFOs. Alternately, the buffer can be eliminated and the memory output can be routed directly to the rear-end board.

The CABLE CONNECTION TABLE provided herein illustrates on arrangement for connecting the buffer board in between the memory and logic boards and the rear-end board. The buffer board receives memory information and a gated clock from the memory and logic boards to clock the memory information into the buffer and receives a rear-end board clock to clock the buffered information into the rear-end board, as generally discussed with reference to Fig 6A.

Alternately, the memory and logic boards can provide the unbuffered information directly to the rear-end board without an intervening buffer board for clocking the memory information into the DACs on the rear-end board with the gated clock from the logic board.

4/3 Buffer Implementation

The 4/3 buffer will now be discussed with reference to Figs 6W to 6AD. A precessional approach is shown controlled with counter U8A decoded with decoder U12B to identify which of the 4-precessional conditions exists for each line-buffer (Fig 6W). This decoded number controls which of the 4-lines of buffer memory are selected for each of the 4-operational positions; the input line buffer, the output line-buffer channel-1, the output line-buffer channel-2, and the output line-buffer channel-3

positions. As the precessional counter sequences through its 4-states, the precessional decoder sequences through the 4-select signals to control sequential precessional operation. The selection logic is shown in the BUFFER MEMORY MULTIPLEXER ASSIGNMENT TABLE, where the input processional counter states are shown decoded into the decoded states and shown further decoded into the single input line-buffer select, signal, the 3-output line-buffer select signal, and the output weight select signal.

BUFFER MEMORY MULTIPLEXER ASSIGNMENT TABLE

INPUT

CNTR INPUT STATE	DATA ABCD	IN ADD. COUNTER ABCD
00	1000	1000
01	0100	0100
10	0010	0010
11	0001	0001

OUTPUT

OUT ADD. COUNTER ABCD	CH-I ABCD	CH-II ABCD	CH-III ABCD	WEIGHT ABCD
0111	0100	0010	0001	0010
1011	0010	0001	1000	0001
1101	0001	1000	0100	1000
1110	1000	0100	0010	0100

NOTES:

1) INPUT DATA assignments are the same as ADD. COUNTER assignments.

2) OUTPUT CH-II assignments are the same as OUTPUT WEIGHT assignments.

3) INPUT ADD COUNTER assignments are the complement of OUTPUT ADD. COUNTER assignments.

The 4/3rds buffer is shown implemented with two address counters, an input address counter controlled by

the image processor and the image memory clock and an output address counter controlled by the CRT monitor clock. The input address counter controls a single line-buffer that is being loaded by the image processor. The output address counter controls three line-buffers outputting to the spatial filter. Address multiplexing logic consists of multiplexers that select either the input counter or the output counter for the address input of each line-buffer RAM in accordance with the input columns in the BUFFER MEMORY MULTIPLEXER ASSIGNMENT TABLE. Similarly, this logic selects the write mode for the line buffer being loaded and selects the read mode for the 3-line-buffers being unloaded.

Similar to the address selection discussed above, the input and output signals to the RAM line-buffer being loaded and from. the RAM line-buffer being unloaded are shown implemented with input multiplexers U4F, U5F, U6F, U8F, U9F, U10F, U12F, U13F, U14F, U16F, U17F, and U18F and output multiplexers U3D, U4D, U5D, U6D, U7D, U8D, U9D, U10D, U11D, U12D, U13D, U14D, U15D, U16D, U17D, and U18D. The single line-buffer, selected for inputting and operating under control of the input address counter, receives input data from the image processor for storing therein. The 3-line buffers, selected for outputting and operating under control of the output address counter, generates output data to the post-processor for exciting the display. The output channel of each of the line buffers is controlled for outputting to each of the 3-output channels under control of the precessional decoder signals. Each of the 3-line buffers selected for outputting are selected for outputting to different output channels; channel-1, channel-2, and channel-3; under control of the

precessional decoder signals; as shown in the OUTPUT columns of the BUFFER MEMORY MULTIPLEXER ASSIGNMENT TABLE. Similarly, the spatial filtering weight is selected from the channel-2 line-buffer, as shown in the WEIGHT column of the BUFFER MEMORY MULTIPLEXER ASSIGNMENT TABLE.

In view of the above and in view of the referenced schematics and block diagrams, a buffer memory is provided that inputs pixel information to any one of 4-line-buffers and outputs pixel information from any one of 4-line-buffers to any one of 3-output channels. Also, sequential operation is provided that sequentially applies each of the 4-line buffers to each of the positions of input buffer, channel-1 output buffer, channel-2 output buffer, and channel-3 output buffer for loading of a single line into a line-buffer and simultaneously for outputting of 3-parallel lines into a post-processor.

The buffer memory is shown implemented to store both weight address information for weight determination and pixel intensity information. The pixel intensity information is loaded into an interface pipeline (kernel) register, such as for use with the post processor, such as a spatial processor. The weight address information is converted to weight information with a table lookup in a weight-RAM. Weight address information is stored in the line-buffer to implement interpolation in the post-processor; which, in one configuration may be more efficiently implemented with weight address information. Alternately, the weight address information can be converted to weight information before loading into the line buffers, such as with a weight RAM, for storing of weight information instead of weight address information in the buffer memory.

A register interface is provided in between the buffer memory and the post-processor. The registers may be considered to be implemented in a pipeline form to enhance performance and to provide stable latched signals for the post-processor. The registers are implemented to store 9-pixels in a 9-pixel kernel arrangement for processing with a post-processor. Also, a weight RAM is provided that stores weight information in response to weight address information from the buffer memory.

The memory components are Intel 2149H RAMs. The logic components are 7400 series logic, particularly 74LS, 74AL5, and 74AS circuits; such as produced by Texas Instruments.

Alternately, the buffer memory can be implemented with other components.

Buffer Memory Address Counters

The buffer memory is composed of one line buffer selected as an input line buffer and 3-line buffers selected as output line buffers. Separate address counters are used to generate addresses for the input line buffer and to generate addresses for the output line buffers so that loading of data into the input line buffer can proceed asynchronously with respect to outputting of data from the output line buffers. The output address counter is. discussed relative to Fig 6X and the input address counter is discussed relative to Fig 6W below.

Control logic for the address counters is shown in Fig 6X, comprising flip-flops U1A and gates U1B-1, U2B-3, AND U2B-6. Gate U1B-1 receives and inverts the line sync signal CLS for loading into flip-flops U1A. The inverted line sync pulse is shifted through flip-flops U1A-2 and U1A-7 and the leading edge is detected with gate U2B-3 and the trailing edge is detected with gate

U2B-6. Leading edge detection is performed by NANDing the once delayed complemented and the twice delayed uncomplemented shifted CLS-signal with gate U28-3. Trailing edge detection is performed by NANDing the once delayed uncomplemented and the twice delayed complemented shifted CLS-signal with gate U2B-6. Therefore, gate U2B-3 will generate a 1-clock period negative going pulse at the leading edge of the CLS-signal and gate U2B-6 will generate a 1-clock period negative going pulse at the trailing edge of the CLS-signal for synchronizing the input address counter and the output address counter to the line sync signal, respectively.

As discussed above, the input line buffer can be controlled to commence loading of information at the beginning of the line sync period to provide extra time to load the line buffer and the output line buffer can be controlled to commence outputting of information at the end of the line sync period to synchronize outputting of pixel information with completion of the blanking pulse.

Clock fanout logic is shown in Fig 6X, where AND gate U7B3 receives the complemented early clock CPE-bar and provides a non-inverting delay and inverters U8B-2, U8B-4, and U8B-6 provide the inverted and delayed CPD clock signal.

The output address counter will now be discussed with reference to Fig 6X. The output address counter is composed of counters U2A, U3A, and U4A. This counter is connected as a synchronous 12-bit counter by connecting the TC-signal on pin-15, the CEP-signal on pin-7, and the CET-signal on pin-10 between the different stages in the manner shown. The output counter is clocked under control of the output pixel clock CPE-bar

inverted and delayed to the CPD clock signal to generate 10-address signals to the output address bus (or read address bus) to the buffer memories. The output address counter is cleared with the trailing edge pulse from U2B-6 to the counter clear input PE-bar on pin-9 at the end of the line blanking period to initiate address counting from the first address in the buffer memory coincident with the beginning of the line blanking CLS-signal.

The input address counter will now be discussed with reference to Fig 6W. The input address counter is composed of counters U5A, U6A, and U7A. This counter is connected as a synchronous 12-bit counter by connecting the TC-signal on pin-15, the CEP-signal on pin-7, and the CET-signal on pin-10 between the different stages in the manner shown. The input counter is clocked under control of the input pixel gated clock CPG C3-22 to generate 10-address signals to the input address bus (or write address bus) to the buffer memories. The CPG clock is the gated clock generated on the control logic board with gate U21D-8. The input address counter is cleared with the leading edge pulse from U2B-3 to the counter clear input PE-bar on pin-9 at the beginning of the line blanking period to initiate address counting from the first address in the buffer memory coincident with the end of the line blanking CLS-signal.

The buffer memory multiplexer control will now be discussed with reference to Fig 6W. The multiplexer logic has been discussed with reference to the BUFFER MEMORY MULTIPLEXER ASSIGNMENT TABLE above. Counter U8A is a modulo-3 counter, counting from 0 to 3 and then overflowing to 0 again. It counts in response to the leading edge pulse from U2B-3, inverted

with U13B-10, and applied to the CEP and CET inputs to increment counter U8A. Consequently, counter U8A is incremented at the beginning of each line sync pulse for changing the buffer memory multiplexing on a scanline-by-scanline basis. The modulo-3 count is decoded by decoder U12B to generate one of four mode signals; F0-bar, Fl-bar, F2-bar, and F3-bar in response to the state of counter U8A. The decoded mode signal controls the buffer memory multiplexer in accordance with the assignments in the BUFFER MEMORY MULTIPLEXER ASSIGNMENT TABLE.

Line Buffer Memory

The line buffer memory is composed of 4-line buffers shared to implement a multiple buffer configuration. These 4-line buffers are similar in design and operate under control of multiplexer signals and address signals.

The first line buffer will now be discussed with reference to Figs 6Y and 6Z. Four RAM circuits U3E to U6E are addressed through tristate multiplexers U3C to U6C. Multiplexers U3C and U4C select the write address from the write bus (or input bus) and multiplexers U5C and U6C select the read address from the read bus (or output bus) under control of the mode control signal F0-bar U12B-4 in accordance with the logic shown in the BUFFER MEMORY MULTIPLEXER ASSIGNMENT TABLE. Multiplexers U3C and U4C are selected with the F0-bar signal and multiplexers U5C and U6C are selected with the F0-bar signal complemented with U13B-2. The selected address is applied to the address inputs on RAMs U3E to U6E. The write multiplexer U4C also multiplexes the write pulse to U4C-11 and to the write inputs to the RAMs WE-bar on pin-10. When the write multiplexer

U3C and U4C is selected, the write address is applied to RAMs U3E to U6E and the write pulse CPG is applied to the write input WE bar of the RAMs. When the read multiplexer U5C and U6C is selected, the read address is applied to RAMs U3E to U6E and the write pin-10 WE-bar is pulled up to select read operations.

The RAM input and output lines IO0 to IO3 are shared between outputting of information in the read mode and inputting of information in the write mode. Input information is selected with line buffers U4F to O6F, which apply input information obtained from the input bus to the RAM IO lines in the write mode and which are tristate-disabled to disconnect the input information on the input bus from the RAM IO lines in the read mode. Line buffers U4F to U6F are controlled with the F0-bar multiplexer, control signal to connect the input bus to the RAM IO lines when the F0-bar signal enables the write address and the write pulse through multiplexers U3C and U4C and to disconnect the input bus from the RAM IO lines when the F0-bar signal enables the read address and disables the write address and write pulse. Hence, line buffers U4F to U6F are enabled when the RAM channel is in the write mode and are disabled when the RAM channel is in the read mode. As can be seen from the schematic, line buffers U4F to U6F apply the 8-intensity bits from image memory over the buffer input bus to the inputs of RAMs U3E and U4E and apply the weight addresses from the address generators over the buffer input bus to the inputs of RAMs U5E and U6E, with 2-spare bits presently unassigned.

Output information is multiplexed onto the buffer output buses; identified as the channel-I bus, the

channel-II bus, the channel-III bus, and the weight bus. The 3-channel buses comprising the pixel intensities from the 3-output line buffers are applied to the 3-channels of kernel registers. The weight bus, comprising the weight addresses of the selected channel, is applied to the single channel of weight registers U22A and U22B for accessing the weight RAM.

The 8-intensity lines from RAMs U3E and U4E are applied to all 3-channels through different multiplexers so that the intensity lines can be selected for one of the 3-output channels or for none of the 3-output channels under control of multiplexers U3D to U6D. Because each intensity parameter and each output channel has 8-bits, because each multiplexer U3D to U6D has 6-bits, and because the 74LS367 multiplexers can each control separately 4-bits and 2-bits, the 8-bits selected for one of 3-channels are partitioned between a pair of multiplexers. For example, the intensity bits from RAMs U3E and U4E are controlled with multiplexers U3D and U4D for channel-I, with multiplexers U4D and U5D for channel-II, and with multiplexers 05D and U6D for channel-III. The specific partitioning of intensity bits and multiplexers is shown in the schematic diagram. The multiplexing of the intensity bits onto the channel-I bus is controlled with the F1-bar multiplexer control signal to control all of multiplexer U3D and 2-bits of multiplexer U4D. The multiplexing of the intensity byte onto the channel-II bus is controlled with the F2-bar multiplexer control signal to control 4-bits of multiplexer U4D and 4-bits of multiplexer U5D. The multiplexing of the intensity byte onto the channel-III bus is controlled with the F3-bar multiplexer control signal to control 2-bits of multiplexer USD and all 6-bits of multiplexer U6D. Consequently, multiplexers U3D to

U6D multiplex the 8-intensity bits from RAMs U3E and U4E onto one of the 3-output channel buses under control of the multiplexer control signals-in accordance with the definitions shown in the BUFFER MEMORY MULTIPLEXER ASSIGNMENT TABLE.

The 6-weight address lines are applied to the weight bus under control of multiplexer U6B as output from RAMs U5E and U6E. This first RAM buffer line outputs to the weight bus under control of the F2-bar signal. Consequently, when the first line buffer is selected with the F2-bar signal to output the stored intensity onto the channel-II bus through multiplexers U4D and U5D, the weight addresses from RAMs U5E and U6E are applied to the weight bus through multiplexer U6B under control of the F3-bar signal.

The second line buffer will now be discussed with reference to Figs 6AA and 6AB. Four RAM circuits U7E to U10E are addressed through tristate multiplexers U7C to U10C. Multiplexers U7C and U8C select the write address from the write bus (or input bus) and multiplexers U9C and U10C select the read address from the read bus (or output bus) under control of the mode control signal F1-bar U12B-5 in accordance with the logic shown in the BUFFER MEMORY MULTIPLEXER ASSIGNMENT TABLE. Multiplexers U7C and U8C are selected with the F1-bar signal and multiplexers U9C and U10C are selected with the F1-bar signal complemented with U13B-4. The selected address is applied to the address inputs on RAMs U7E to U10E. The write multiplexer U8C also multiplexes the write pulse to U8C-11 and to the write inputs to the RAMs WE-bar on pin-10. When the write multiplexer U7C and U8C is selected, the write address is applied-to

RAMs U7E to U10E and the write pulse CPG is applied to the write input WE-bar of the RAMs. When the read multiplexer U9C and U10C is selected, the read address is applied to RAMs U7E to U10E and the write pin-10 WE-bar is pulled up to select read operations.

The RAM input and output lines IO0 to IO3 are shared between outputting of information in the read mode and inputting of information in the write mode. Input information is selected with line buffers U8F to U10F, which apply input information obtained from the input bus to the RAM IO) lines in the write mode and which are tristate-disabled to disconnect the input information on the input bus from the RAM IO lines in the read mode. Line buffers U8F to U10F are controlled with the F1-bar multiplexer control signal to connect the input bus to the RAM IO lines when the F1-bar signal enables the write address and the write pulse through multiplexers U7C and U8C and to disconnect the input bus from the RAM IO lines when the F1-bar signal enables the read address and disables the write address and write pulse. Hence, line buffers U8F to U1OF are enabled when the RAM channel is in the write mode and are disabled when the RAM channel is in the read mode. As can be seen from the schematic, line buffers U8F to U10F apply the 8-intensity bits from image memory over the buffer input bus to the inputs of RAMs U7E and U8E and apply the weight addresses from the address generators over the buffer input bus to the inputs of RAMs U9E and U10E, with 2-spare bits presently unassigned.

Output information is multiplexed onto the buffer output buses; identified as the channel-I bus, the channel-II bus, the channel-III bus, and the weight bus.

The 3-channel buses comprising the pixel intensities from the 3-output line buffers are applied to the 3-channels of kernel registers. The weight bus, comprising the weight addresses of the selected channel, is applied to the single channel of weight registers U22A and U22B for accessing the weight RAM.

The 8-intensity lines from RAMs U7E and U8B are applied to all 3-channels through different multiplexers so that the intensity lines can be selected for one of the 3-output channels or for none of the 3-output channels under control of multiplexers U7D to U10D. Because each intensity parameter and each output channel has 8-bits, because each multiplexer U7D to U10D has 6-bits, and because the 74LS367 multiplexers can each control separately 4-bits and 2-bits, the 8-bits selected for one of 3-channels are partitioned between a pair of multiplexers. For example, the intensity bits from RAMs U7E and U8E are controlled with multiplexers U7D and U8D for channel-I, with multiplexers U8D and U9D for channel-II, and with multiplexers U9D and U1OD for channel-III. The specific partitioning of intensity bits and multiplexers is shown in the schematic diagram. The multiplexing of the intensity bits onto the channel-1 bus is controlled with the F2-bar multiplexer control signal to control all of multiplexer U7D and 2-bits of multiplexer U8D. The multiplexing of the intensity byte onto the channel-II bus is controlled with the F3-bar multiplexer control signal to control 4-bits of multiplexer U8D and 4-bits of multiplexer U9D. The multiplexing of the intensity byte Onto the channel-III bus is controlled with the F0-bar multiplexer control signal to control 2-bits of multiplexer U9D and all 6-bits of multiplexer U10D. Consequently, multiplexers U7D to U10D multiplex the 8-intensity bits from RAMs U7E

and U8E onto one of the 3-output channel buses under control of the multiplexer control signals in accordance with the definitions shown in the BUFFER MEMORY MULTIPLEXER ASSIGNMENT TABLE.

The 6-weight address lines are applied to the weight bus under control of multiplexer U9E as output from RAMs U9E and U10B. This first RAM buffer line outputs to the weight bus under control of the F3-bar signal. Consequently, when the first line buffer is selected with the F3-bar signal to output the stored intensity onto the channel-II bus through multiplexers U8D and U9D, the weight addresses from RAMs U9E and U10E are applied to the weight bus through multiplexer U10B under control of the F3-bar signal.

The third line buffer will now be discussed with reference to Figs 6AC and 6AD. Four RAM circuits U11E to U14E are addressed through tristate multiplexers U11C to U14C. Multiplexers U11C and U12C select the write address from the write bus (or input bus) and multiplexers U13C and U14C select the read address from the read bus (or output bus) under control of the mode control signal F2-bar 012B-6 in accordance with the logic shown in the BUFFER MEMORY MULTIPLEXER ASSIGNMENT TABLE. Multiplexers U11C and U12C are selected with the F2-bar signal and multiplexers U13C and U14C are selected with the F2-bar signal complemented with U13B-6. The selected address is applied to the address inputs on RAMs U11E to U14E. The write multiplexer U12C also multiplexes the write pulse to U12C-11 and to the write inputs to the RAMs WE-bar on pin-10. When the write multiplexer U11C and U12C is selected, the write address is applied to RAMs U11E to U14E and the write pulse CPG is ap-

plied to the write input WE-bar of the RAMs. When the read multiplexer U13C and U14C is selected, the read address is applied to RAMs U11E to U14E and the write pin-10 WE bar is pulled up to select read operations.

The RAM input and output lines IO0 to IO3 are shared between outputting of information in the read mode and inputting of information in the write mode. Input information is selected with line buffers U12F to U14F, which apply input information obtained from the input bus to the RAM IO lines in the write mode and which are tristate-disabled to disconnect the input information on the input bus from the RAM IO lines in the read mode. Line buffers U12F to U14F are controlled with the F3-bar multiplexer control signal to connect the input bus to the RAM IO lines when the F2-bar signal enables the write address and the write pulse through multiplexers U15C and U16C and to disconnect the input bus from the RAM IO lines when the F2-bar signal enables the read address and disables the write address and write pulse. Hence, line buffers U12F to U14F are enabled when the RAM channel is in the write mode and are disabled when the RAM channel is in the read mode. As can be seen from the schematic, line buffers U12F to U14F apply the 8-intensity bits from image memory over the buffer input bus to the inputs of RAMs U11E and U12E and apply the weight addresses from the address generators over the buffer input bus to the inputs of RAMs U13B and U14E, with 2-spare bits presently unassigned.

Output information is multiplexed onto the buffer output buses; identified as the channel-I bus, the channel-II bus, the channel-III bus, and the weight bus. The 3-channel buses comprising the pixel intensities

from the 3-output line buffers are applied to the 3-channels of kernel registers. The weight bus, comprising the weight addresses of the selected channel, is applied to the single channel of weight registers U22A and U22B for accessing the weight RAM.

The 8-intensity lines from RAMs U11E and U12E are applied to all 3-channels through different multiplexers so that the intensity lines can be selected for one of the 3-output channels or for none of the 3-output channels under control of multiplexers U11D to U14D. Because each intensity parameter and each output channel has 8-bits, because each multiplexer U11D to U14D has 6-bits, and because the 74LS367 multiplexers can each control separately 4-bits and 2-bits, the 8-bits selected for one of 3-channels are partitioned between a pair of multiplexers. For example, the intensity bits from RAMs U11E and U12E are controlled with multiplexers U11D and U12D for channel-I, with multiplexers U12D and U13D for channel-II, and with multiplexers U13D and U14D for channel-III. The specific partitioning of intensity bits and multiplexers is shown in the schematic diagram. The multiplexing of the intensity bits onto the channel-I bus is controlled with the F3-bar multiplexer control signal to control all of multiplexer U11D and 2-bits of multiplexer U12D. The multiplexing of the intensity byte onto the channel-II bus is controlled with the F0-bar multiplexer control signal to control 4-bits of multiplexer U12D and 4-bits of multiplexer U13D. The multiplexing of the intensity byte onto the channel-III bus is controlled with the F1-bar multiplexer control signal to control 2-bits of multiplexer U13D and all 6-bits of multiplexer U14D. Consequently, multiplexers U11D to U14D multiplex the 8-intensity bits from RAMs U11E and U12E onto one of the 3-output channel buses

under control of the multiplexer control signals in accordance with the definitions shown in the BUFFER MEMORY MULTIPLEXER ASSIGNMENT TABLE.

The 6-weight address lines are applied to the weight bus under control of multiplexer U14E as output from RAMs U13E and U14E. This first RAM buffer line outputs to the weight bus under control of the F0-bar signal. Consequently, when the first line buffer is selected with the FU-bar signal to output the stored intensity onto the channel-II bus through multiplexers U12D and U13D, the weight addresses from RAMs U13E and U14E are applied to the weight bus through multiplexer U14B under control of the F0-bar signal.

The fourth line buffer will now be discussed with reference to Figs 6AE and 6AF. Four RAM circuits U15E to U18E are addressed through tristate multiplexers U15E to U18E. Multiplexers U15C and U16C select the write address from the write bus (or input bus) and multiplexers U17C and U18C select the read address from the read bus (or output bus) under control of the mode control signal F3-bar U12B-7 in accordance with the logic shown in the BUFFER MEMORY MULTIPLEXER ASSIGNMENT TABLE. Multiplexers U15C and U16C are selected with the F3-bar signal and multiplexers U17C and U18C are selected with the F3-bar signal complemented with U13B-8. The selected address is applied, to the address inputs on RAMs U15E to U18E. The write multiplexer U16C also multiplexes the write pulse to U16C-11 and to the write inputs to the RAMs WE-bar on pin-10. When the write multiplexer U15C and U16C is selected, the write address is applied to RAMs U15E to U18E and the write pulse CPG is applied to the write input WE-bar of the RAMs. When the

read multiplexer U17C and U18C is selected, the read address is applied-to RAMs U15E to U18E and the write pin-10 WE-bar is pulled Up to select read operations.

The RAM input and output lines IO0 to IO3 are shared between outputting of information in the read mode and inputting of information in the write mode. Input information is selected with line buffers U16F to U18F, which apply input information obtained from the input bus to the RAM IO lines in the write mode and which are tristate-disabled to disconnect the input information on the input bus from the RAM IO lines in the read mode. Line buffers U16F to U18F are controlled with the F3-bar multiplexer control signal to connect the input bus to the RAM IO lines when the F3-bar signal enables the write address and the write pulse through multiplexers U15C and U16C and to disconnect the input bus from the RAM IO lines when the F3-bar signal enables the read address and disables the write address and write pulse. Hence, line buffers U16F to U18F are enabled when the RAM channel is in the write mode and are disabled when the RAM channel is in the read mode. As can be seen from the schematic, line buffers U16F to U18F apply the 8-intensity bits from image memory over the buffer input bus to the inputs of RAMs U15E and U16E and apply the weight addresses from the address generators over the buffer input bus to the inputs of RAMs U15E and U16E, with 2-spare bits presently unassigned.

Output information is multiplexed onto the buffer output buses; identified as the channel-I bus, the channel-II bus the channel-III bus, and the weight bus. The 3-channel buses comprising the pixel intensities

from the 3-output line buffers are applied to the 3-channels of kernel registers. The weight bus, comprising the weight addresses of the selected channel, is applied to the single channel of weight registers U22A and U22B for accessing the weight RAM.

The 8-intensity lines from RAMs 1115E and U16E are applied to all 3-channels through different multiplexers so that the intensity lines can be selected for one of the 3-output channels or for none of the 3-output channels under control of multiplexers U15D to 818D. Because each intensity parameter and each output channel has 6-bits, because each multiplexer U15D to U18D has 6-bits, and because the 74LS367 multiplexers can each control separately 4-bits and 2-bits, the 8-bits selected for one of 3-channels are partitioned between a pair of multiplexers. For example, the intensity bits from RAMs U15E and U16E are controlled with multiplexers U15D and 1116D for channel-I, with multiplexers U16D and U17D for channel-II, and with multiplexers U17D and U18D for channel-III. The specific partitioning of intensity bits and multiplexers is shown in the schematic diagram. The multiplexing of the intensity bits onto the channel-I bus is controlled with the FO-bar multiplexer control signal to control all of multiplexer U15D and 2-bits of multiplexer U16D. The multiplexing of the intensity byte onto the channel-II bus is controlled with the F1-bar multiplexer control signal to control 4-bits of multiplexer U16D and 4-bits of multiplexer U17D. The multiplexing of the intensity byte onto the channel-III bus is controlled with the F2-bar multiplexer control signal to control 2-bits of multiplexer U16D and all 6-bits of multiplexer U17D. Consequently, multiplexers U15D to U18D multiplex the 8-intensity bits from RAMs U15E and U16E onto one of

the 3-output channel 'buses under control of the multiplexer control signals in accordance with the definitions shown in the BUFFER MEMORY MULTIPLEXER ASSIGNMENT TABLE.

The 6-weight address lines are applied to the weight bus under control of multiplexer U18B as output from RAMs U17E and U18E. This first RAM buffer line outputs-to the weight bus under control of the F1-bar signal. Consequently, when the first line buffer is selected with the F1-bar signal to output the stored intensity onto the channel-II bus through multiplexers U16D and 017D, the weight addresses from RAMs U17E and U18E are applied to the weight bus through multiplexer U18E under control of the F1-bar signal.

Kernel Logic

The kernel logic for spatial processing will now be discussed with reference to Fig 6AG. This kernel logic includes a 9-pixel kernel implemented with registers U19A to U19D, U20A to U20D, and U21A to U21D.

The 9-pixel kernel is composed of 3-adjacent buffered lines and 3-adjacent pixels on each line. The 3-lines are shifted out of the 3-line buffers into a 3-pixel register for each line buffer. Because each pixel is shown implemented as an 9-bit intensity word and because each register has 6 flip-flops, 1-1/3 register chips are needed to store a pixel word. Therefore, the 3-lines of 8-bit pixels are stored in 4-lines of 6-bit registers.

Referring to the pixel designation of Fig 5D, the following pixel storage is implemented with the kernel registers. Pixel-0 is stored in 6-bits of U19A and 2-bits of U19B. Pixel-1 is stored in 6-bits of U20A and 2-bits of U20B. Pixel-2 is stored in 6-bits of U21A and 2-bits of U21B. Pixel-7 is stored in 4-bits of U19B and 4-bits of

U19C. Pixel-8 is stored in 4-bits of U20B and 0-bits of U20C. Pixel-3 is stored in 4-bits of U21B and 4-bits of U21C. Pixel-6 is stored in 2-bits of 019C and 6-bits of U19D. Pixel-5 is stored in 2-bits of U20C and 6-bits of U20D). Pixel-4 is stored in 2-bits of U21C and 6-bits of U21D.

The above assignment of 8-bit pixels to 6-bit registers can be seen with reference to the output lines at the left of Fig 6AG. These output lines show the 8-lines grouped together for each of the 9-kernel pixels and show the source registers for these lines.

The 3-lines of pixels are scanned out of the line buffers onto the channel-I bus, channel-II bus, and channel III bus; as shown at the left hand side of Figs 6Z, 6AB, 6AD, and 6AF. The 3-channel scanline pixels are each implemented with 8-pixel lines being input to registers U19A to U19D with the above described partitioning for triple 8-bit pixel bytes loaded into quadruple 6-bit registers. The pixel information in registers U19A to U190 is shifted into registers U20A to U20D respectively and is also output to the spatial filter logic as pixel-0, pixel-7, and pixel-6 respectively of the kernel. The pixel information in registers U20A to U20D is shifted into registers U21A to U21D respectively and is output to the spatial filter logic as pixel-1, pixel-8, and pixel-5 respectively of the kernel. The pixel information in registers U21A to U21D is output to the spatial filter logic as pixel-2, pixel-3, and pixel-4 respectively of the kernel. This shift register operation is performed under control of the CPE clock U8B-4 which clocks the information out of the line buffers, into the kernel registers, and through the kernel registers to provide a 9-pixel kernel in parallel to the spatial filter logic.

In a non-filtered implementation, the center pixel is provided to the video DACs on the rear end board to display the center pixel without spatial filtering. The center pixel is shown output on cable C-4 lines 22, 24, 26, 28, 30, 32, 34, and 36.

In a spatial filtering implementation, the output of the 9-pixel kernel is provided in parallel to the sum-of-the-products logic that performs spatial filtering. The output of the sum-of-the-products processing is provided to the ideo DACs on the rear-end board to display the spatially filtered pixel. The 9-pixel kernel is shown output in parallel through the 72-lines. (9-pixels by 8-bits per pixel) at the left hand side of Fig 6AG.

Weight Logic

The weight logic will now be discussed with reference to Fig 6AH. The weight logic is implemented with registers U22A and U22B; decoders U22C and U22D; RAMs U21E to U23E; and multiplexers U23C and U23D.

The weight addresses stored in the line buffers are output to the weight RAMs U21E to U23E for accessing of the weights associated therewith. In one configuration, the weights to be accessed are associated with the center pixel in the kernel. Therefore, the weight addresses from the line buffer are shown delayed 2-clock periods with registers U22A and U22B so that they are available as addresses to the weight RAM when the pixel with which they are associated is in the center pixel position, pixel-8 position, of the kernel. Multiplexers U22C and U22D provide for addressing of weight RAM U21E to U23E from two sources, for reading and for writing.

During the run mode, addresses from the line buffers are selected with multiplexers U22C and U22D for ac-

cessing weights stored in weight RAMs U21E to U23E. During the load mode, the computer can generate weight addresses through the output port for writing weights into the weight RAMs; where the addresses selected with multiplexers U22C and U22D and are applied to weight RAMs U21E to U23E.

The RAM IO lines IO0 to IO3 are used for both input and output of data, controlled with the WE-bar pins. In the run mode, the W2-bar and W3-bar signals to the WE-bar pins are high, selecting reading from the weight RAM for outputting on the RAM I0 lines to the spatial filter logic. In the load mode, the W2-bar and W3-bar signals can be controlled by the computer to be low, selecting writing into the weight RAM from the computer output signals through multiplexers U23C and U23D. The weight addresses stored in register U22B are output to multiplexers U22C and U22D for accessing of weights from the weight RAM when selected by the run mode signal to multiplexers U22C and U22D. The weight addresses from the computer output port are applied to multiplexers U22C and U22D for storing of weights in the weight RAM when selected by the load mode signal to multiplexers U22C and U22D.

The weight bus communicates the weight address bits from the line buffers to weight register U22A; where the weight address is shifted into the weight registers to address the weight RAMs in a manner similar to the pixel intensities being shifted into the kernel registers for spatial filtering, as discussed above. The weight addresses are composed of the Y-weight address YW0B, YW1B, and YW2B and the X-weight address XW0B, XW1B, and XW2B shifted into register 022A.

Multiplexers U22C and U22D select the address for the weight RAMs, comprising the buffered weight addresses from register U22B in the run mode and the computer generated weight addresses XW0, XW1, XW2, YW0, YW1, and YW2 in the load mode when the computer is loading the weight RAMs. The multiplexer source information is selected with the load/run signal from the computer. The addresses from the multiplexers are used to address the weight RAMs to access the appropriate weights as a function of the weight addresses from the line buffers in the run mode and to store the computer generated weights as a function of the computer generated weight addresses in the load mode when the W2-bar or W3-bar signals select writing into the weight RAMs. The data to be loaded into the weight RAMs in the load mode is input to tri state buffers U23C and U23D and is controlled to be applied to the RAM IO lines with control signal C2-34 to the buffer circuits. When the input data is applied to the RAM IO lines, the input data can be stored in the RAMs under control of the W2-bar signal or the W3-bar signal to RAMs U21E to U23E. When the input data is not applied to the RAM IO lines through U23C and U23D, the weights stored in the RAMs are output on the RAM IO lines to the spatial filter.

REAR-END BOARD

The rear-end board interfaces the system to a CRT monitor and provides synchronization and clock signals for the CRT monitor and for the rest of the system. The rear-end board also performs auxiliary functions, such as converting analog joystick signals to digital form for control of a display processor. The rear-end board is

shown in Figs 6S to 6V in detailed schematic diagram form.

A clock pulse generator 630A is implemented with a pair of inverters, an 18.432-MHz (herein referred to as 18-MHz for convenience) crystal, resistors, and capacitors as shown in Fig 6T to generate a square wave signal from inverter 630B pin-12. A counter circuit (74LS163N) is clocked from the inverted 18-MHz signal to pin-2 through inverter 74LS04 pin 2 for counting down the 18-MHz signal to about a 9-MHz clock signal for the display processor output from pin-14 and about a 2-mHz clock signal to the sync generator circuit MM5321 from pin-12. A group of 4-switches with pull-up resistors are connected to the preload inputs of the counter on pins 3 to 6 to preload a selected amount for implementing count periods other than binary numbers.

A synchronization signal generator is implemented with a National Semiconductor MM5321component. The MM5321 is connected in a usual fashion, such as described in the specification sheets and shown in Fig 6T. Switches D.C., A.R, and H.R. select MM532 modes of operation.

The MM5321 horizontal drive signal is output from pin-15 and is used to blank the digital to analog converters (DACs) and is output through an 8T98-9 inverter H-DRIVE for generating the horizontal sync signal or line sync signal CLS to the digital logic boards. The horizontal drive signal is also output to flip-flop U1-9, which is used to experiment with horizontal blanking HB signals.

The MM5321 vertical drive signal is output from pin-11 and is used to generate vertical blanking signals through an 8T97-5 to vertical blanking flip-flops U2, generating vertical blanking signal VB which is used to

blank the video DACs. The vertical blanking signal VB U2-9 is buffered with 8T97-11 through cable C4-2 to apply the vertical blanking signal to the digital logic as the CFS signal.

The MM5321 composite sync signal is output from pin-16 and is used as the composite sync signal to the CRT monitor, buffered with an 3 and an 8T98-3 for complement signals.

The MM5321 blanking clock signal is output from pin-14 and is used to clock the vertical blanking flip-flops. U2 and the horizontal blanking flip-flops U1-9 HB through an inverter 8T98-7.

The MM5321 interlace control signal is output from pin-9 and is used to control flip-flop U1-5 FLD-bar to generate the field-1-bar signal on cable C4-12 to the control logic board.

Joystick input circuits are shown in Figs 6U and 6V. Fig 6U provides the-control circuits for the joystick analog to digital converters (ADCs) and Fig 6V shows the ADCs. These ADCs are input to the computer through the control logic board to provide operator control of display processing.

The joysticks utilized in this configuration are Apple-2 Compatible Joysticks named Computer Compatible Joystick. They are analog joysticks having analog potentiometers for analog control. The joystick signals are input through plugs PJ1 and PJ2 at pin-6 and pin-7 for connection to the scaling amplifiers and ADCs shown in Fig 6V. The ADCs are controlled to start the conversion with the frame sync transition of the frame sync signal by shifting the frame sync signal through flip-flops U9A-5 and U9A-9 and detecting the condition of U9A-5 being

in the 0-state and U9A-9 being in the 1-state with AND-gate U12-3 to generate a 1-clock period start convert pulse to the ADCs. The ADCs will start the conversion in response to this start convert pulse and will latch up the converted digital number for input to the computer under program control.

The two computer signals SEL0 and SEL1 are received from the computer through the control logic board to select one of four ADC numbers for input to the computer. These signals are inverted with U13-7 and U13-9. The inverted and non-inverted SEL0 and SEL1 signals are decoded with U11-3 for ADC 1-selection with signal S1, ADC-2 selection with signal S2, ADC-3 selection with signal S3, and ADC-4 selection with signal S4. Inverters U10 and U13 receive 8 signals from the ADCs, shown in Fig 6V, and buffers these 8-signals to drive the cable for input to the computer through the control logic board.

Consequently, the computer under program control generates select signals SEL0 and SEL1 and reads the 8-bit number from the selected ADC. In one implementation, the computer under program control generates four sequential select signal codes on lines SEL0 and SEL1 to address the four ADCs in sequence and inputs the selected ADCs output number for processing under program control.

The 4-ADCs and associated scaling amplifiers are shown in Fig 6V. The ADCs are implemented with the well known ADC0800 components, such as manufactured by National Semiconductor. The scaling amplifiers are implemented with the well known LF356 amplifiers. Each of the 4-joystick inputs from plugs PJ1 and PJ2 (Fig 6U) are shown connected to a different ADC chan-

nel through a scaling amplifier U1, U2, U5, and U6 (Fig 6V). The scaling amplifiers are connected in a conventional manner with resistor and capacitor networks to scale the joystick signals. Each scaling amplifier has its output on pin-6 connected to the input of its related ADC on pin-12. The ADCs convert the analog signal input at pin-12 in response to the start convert signal to pin-6 and latch the converted number in an internal register. The internal register is implemented with a tristate output controlled by the output enable signal to pin-7. The corresponding output lines of each ADC are connected together to form an 8-bit bus D0 to D7 which is routed to buffer amplifiers. U10 and U13 (Fig 6U). Consequently, when one of the ADCs is tristate-enabled with one of the decoded select signals. S1 to S4 (Fig 6U) input to pin-7 of the ADCs (Fig 6V), the number converted by that ADC is applied to the 8-bit data bus for communication to the computer.

One channel of video DAC is shown in Fig 6S. Each of the three channels are implemented with similar signals, except that the green channel having 3-bits is connected to data bits D5 to D7 and the red and blue channels having 2-bits are connected to data bits D6 and D7. These video DACs are high speed DACs for converting intensity signals from digital signal form, as generated by the display processor, to analog signal form for exciting a CRT monitor. Three video DACs are used to convert three video signals; the red video signal, the blue video signal, and the green video signal; to generate the RGB signals to the CRT monitor. The video DACs can be implemented with the TDC1016 DACs manufactured by TRW. The connections for this DAC are shown .in the VIDEO DAC CONNECTION TABLE provided herein. The D9 and D10 data pins are connected to

ground. The digital red and blue signals having 2-bits resolution are connected to the D7 and D8 data pins. The digital green signal having 3-bits resolution is connected to the D6 and D8 data pins. The other data pins are connected to ground.

Buffer amplifiers are implemented with the well known LM359 buffer amplifier, where the buffer amplifier connections are shown in Fig 6S. The output of each buffer amplifier excites one of the red, green, or blue inputs to the CRT monitor.

No. 10-1219

In the Supreme Court of the United States

DAVID J. KAPPOS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR, UNITED STATES PATENT AND TRADEMARK OFFICE, PETITIONER

v.

GILBERT P. HYATT

ON WRIT OF CERTIORARI TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

VOLUME 2
JOINT APPENDIX

DONALD B. VERRILLI, JR.
Solicitor General
Department of Justice
Washington, D.C. 20530-0001
SupremeCtBriefs@usdoj.gov
(202) 514-2217

Counsel of Record for Petitioner

AARON M. PANNER*
Kellogg, Huber, Hansen, Todd, Evans & Figel, P.L.L.C.
1615 M Street, N.W.
Suite 400
Washington, D.C. 20036
apanner@khhte.com
(202) 723-6871

GREGORY L. ROTH
5712 Parkwest Circle
La Palma, CA 90623
(714) 723-6871

* *Counsel of Record for Respondent*

PETITION FOR A WRIT OF CERTIORARI FILED: APR. 7, 2011
CERTIORARI GRANTED: JUNE 27, 2011

TABLE OF CONTENTS

Page

VOLUME 1

Court of appeals docket entries 1
District court docket entries 4
In re Application of Gilbert P. Hyatt:
Specification (June 6, 1995) 9

VOLUME 2

Specification Diagrams (June 6, 1995) 146

VOLUME 3

Amendment Under 37 C.F.R. § 1.111 (Oct. 15, 1996) 263
Final Office Action (July 30, 1997) 365
Appeal Brief (Sept. 2, 1998) 393

VOLUME 4

Examiner's Answer (Aug. 13, 1999) 541
Reply Brief Under 37 C.F.R. § 1.193(b) (July 31, 2000) 588
Request for Rehearing (Sept. 30, 2002) 670

CIRCUIT SPECIFICATIONS

The circuits used in the experimental system are generally commercially available circuits that are well known and that are described in widely distributed specification sheets and component catalogs. A list of these specification sheets and catalogs is provided hereinafter and the materials referenced therein are incorporated herein by reference. For example, the 74LS00, 74ALS00, and 74AS00 specifications are set forth in the referenced Texas Instruments and Motorola catalogs and the Intel 8216 bus interface and the Intel 2149 RAM specifications are set forth in the referenced Intel catalogs; which are herein incorporated by reference.

1. Texas Instruments, ALS/AS Logic Circuits Data Book, 198[illegible]
2. Texas Instruments, The TTL Data Book, Volume 3, 1984.
3. Texas Instruments, The TTL Pocket Data Book, 1983.
4. Intel, Component Data Catalog, 1981.
5. Intel, Memory Components Handbook, 1984.
6. Motorola, Schottky TTL Databook, 1981.

Various circuits used in the experimental system are described i the following list of component specifications, which are herein incorporated by reference.

1. TRW, LSI D/A Converters, TDC1016J-8/9/10.
2. TRW, Monolithic Video D/A Converters; TDC1016J-8, TDC0106J-9, TDC1016J-10; 1979.
3. Texas Instruments, TMS-4016, 2048-Word By 8-Bit Static RAM.
4. National Semiconductor, ADC0800 8-Bit A/D Converter.

COMPUTER PORT TABLE

VIDEO DAC CONNECTION TABLE

1	NC	NO CONNECTION
2	VEE	-5VDC
3	COMP	6.8 MICROFARAD CAPACITOR TO -5VDC
4	REF	-1V
5	AGND	GROUND
6	AGND	GROUND
7	OUT	VIDEO OUTPUT TO BUFFER AMPLIFIER
8	GND	GROUND
9	VCC	+5VDC
10	DGND	GROUND
11	MDIS	BLANKING SIGNAL
12	CLK	CLOCK
13	$\overline{\text{CLK}}$	
14	$\overline{\text{MDIS}}$	
15	$\overline{\text{D1}}$	MOST SIGNIFICANT BIT, COMPLEMENT
16	D1	MOST SIGNIFICANT BIT, UNCOMPLEMENT
17	N2C	+5VDC
18	$\overline{\text{D2}}$	DATA BIT 2, COMPLEMENT
19	D2	DATA BIT 2, UNCOMPLEMENT
20	NFH	GROUND
21	NFL	GROUND
22	$\overline{\text{D3}}$	DATA BIT 3, COMPLEMENT - GROUND
23	D3	DATA BIT 3, UNCOMPLEMENT - GROUND
24	$\overline{\text{D4}}$	DATA BIT 4, COMPLEMENT - GROUND
25	D4	DATA BIT 4, UNCOMPLEMENT - GROUND
26	$\overline{\text{D5}}$	DATA BIT 5, COMPLEMENT - GROUND
27	D5	DATA BIT 5, UNCOMPLEMENT - RED, BLUE GROUND; GREEN SIGN
28	$\overline{\text{D6}}$	DATA BIT 6, COMPLEMENT - GROUND
29	D6	DATA BIT 6, UNCOMPLEMENT - RED, GREEN, BLUE SIGNAL
30	$\overline{\text{D7}}$	DATA BIT 7, COMPLEMENT - GROUND
31	D7	DATA BIT 7, UNCOMPLEMENT - RED, GREEN, BLUE SIGNAL
32	$\overline{\text{D8}}$	DATA BIT 8, COMPLEMENT - GROUND
33	D8	DATA BIT 8, UNCOMPLEMENT - GROUND
34	$\overline{\text{D9}}$	DATA BIT 9, COMPLEMENT - GROUND
35	D9	DATA BIT 9, UNCOMPLEMENT
36	$\overline{\text{D10}}$	LEAST SIGNIFICANT BIT, COMPLEMENT
37	D10	LEAST SIGNIFICANT BIT, UNCOMPLEMENT
38	NC	NO CONNECTION
39	NC	NO CONNECTION
40	NC	NO CONNECTION

[illegible]
10/17/4

6. Signetics, Hex Buffers/Inverters; 8T95, 96, 97, 98.

7. Mitsubishi; M58725P,S;P-15,S-15; 16384-BIT (2048-word by 8-bit static RAM.

PORT-A CONTROL PORT

BIT	NAME	FUNCTION	NOTES
0	DOA0	TEST PULSE-1	
1	DOA1	JOYSTICK SELECT-1	
2	DOA2	JOYSTICK SELECT-0	
3	DOA3		
4	DOA4	UNBLANK	HIGH IS UNBLANK
5	DOA5	SEQUENTIAL-LOAD	SEQUENTIAL LOAD
6	DOA6	LOAD-BAR/RUN	BRACKETED BY FR
7	DOA7	DATA STROBE	BRACKETED BY PB
0	DIA0	FRAME SYNC	VERTICAL FIELD
1	DIA1		
2	DIA2	LINE SYNC	HORIZONTAL LINE
3	DIA3		
4	DIA4	FRAME-1	
5	DIA5		
6	DIA6		
7	DIA7		

SEQUENTIAL CONTROL OF IMAGE LOADING

(1) RESET DOA5
(2) LOAD X+Y START ADDRESSES, (PIXEL ADDRESS
(3) LOAD SLOPES TIMES 256
(4) SET DOA5
(5) GENERATE A SEQUENCE OF STROBED DATA OUTPU
(6) ADDRESS COUNTER WILL AUTOMATICALLY ADVANC
(7) DOA5 must be set before strobing data int
independent of whether one or a sequence
to be generated.

PORT-B ADDRESS/DATA PORT

BIT	NAME	FUNCTION	NOTES
0	DOB0	LSB	
1	DOB1	↕	
2	DOB2	↕	
3	DOB3	↕	
4	DOB4	↕	
5	DOB5	↕	
6	DOB6	↕	
7	DOB7	MSB	
0	DIB0	LSB	
1	DIB1	↕	
2	DIB2	↕	
3	DIB3	↕	
4	DIB4	↕	
5	DIB5	↕	
6	DIB6	↕	
7	DIB7	MSB	

PORT-C DESTINATION SELECT PORT

BIT	NAME	FUNCTION	NOTES
0	DOC0	LSB	
1	DOC1	|	
2	DOC2	|	
3	DOC3	|	
4	DOC4	|	
5	DOC5	|	
6	DOC6	|	
7	DOC7	MSB	
0	DIC0	LSB	
1	DIC1	|	
2	DIC2	|	
3	DIC3	|	
4	DIC4	|	
5	DIC5	|	
6	DIC6	|	
7	DIC7	MSB	

DESTINATION SELECT ASSIGNMENTS

P	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	0	0									
1	0	0	0	0	0	0	0	1									
2	0	0	0	0	0	0	1	0									
	▼																
127	0	0	0	0	1	1	1	1									
128	0	0	0	1	0	0	0	0									

129	0	0	0	1	0	0	0	1	
130	0	0	0	1	0	0	1	0	
	⋮								
240	1	1	1	1	0	0	0	0	XR-DELTA LSH
241	1	1	1	1	0	0	0	1	YR-DELTA LSH
242	1	1	1	1	0	0	1	0	XP-DELTA MSH
243	1	1	1	1	0	0	1	1	XP-DELTA LSH
244	1	1	1	1	0	1	0	0	YP-DELTA LSH
245	1	1	1	1	0	1	0	1	YP-DELTA MSH
246	1	1	1	1	0	1	1	0	XR-ADDRESS MSH
247	1	1	1	1	0	1	1	1	XR-ADDRESS LSH
248	1	1	1	1	1	0	0	0	XR-DELTA MSH
249	1	1	1	1	1	0	0	1	YR-ADDRESS MSH
250	1	1	1	1	1	0	1	0	YR-ADDRESS LSH
251	1	1	1	1	1	0	1	1	YR-DELTA MSH
252	1	1	1	1	1	1	0	0	DATA
253	1	1	1	1	1	1	0	1	WEIGHTS, LS BYTE (W2)
254	1	1	1	1	1	1	1	0	WEIGHTS, MS NIBBLE(W
255	1	1	1	1	1	1	1	1	SPARE

NOTES

1. Frame sync and CP-bar must be synchronized
2. Gated clock.
3. First line sync per frame is under the frame sync envelope. Therefore, U20D-1 generates second line sync as first pulse.
4. First line sync under frame sync envelope loads pixel registers.

CXPSM	XP-DELTA MSB CLOCK
CXPSL	XP-DELTA LSB CLOCK
CYPSM	YP-DELTA MSB CLOCK
CYPSL	YP-DELTA LSB CLOCK
CXRSM	XR-DELTA MSB CLOCK
CXRSL	XR-DELTA LSB CLOCK
CYRSM	YR-DELTA MSB CLOCK
CYRSL	YR-DELTA LSB CLOCK
CD	DATA STROBE
CXRM	XR-ADDRESS MSH CLOCK
CXRL	XR-ADDRESS LSH CLOCK
CXPM	XP-ADDRESS MSH CLOCK
CXPL	XP-ADDRESS LSH CLOCK
CYRM	YR-ADDRESS MSH CLOCK
CYRL	YR-ADDRESS LSH CLOCK
CYPM	YP-ADDRESS MSH CLOCK
CYPL	YP-ADDRESS LSH CLOCK

CABLE CONNECTION TABLE

CABLE-I BM1,2/BL1 (C1)

PIN	SIGNAL	SIGNAL DESCRIPTION	SOURCE	DESTINATION
1	GROUND	GROUND		
2	YA0	MEMORY ADDRESS, BIT-Y0	BL1-U9E-10	BM1,2-U19B-1
3	GROUND	GROUND		
4	YA1	MEMORY ADDRESS, BIT-Y1	BL1-U9E-12	BM1,2-U19B-2
5	GROUND	GROUND		
6	YA2	MEMORY ADDRESS, BIT-Y2	BL1-U9E-15	BM1,2-U19B-3
7	GROUND	GROUND		
8	YA3	MEMORY ADDRESS, BIT-Y3	BL1-U8E-2	BM1,2-U19A-2
9	GROUND	GROUND		
10	YA4	MEMORY ADDRESS, BIT-Y4	BL1-U8E-5	BM1,2-U19A-4
11	GROUND	GROUND		
12	YA5	MEMORY ADDRESS, BIT-Y5	BL1-U8E-7	BM1,2-U19A-6
13	GROUND	GROUND		
14	YA6	MEMORY ADDRESS, BIT-Y6	BL1-U8E-10	BM1,2-U19A-10
15	GROUND	GROUND		
16	YA7	MEMORY ADDRESS, BIT-Y7	BL1-U8E-12	BM1,2-U19A-12
17	GROUND	GROUND		
18	YA8	MEMORY ADDRESS, BIT-Y8	BL1-U8E-15	BM1,2-U19A-14
19	GROUND	GROUND		
20	XA0	MEMORY ADDRESS, BIT-X0	BL1-U9D-10	BM1,2-U19C-1
21	GROUND	GROUND		
22	XA1	MEMORY ADDRESS, BIT-X1	BL1-U9D-12	BM1,2-U19C-2
23	GROUND	GROUND		
24	XA2	MEMORY ADDRESS, BIT-X2	BL1-U9D-15	BM1,2-U19C-3
25	GROUND	GROUND		

26	XA3	MEMORY	ADDRESS, BIT-X3 (BM2)	BL1-U8D-2	BM1,2-U19B-6
27	GROUND	GROUND			
28	XA3-BAR	MEMORY	ADDRESS, BIT-X3-BAR (BM1)	BL1-U18D-4	BM1,2-U19B-6
29	GROUND	GROUND			
30	XA4	MEMORY	ADDRESS, BIT-X4	BL1-U8D-5	BM1,2-U19D-4
31	GROUND	GROUND			
32	XA5	MEMORY	ADDRESS, BIT-X5	BL1-U8D-7	BM1,2-U19D-6
33	GROUND	GROUND			
34	XA6	MEMORY	ADDRESS, BIT-X6	BL1-U8D-10	BM1,2-U19D-10
35	GROUND	GROUND			
36	XA7	MEMORY	ADDRESS, BIT-X7	BL1-U8D-12	BM1,2-U19D-12
37	GROUND	GROUND			
38	XA8	MEMORY	ADDRESS, BIT-X8	BL1-U8D-15	BM1,2-U19D-14
39	GROUND	GROUND			
40	W1-BAR	MEMORY	READ/WRITE (LOW => WRITE)	BL1-U22C-11	BM1,2-U19E-4
41	GROUND	GROUND			
42					
43	GROUND	GROUND			
44					
45	GROUND	GROUND			
46					
47	GROUND	GROUND			
48					
49	GROUND	GROUND			
50					

CABLE-II BM1,2/BL1/BB1 (C2)

PIN	SIGNAL	SIGNAL	DESCRIPTION	SOURCE	DESTINATION
1	GROUND	GROUND			
2	MI0	MEMORY	DATA INPUT, BIT-0 (PB0)	BL1-C6-9	BM1,2-U17A,B,C,D-4
3	GROUND	GROUND			
4	MI1	MEMORY	DATA INPUT, BIT-1 (PB1)	BL1-C6-22	BM1,2-U17A,B,C,D-7
5	GROUND	GROUND			
6	MI2	MEMORY	DATA INPUT, BIT-2 (PB2)	BL1-C6-10	BM1,2-U17A,B,C,D-9
7	GROUND	GROUND			
8	MI3	MEMORY	DATA INPUT, BIT-3 (PB3)	BL1-C6-23	BM1,2-U17A,B,C,D-12
9	GROUND	GROUND			
10	MI4	MEMORY	DATA INPUT, BIT-4 (PB4)	BL1-C6-11	BM1,2-U18A,B,C,D-4
11	GROUND	GROUND			
12	MI5	MEMORY	DATA INPUT, BIT-5 (PB5)	BL1-C6-24	BM1,2-U18A,B,C,D-7
13	GROUND	GROUND			
14	MI6	MEMORY	DATA INPUT, BIT-6 (PB6)	BL1-C6-12	BM1,2-U18A,B,C,D-9
15	GROUND	GROUND			
16	MI7	MEMORY	DATA INPUT, BIT-7 (PB7)	BL1-C6-25	BM1,2-U18A,B,C,D-12
17	GROUND	GROUND			
18	MO0	MEMORY	DATA OUTPUT, BIT-0 (GREEN)	BM1,2-U17A,B,C,D-2	BB1-U...;C4-22
19	GROUND	GROUND			
20	MO1	MEMORY	DATA OUTPUT, BIT-1 (GREEN)	BM1,2-U17A,B,C,D-5	BB1-U...;C4-24
21	GROUND	GROUND			
22	MO2	MEMORY	DATA OUTPUT, BIT-2 (GREEN)	BM1,2-U17A,B,C,D-11	BB1-U...;C4-26
23	GROUND	GROUND			
24	MO3	MEMORY	DATA OUTPUT, BIT-3 (RED)	BM1,2-U17A,B,C,D-14	BB1-U...;C4-28
25	GROUND	GROUND			

26	MO4	MEMORY DATA OUTPUT, BIT-4 (RED)	BM1,2-U18A,B,C,D-2	BB1	;C4-30
27	GROUND	GROUND			
28	MO5	MEMORY DATA OUTPUT, BIT-5 (BLUE)	BM1,2-U18A,B,C,D-5	BB1	;C4-32
29	GROUND	GROUND			
30	MO6	MEMORY DATA OUTPUT, BIT-6 (BLUE)	BM1,2-U18A,B,C,D-11	BB1	;C4-34
31	GROUND	GROUND			
32	MO7	MEMORY DATA OUTPUT, BIT-7 (SPARE)	BM1,2-U18A,B,C,D-14	BB1	;C4-36
33	GROUND	GROUND			
34	DIEW-BAR	MEMORY READ/WRITE	BL1-U21E-6	BM1,2-U18A,B,C,D-15 BM1,2-U17A,B,C,D-15 U19C-6 BB1-U23C-1,15 BB1-U23D-1,15	
35	GROUND	GROUND			
36					
37	GROUND	GROUND			
38					
39	GROUND	GROUND			
40					
41	GROUND	GROUND			
42					
43	GROUND	GROUND			
44					
45	GROUND	GROUND			
46					
47	GROUND	GROUND			
48					
49	GROUND	GROUND			
50					

CABLE-III BR1/BL1/BB1 (C3)

PIN	SIGNAL	SIGNAL DESCRIPTION	SOURCE	DESTINATION
1	GROUND	GROUND		
2	YW0	WEIGHT ADDRESS		BB1-U22C-10
3	GROUND	GROUND		
4	YW1	WEIGHT ADDRESS		BB1-U22C-13
5	GROUND	GROUND		
6	YW2	WEIGHT ADDRESS		BB1-U22C-6
7	GROUND	GROUND		
8	XW0	WEIGHT ADDRESS		BB1-U22C-3
9	GROUND	GROUND		
10	XW1	WEIGHT ADDRESS		BB1-U22D-3
11	GROUND	GROUND		
12	XW2	WEIGHT ADDRESS		BB1-U22D-6
13	GROUND	GROUND		
14	YA0	WEIGHT ADDRESS		BB1-U22D-13
15	GROUND	GROUND		
16	YA1	WEIGHT ADDRESS		BB1-U22D-10
17	GROUND	GROUND		
18	DQA6			BB1-U7B-4
19	GROUND	GROUND		
20				
21	GROUND	GROUND		
22	CPG	GATED CLOCK PULSE	BL1-U21D-8	BB1-U7A,U6A,U5A-2
23	GROUND	GROUND		
24				
25	GROUND	GROUND		

```
26
27  GROUND   GROUND
28
29  GROUND   GROUND
30
31  GROUND   GROUND
32
33  GROUND   GROUND
34
35  GROUND   GROUND
36
37  GROUND   GROUND
38
39  GROUND   GROUND
40
41  GROUND   GROUND
42
43  GROUND   GROUND
44
45  GROUND   GROUND
46
47  GROUND   GROUND
48  W2-BAR   WEIGHT RAM READ/WRITE(LOW=>WRITE) BL1-U22C-6    BB1-U21E,U22E-10
49  GROUND   GROUND
50  W3-BAR   WEIGHT RAM READ/WRITE(LOW=>WRITE) BL1-U22C-8    BB1-U23E-10
```

CABLE-IV BR1/BL1/BB1 (C4)

PIN	SIGNAL	SIGNAL DESCRIPTION	SOURCE	DESTINATION
1	GROUND	GROUND		
2	FRAME SYNC (CFS)		BR1	BL1-U22E-11, C5-2
3	GROUND	GROUND		
4	LINE SYNC (CLS)		BR1	BL1-U22E-13, C5-3
5	GROUND	GROUND		
6	INPUT PIXEL CLOCK EARLY (CPE-BAR)		BR1	BL1-U21E-1
7	GROUND	GROUND		
8	DAC PIXEL CLOCK (CPD) (CHANGE TO BF1-10MHZ)		BB1-U8B-6	BR1-
9	GROUND	GROUND		
10	OUTPUT PIXEL CLOCK (CPO)		BR1	BB1
11	GROUND	GROUND		
12	FIELD-1 (F1)		BR1	C5-4
13	GROUND	GROUND		
14			BR1	C5-5
15	GROUND	GROUND		
16	SEL0	ADC SELECT LSB DOA2	C5-10	BR1-U11,U13
17	GROUND	GROUND		
18	SEL1	ADC SELECT MSB DOA1	C5-22	BR1-U11,U13
19	GROUND	GROUND		
20	DJ7	JOYSTICK COMMAND MSB	BR1-U10-3	C6-18
21	GROUND	GROUND		
22	MOOR	BUFFER OUTPUT TO CRT DACS (GREEN)	BB1-U19B-7	BR-U
23	GROUND	GROUND		
24	MO1R	BUFFER OUTPUT TO CRT DACS (GREEN)	BB1-U19B-10	BR-U
25	GROUND	GROUND		

26	MO2R	BUFFER OUTPUT TO CRT DACS (GREEN)	BB1-U19B-12	BR-U
27	GROUND	GROUND		
28	MO3R	BUFFER OUTPUT TO CRT DACS (RED)	BB1-U19B-15	BR-U
29	GROUND	GROUND		
30	MO4R	BUFFER OUTPUT TO CRT DACS (RED)	BB1-U19C-2	BR-U
31	GROUND	GROUND		
32	MO5R	BUFFER OUTPUT TO CRT DACS (BLUE)	BB1-U19C-5	BR-U
33	GROUND	GROUND		
34	MO6R	BUFFER OUTPUT TO CRT DACS (BLUE)	BB1-U19C-7	BR-U
35	GROUND	GROUND		
36	MO7R	BUFFER OUTPUT TO CRT DACS (SPARE)	BB1-U19C-10	
37	GROUND	GROUND		
38	DJ6	JOYSTICK COMMAND	BR1-U10-5	C6-5
39	GROUND	GROUND		
40	DJ5	JOYSTICK COMMAND	BR1-U10-7	C6-17
41	GROUND	GROUND		
42	DJ4	JOYSTICK COMMAND	BR1-U10-9	C6-4
43	GROUND	GROUND		
44	DJ3	JOYSTICK COMMAND	BR1-U10-11	C6-16
45	GROUND	GROUND		
46	DJ2	JOYSTICK COMMAND	BR1-U10-13	C6-3
47	GROUND	GROUND		
48	DJ1	JOYSTICK COMMAND	BR1-U13-13	C6-15
49	GROUND	GROUND		
50	DJ0	JOYSTICK COMMAND	BR1-U13-11	C6-2

CABLE-V BL1/COMPUTER PORT-A CONTROL (C5)

PIN	SIGNAL	SIGNAL DESCRIPTION	SOURCE	DESTINATION	
1	-12V				
2	DIA0	COMPUTER DATA INPUT, FRAME SYNC	C4-2	COMPUTER	
3	DIA2	COMPUTER DATA INPUT, LINE SYNC	C4-4	COMPUTER	
4	DIA4	COMPUTER DATA INPUT, FIELD 1-BAR	C4-12	COMPUTER	
5	DIA6	COMPUTER DATA INPUT		COMPUTER	
6					
7	+5V				
8					
9	DOA0	COMPUTER DATA OUTPUT, TEST PULSE-1	COMPUTER		
10	DOA2	COMPUTER DATA OUTPUT, JOYSTICK SEL.-0	COMPUTER	C4-16	
11	DOA4	COMPUTER DATA OUTPUT, TEST PULSE-16	COMPUTER		
12	DOA6	COMPUTER DATA OUTPUT, LOAD-BAR/RUN	COMPUTER	BL1-U16D-5	
13	+12V				
14	GROUND	GROUND			
15	DIA1	COMPUTER DATA INPUT		COMPUTER	
16	DIA3	COMPUTER DATA INPUT		COMPUTER	
17	DIA5	COMPUTER DATA INPUT		COMPUTER	
18	DIA7	COMPUTER DATA INPUT		COMPUTER	
19	GROUND	GROUND			
20	GROUND	GROUND			
21					
22	DOA1	COMPUTER DATA OUTPUT, JOYSTICK SEL.-1	COMPUTER	C4-18	
23	DOA3	COMPUTER DATA OUTPUT, UNBLANK	COMPUTER	C4-	
24	DOA5	COMMAND SEQ. LOAD OF IMAGE MEMORY	COMPUTER	BL1-U18E-12	
25	DOA7	OUTPUT DATA STROBE	COMPUTER	BL1-U22B-2	
26					

CABLE-VI BL1/COMPUTER PORT-B ADDRESS/DATA (C6)

PIN	SIGNAL	SIGNAL DESCRIPTION		SOURCE	DESTINATION
1	-12V				
2	DIB0	COMPUTER DATA INPUT,	JOYSTICK	C4-50	COMPUTER
3	DIB2	COMPUTER DATA INPUT,	JOYSTICK	C4-46	COMPUTER
4	DIB4	COMPUTER DATA INPUT,	JOYSTICK	C4-42	COMPUTER
5	DIB6	COMPUTER DATA INPUT,	JOYSTICK	C4-38	COMPUTER
6					
7	+5V				
8					
9	DOB0	COMPUTER DATA OUTPUT		COMPUTER	C2-2; U17C-3
10	DOB2	COMPUTER DATA OUTPUT		COMPUTER	C2-6; U17C-6
11	DOB4	COMPUTER DATA OUTPUT		COMPUTER	C2-10; U17C-13
12	DOB6	COMPUTER DATA OUTPUT		COMPUTER	C2-14
13	+12V				
14	GROUND	GROUND			
15	DIB1	COMPUTER DATA INPUT,	JOYSTICK	C4-48	COMPUTER
16	DIB3	COMPUTER DATA INPUT,	JOYSTICK	C4-44	COMPUTER
17	DIB5	COMPUTER DATA INPUT,	JOYSTICK	C4-40	COMPUTER
18	DIB7	COMPUTER DATA INPUT,	JOYSTICK	C4-20	COMPUTER
19	GROUND	GROUND			
20	GROUND	GROUND			
21					
22	DOB1	COMPUTER DATA OUTPUT		COMPUTER	C2-4; U17C-4
23	DOB3	COMPUTER DATA OUTPUT		COMPUTER	C2-8; U17C-11
24	DOB5	COMPUTER DATA OUTPUT		COMPUTER	C2-12; U17C-14
25	DOB7	COMPUTER DATA OUTPUT		COMPUTER	C2-16
26					

CABLE-VII BL1/COMPUTER PORT-C REGISTER SELECT (C7)

PIN	SIGNAL	SIGNAL DESCRIPTION	SOURCE	DESTINATION
1	-12V			
2	DIC0	COMPUTER DATA INPUT		COMPUTER
3	DIC2	COMPUTER DATA INPUT		COMPUTER
4	DIC4	COMPUTER DATA INPUT		COMPUTER
5	DIC6	COMPUTER DATA INPUT		COMPUTER
6				
7	+5V			
8				
9	DOC0	COMPUTER DATA OUTPUT	COMPUTER	BL1-U19B-1, U20B-1
10	DOC2	COMPUTER DATA OUTPUT	COMPUTER	BL1-U19B-3, U20B-3
11	DOC4	COMPUTER DATA OUTPUT	COMPUTER	BL1-U21D-5
12	DOC6	COMPUTER DATA OUTPUT	COMPUTER	BL1-U21D-2
13	+12V			
14	GROUND	GROUND		
15	DIC1	COMPUTER DATA INPUT		COMPUTER
16	DIC3	COMPUTER DATA INPUT		COMPUTER
17	DIC5	COMPUTER DATA INPUT		COMPUTER
18	DIC7	COMPUTER DATA INPUT		COMPUTER
19	GROUND	GROUND		
20	GROUND	GROUND		
21				
22	DOC1	COMPUTER DATA OUTPUT	COMPUTER	BL1-U19B-2, U20B-2
23	DOC3	COMPUTER DATA OUTPUT	COMPUTER	BL1-U19B-6, U20B-5
24	DOC5	COMPUTER DATA OUTPUT	COMPUTER	BL1-U21D-4
25	DOC7	COMPUTER DATA OUTPUT	COMPUTER	BL1-U21D-1
26				

BOARD-BM1,2 MEMORY BOARD

POSITION	TYPE	PINS	SPARES
U1A	58725	24	NONE
U1B	58725	24	NONE
U1C	58725	24	NONE
U1D	58725	24	NONE
U1E			
U2A	58725	24	NONE
U2B	58725	24	NONE
U2C	58725	24	NONE
U2D	58725	24	NONE
U2E			
U3A	58725	24	NONE
U3B	58725	24	NONE
U3C	58725	24	NONE
U3D	58725	24	NONE
U3E			
U4A	58725	24	NONE
U4B	58725	24	NONE
U4C	58725	24	NONE
U4D	58725	24	NONE
U4E			
U5A	58725	24	NONE
U5B	58725	24	NONE
U5C	58725	24	NONE
U5D	58725	24	NONE
U5E			
U6A	58725	24	NONE
U6B	58725	24	NONE
U6C	58725	24	NONE
U6D	58725	24	NONE
U6E			
U7A	58725	24	NONE
U7B	58725	24	NONE
U7C	58725	24	NONE
U7D	58725	24	NONE
U7E			

U8A	58725	24	NONE
U8B	58725	24	NONE
U8C	58725	24	NONE
U8D	58725	24	NONE
U8E			
U9A	58725	24	NONE
U9B	58725	24	NONE
U9C	58725	24	NONE
U9D	58725	24	NONE
U9E			
U10A	58725	24	NONE
U10B	58725	24	NONE
U10C	58725	24	NONE
U10D	58725	24	NONE
U10E			
U11A	58725	24	NONE
U11B	58725	24	NONE
U11C	58725	24	NONE
U11D	58725	24	NONE
U11E			
U12A	58725	24	NONE
U12B	58725	24	NONE
U12C	58725	24	NONE
U12D	58725	24	NONE
U12E			
U13A	58725	24	NONE
U13B	58725	24	NONE
U13C	58725	24	NONE
U13D	58725	24	NONE
U13E			
U14A	58725	24	NONE
U14B	58725	24	NONE
U14C	58725	24	NONE
U14D	58725	24	NONE
U14E			

U15A	58725	24	NONE
U15B	58725	24	NONE
U15C	58725	24	NONE
U15D	58725	24	NONE
U15E			
U16A	58725	24	NONE
U16B	58725	24	NONE
U16C	58725	24	NONE
U16D	58725	24	NONE
U16E			

U17A	8216	16	NONE	
U17B	8216	16	NONE	
U17C	8216	16	NONE	
U17D	8216	16	NONE	
U17E	LS00	14	NONE	
U18A	8216	16	NONE	
U18B	8216	16	NONE	
U18C	8216	16	NONE	
U18D	8216	16	NONE	
U18E	LS00	14	NONE	
U19A	8T97	16	NONE	(LS365 EQUIVALENT)
U19B	ALS138	16	NONE	
U19C	ALS138	16	NONE	
U19D	8T97	16	2/3	(LS365 EQUIVALENT)
U19E	LS138	16	NONE	
U20A				
U20B				
U20C				
U20D				
U20E				

BOARD-BB1 BUFFER BOARD

POSITION	TYPE	PINS	SPARES
U1A	LS175	16	12/10,11;13/15,14
U1B	LS02	14	5,6/4;8,9/10;11,12/13
U1C			
U1D			
U1E			
U1F			
U2A	ALS163	16	NONE
U2B	LS00	14	9,10/8;12,13/11
U2C			
U2D			
U2E			
U2F			
U3A	ALS163	16	NONE
U3B			
U3C	LS365	16	NONE
U3D	LS367	16	NONE
U3E	2149H	18	NONE
U3F			
U4A	ALS163	16	NONE
U4B			
U4C	LS365	16	NONE
U4D	LS367	16	NONE
U4E	2149H	18	NONE
U4F	ALS365	16	NONE
U5A	ALS161	16	NONE
U5B			
U5C	LS365	16	NONE
U5D	LS367	16	NONE
U5E	2149H	18	NONE
U5F	ALS365	16	NONE
U6A	ALS161	16	NONE
U6B	LS365	16	NONE
U6C	LS367	16	12/11;14/13
U6D	LS367	16	NONE
U6E	2149H	18	NONE
U6F	ALS367	16	12/11;14/13
U7A	ALS161	16	NONE
U7B	LS08	14	9,10/8;12,13/11
U7C	LS365	16	NONE
U7D	LS367	16	NONE
U7E	2149H	18	NONE
U7F			

U8A	ALS161	16	NONE
U8B	LS04	14	11/10;13/12
U8C	LS365	16	NONE
U8D	LS367	16	NONE
U8E	2149H	18	NONE
U8F	ALS365	16	NONE
U9A			
U9B			
U9C	LS365	16	NONE
U9D	LS367	16	NONE
U9E	2149H	18	NONE
U9F	ALS365	16	NONE
U10A			
U10B	LS365	16	NONE
U10C	LS367	16	12/11;14/13
U10D	LS367	16	NONE
U10E	2149H	18	NONE
U10F	ALS367	16	12/11;14/13
U11A			
U11B			
U11C	LS365	16	NONE
U11D	LS367	16	NONE
U11E	2149H	18	NONE
U11F			
U12A			
U12B	LS139	16	13,14,15/9,10,11,12
U12C	LS365	16	NONE
U12D	LS367	16	NONE
U12E	2149H	18	NONE
U12F	ALS365	16	NONE
U13A			
U13B	LS04	14	13/12
U13C	LS365	16	NONE
U13D	LS367	16	NONE
U13E	2149H	18	NONE
U13F	ALS365	16	NONE
U14A			
U14B	LS365	16	NONE
U14C	LS367	16	12/11;14/13
U14D	LS367	16	NONE
U14E	2149H	18	NONE
U14F	ALS367	16	12/11;14/13

U15A			
U15B			
U15C	LS365	16	NONE
U15D	LS367	16	NONE
U15E	2149H	18	NONE
U15F			
U16A			
U16B			
U16C	LS365	16	NONE
U16D	LS367	16	NONE
U16E	2149H	18	NONE
U16F	ALS365	16	NONE
U17A			
U17B			
U17C	LS365	16	NONE
U17D	LS367	16	NONE
U17E	2149H	18	NONE
U17F	ALS365	16	NONE
U18A			
U18B	LS365	16	NONE
U18C	LS367	16	12/11;14/13
U18D	LS367	16	NONE
U18E	2149H	18	NONE
U18F	ALS367	16	12/11;14/13
U19A	LS174	16	NONE
U19B	LS174	16	NONE
U19C	LS174	16	NONE
U19D	LS174	16	NONE
U19E			
U19F			
U20A	LS174	16	NONE
U20B	LS174	16	NONE
U20C	LS174	16	NONE
U20D	LS174	16	NONE
U20E			
U20F			
U21A	LS174	16	NONE
U21B	LS174	16	NONE
U21C	LS174	16	NONE
U21D	LS174	16	NONE
U21E	2149H	18	NONE
U21F			

U22A	LS174	16	NONE
U22B	LS174	16	NONE
U22C	LS257	16	NONE
U22D	LS257	16	14,13/12;11,10/9
U22E	2149H	18	NONE
U22F			
U23A			
U23B			
U23C	LS367	16	NONE
U23D	LS367	16	NONE
U23E	2149H	18	NONE
U23F			
U24A			
U24B			
U24C			
U24D			
U24E			
U24F			
U25A			
U25B			
U25C			
U25D			
U25E			
U25F			
U26A			
U26B			
U26C			
U26D			
U26E			
U26F			
U27A			
U27B			
U27C			
U27D			
U27E			
U27F			
U28A			
U28B			
U28C			
U28D			
U28E			
U28F			

BOARD-BL1 LOGIC BOARD

POSITION	TYPE	PINS	SPARES
U1A			
U1B			
U1C			
U1D			
U1E			
U2A			
U2B			
U2C			
U2D			
U2E			
U3A		14	
U3B		14	
U3C		14	
U3D		14	
U3E		14	
U4A		14	
U4B		14	
U4C		14	
U4D		14	
U4E			
U5A			
U5B	LS174	16	NONE
U5C	LS174	16	NONE
U5D	LS174	16	NONE
U5E	LS174	16	NONE
U6A			
U6B	LS283	16	NONE
U6C	LS283	16	NONE
U6D	S283	16	NONE
U6E	F283	16	NONE
U7A			
U7B	LS174	16	NONE
U7C	LS174	16	NONE
U7D	LS174	16	NONE
U7E	LS174	16	NONE

U8A	LS04	14	11/10;13/12
U8B	LS174	16	NONE
U8C	LS174	16	NONE
U8D	AS174	16	NONE
U8E	AS174	16	NONE
U9A	AS21	14	NONE
U9B	LS174	16	NONE
U9C	LS174	16	NONE
U9D	AS174	16	NONE
U9E	AS174	16	NONE
U10A	AS21	14	NONE
U10B	LS257	16	NONE
U10C	LS257	16	NONE
U10D	ALS257	16	NONE
U10E	ALS257	16	NONE
U11A	LS02	14	2,3/1;5,6/4;8,9/10;11,12/13
U11B	LS257	16	NONE
U11C	LS257	16	NONE
U11D	ALS257	16	NONE
U11E	ALS257	16	NONE
U12A	AS20	14	NONE
U12B	LS257	16	NONE
U12C	LS257	16	NONE
U12D	ALS257	16	NONE
U12E	ALS257	16	NONE
U13A	AS20	14	NONE
U13B	LS283	16	NONE
U13C	LS283	16	NONE
U13D	S283	16	NONE
U13E	S283	16	NONE
U14A	AS04	14	9/8;11/10;13/12
U14B	LS283	16	NONE
U14C	LS283	16	NONE
U14D	S283	16	NONE
U14E	S283	16	NONE

U15A	LS08	14	9,10/8
U15B	LS283	16	NONE
U15C	LS283	16	NONE
U15D	F283	16	NONE
U15E	F283	16	NONE
U16A	ALS32	14	8,9/10;11,12/13
U16B		16	
U16C		16	
U16D	F283	16	NONE
U16E	F283	16	NONE
U17A	ALS00	14	NONE
U17B	LS174	16	NONE
U17C	LS174	16	NONE
U17D	LS174	16	NONE
U17E	LS174	16	NONE
U18A		14	
U18B	LS04	14	1/2;3/4;9/8;11/10;13/12;5/6
U18C	LS32	14	NONE
U18D	LS04	14	11/10
U18E	LS00	14	10/8
U19A	LS02	14	5,6/4; 8,9/10; 11,12/13
U19B	LS138	16	NONE
U19C	LS02	14	NONE
U19D	LS02	14	8,9/10
U19E		14	
U20A		14	
U20B	LS138	16	NONE
U20C	LS02	14	NONE
U20D	LS02	14	NONE
U20E	LS08	14	NONE
U21A			
U21B	LS174	16	6/7;11/10;13/12;14/15 (CPD CLOCK)
U21C	LS02	14	NONE
U21D	LS20	14	NONE
U21E	LS04	14	NONE

U22A	LS04	14	5/6;11/10
U22B	LS00	14	4,5/6;9,10/8;12,13/11
U22C	LS32	14	NONE
U22D		14	
U22E	ALS174	16	3/2;4/5
U23A	OSC	-	NONE
U23B			
U23C	LS174	16	6/7;13/12;14/15
U23D	ALS174	16	NONE
U23E			
U24A	OSC	-	NONE
U24B			
U24C			
U24D			
U24E			

MEMORY TABLE-A TO MEMORY TABLE-D

MEMORY TABLE-A

RAM	PIN-1	PIN-2	PIN-3	PIN-4	PIN-5	PIN-6
U1A	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U2A	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U3A	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U4A	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U5A	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U6A	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U7A	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U8A	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U9A	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U10A	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U11A	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U12A	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U13A	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U14A	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U15A	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U16A	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U1B	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U2B	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U3B	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U4B	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U5B	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U6B	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U7B	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U8B	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U9B	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U10B	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U11B	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U12B	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U13B	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U14B	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U15B	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U16B	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7

MEMORY TABLE-A (CONTINUED)

RAM	PIN-7	PIN-8	PIN-9	PIN-10	PIN-11	PIN-12
U1A	U19A-5	U19A-3	U17A-3	U17A-6	U17A-10	GROUND
U2A	U19A-5	U19A-3	U17A-3	U17A-6	U17A-10	GROUND
U3A	U19A-5	U19A-3	U17A-3	U17A-6	U17A-10	GROUND
U4A	U19A-5	U19A-3	U17A-3	U17A-6	U17A-10	GROUND
U5A	U19A-5	U19A-3	U17A-3	U17A-6	U17A-10	GROUND
U6A	U19A-5	U19A-3	U17A-3	U17A-6	U17A-10	GROUND
U7A	U19A-5	U19A-3	U17A-3	U17A-6	U17A-10	GROUND
U8A	U19A-5	U19A-3	U17A-3	U17A-6	U17A-10	GROUND
U9A	U19A-5	U19A-3	U17A-3	U17A-6	U17A-10	GROUND
U10A	U19A-5	U19A-3	U17A-3	U17A-6	U17A-10	GROUND
U11A	U19A-5	U19A-3	U17A-3	U17A-6	U17A-10	GROUND
U12A	U19A-5	U19A-3	U17A-3	U17A-6	U17A-10	GROUND
U13A	U19A-5	U19A-3	U17A-3	U17A-6	U17A-10	GROUND
U14A	U19A-5	U19A-3	U17A-3	U17A-6	U17A-10	GROUND
U15A	U19A-5	U19A-3	U17A-3	U17A-6	U17A-10	GROUND
U16A	U19A-5	U19A-3	U17A-3	U17A-6	U17A-10	GROUND
U1B	U19A-5	U19A-3	U17B-3	U17B-6	U17B-10	GROUND
U2B	U19A-5	U19A-3	U17B-3	U17B-6	U17B-10	GROUND
U3B	U19A-5	U19A-3	U17B-3	U17B-6	U17B-10	GROUND
U4B	U19A-5	U19A-3	U17B-3	U17B-6	U17B-10	GROUND
U5B	U19A-5	U19A-3	U17B-3	U17B-6	U17B-10	GROUND
U6B	U19A-5	U19A-3	U17B-3	U17B-6	U17B-10	GROUND
U7B	U19A-5	U19A-3	U17B-3	U17B-6	U17B-10	GROUND
U8B	U19A-5	U19A-3	U17B-3	U17B-6	U17B-10	GROUND
U9B	U19A-5	U19A-3	U17B-3	U17B-6	U17B-10	GROUND
U10B	U19A-5	U19A-3	U17B-3	U17B-6	U17B-10	GROUND
U11B	U19A-5	U19A-3	U17B-3	U17B-6	U17B-10	GROUND
U12B	U19A-5	U19A-3	U17B-3	U17B-6	U17B-10	GROUND
U13B	U19A-5	U19A-3	U17B-3	U17B-6	U17B-10	GROUND
U14B	U19A-5	U19A-3	U17B-3	U17B-6	U17B-10	GROUND
U15B	U19A-5	U19A-3	U17B-3	U17B-6	U17B-10	GROUND
U16B	U19A-5	U19A-3	U17B-3	U17B-6	U17B-10	GROUND

MEMORY TABLE-B

RAM	PIN-1	PIN-2	PIN-3	PIN-4	PIN-5	PIN-6
U1C	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U2C	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U3C	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U4C	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U5C	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U6C	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U7C	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U8C	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U9C	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U10C	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U11C	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U12C	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U13C	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U14C	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U15C	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U16C	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U1D	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U2D	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U3D	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U4D	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U5D	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U6D	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U7D	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U8D	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U9D	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U10D	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U11D	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U12D	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U13D	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U14D	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U15D	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7
U16D	U19D-7	U19D-5	U19A-13	U19A-11	U19A-9	U19A-7

MEMORY TABLE-B (CONTINUED)

RAM	PIN-7	PIN-8	PIN-9	PIN-10	PIN-11	PIN-12
U1C	U19A-5	U19A-3	U17C-3	U17C-6	U17C-10	GROUND
U2C	U19A-5	U19A-3	U17C-3	U17C-6	U17C-10	GROUND
U3C	U19A-5	U19A-3	U17C-3	U17C-6	U17C-10	GROUND
U4C	U19A-5	U19A-3	U17C-3	U17C-6	U17C-10	GROUND
U5C	U19A-5	U19A-3	U17C-3	U17C-6	U17C-10	GROUND
U6C	U19A-5	U19A-3	U17C-3	U17C-6	U17C-10	GROUND
U7C	U19A-5	U19A-3	U17C-3	U17C-6	U17C-10	GROUND
U8C	U19A-5	U19A-3	U17C-3	U17C-6	U17C-10	GROUND
U9C	U19A-5	U19A-3	U17C-3	U17C-6	U17C-10	GROUND
U10C	U19A-5	U19A-3	U17C-3	U17C-6	U17C-10	GROUND
U11C	U19A-5	U19A-3	U17C-3	U17C-6	U17C-10	GROUND
U12C	U19A-5	U19A-3	U17C-3	U17C-6	U17C-10	GROUND
U13C	U19A-5	U19A-3	U17C-3	U17C-6	U17C-10	GROUND
U14C	U19A-5	U19A-3	U17C-3	U17C-6	U17C-10	GROUND
U15C	U19A-5	U19A-3	U17C-3	U17C-6	U17C-10	GROUND
U16C	U19A-5	U19A-3	U17C-3	U17C-6	U17C-10	GROUND
U1D	U19A-5	U19A-3	U17D-3	U17D-6	U17D-10	GROUND
U2D	U19A-5	U19A-3	U17D-3	U17D-6	U17D-10	GROUND
U3D	U19A-5	U19A-3	U17D-3	U17D-6	U17D-10	GROUND
U4D	U19A-5	U19A-3	U17D-3	U17D-6	U17D-10	GROUND
U5D	U19A-5	U19A-3	U17D-3	U17D-6	U17D-10	GROUND
U6D	U19A-5	U19A-3	U17D-3	U17D-6	U17D-10	GROUND
U7D	U19A-5	U19A-3	U17D-3	U17D-6	U17D-10	GROUND
U8D	U19A-5	U19A-3	U17D-3	U17D-6	U17D-10	GROUND
U9D	U19A-5	U19A-3	U17D-3	U17D-6	U17D-10	GROUND
U10D	U19A-5	U19A-3	U17D-3	U17D-6	U17D-10	GROUND
U11D	U19A-5	U19A-3	U17D-3	U17D-6	U17D-10	GROUND
U12D	U19A-5	U19A-3	U17D-3	U17D-6	U17D-10	GROUND
U13D	U19A-5	U19A-3	U17D-3	U17D-6	U17D-10	GROUND
U14D	U19A-5	U19A-3	U17D-3	U17D-6	U17D-10	GROUND
U15D	U19A-5	U19A-3	U17D-3	U17D-6	U17D-10	GROUND
U16D	U19A-5	U19A-3	U17D-3	U17D-6	U17D-10	GROUND

MEMORY TABLE-C

RAM	PIN-13	PIN-14	PIN-15	PIN-16	PIN-17	PIN-18
U1A	U17A-13	U18A-3	U18A-6	U18A-10	U18A-13	U19B-15
U2A	U17A-13	U18A-3	U18A-6	U18A-10	U18A-13	U19B-15
U3A	U17A-13	U18A-3	U18A-6	U18A-10	U18A-13	U19B-15
U4A	U17A-13	U18A-3	U18A-6	U18A-10	U18A-13	U19B-15
U5A	U17A-13	U18A-3	U18A-6	U18A-10	U18A-13	U19B-15
U6A	U17A-13	U18A-3	U18A-6	U18A-10	U18A-13	U19B-15
U7A	U17A-13	U18A-3	U18A-6	U18A-10	U18A-13	U19B-15
U8A	U17A-13	U18A-3	U18A-6	U18A-10	U18A-13	U19B-15
U9A	U17A-13	U18A-3	U18A-6	U18A-10	U18A-13	U19B-14
U10A	U17A-13	U18A-3	U18A-6	U18A-10	U18A-13	U19B-14
U11A	U17A-13	U18A-3	U18A-6	U18A-10	U18A-13	U19B-14
U12A	U17A-13	U18A-3	U18A-6	U18A-10	U18A-13	U19B-14
U13A	U17A-13	U18A-3	U18A-6	U18A-10	U18A-13	U19B-14
U14A	U17A-13	U18A-3	U18A-6	U18A-10	U18A-13	U19B-14
U15A	U17A-13	U18A-3	U18A-6	U18A-10	U18A-13	U19B-14
U16A	U17A-13	U18A-3	U18A-6	U18A-10	U18A-13	U19B-14
U1B	U17B-13	U18B-3	U18B-6	U18B-10	U18B-13	U19B-13
U2B	U17B-13	U18B-3	U18B-6	U18B-10	U18B-13	U19B-13
U3B	U17B-13	U18B-3	U18B-6	U18B-10	U18B-13	U19B-13
U4B	U17B-13	U18B-3	U18B-6	U18B-10	U18B-13	U19B-13
U5B	U17B-13	U18B-3	U18B-6	U18B-10	U18B-13	U19B-13
U6B	U17B-13	U18B-3	U18B-6	U18B-10	U18B-13	U19B-13
U7B	U17B-13	U18B-3	U18B-6	U18B-10	U18B-13	U19B-13
U8B	U17B-13	U18B-3	U18B-6	U18B-10	U18B-13	U19B-13
U9B	U17B-13	U18B-3	U18B-6	U18B-10	U18B-13	U19B-12
U10B	U17B-13	U18B-3	U18B-6	U18B-10	U18B-13	U19B-12
U11B	U17B-13	U18B-3	U18B-6	U18B-10	U18B-13	U19B-12
U12B	U17B-13	U18B-3	U18B-6	U18B-10	U18B-13	U19B-12
U13B	U17B-13	U18B-3	U18B-6	U18B-10	U18B-13	U19B-12
U14B	U17B-13	U18B-3	U18B-6	U18B-10	U18B-13	U19B-12
U15B	U17B-13	U18B-3	U18B-6	U18B-10	U18B-13	U19B-12
U16B	U17B-13	U18B-3	U18B-6	U18B-10	U18B-13	U19B-12

MEMORY TABLE-C (CONTINUED)

RAM	PIN-19	PIN-20	PIN-21	PIN-22	PIN-23	PIN-24
U1A	U19D-13	U19C-15	U19E-15	U19D-11	U19D-9	VCC
U2A	U19D-13	U19C-14	U19E-14	U19D-11	U19D-9	VCC
U3A	U19D-13	U19C-13	U19E-13	U19D-11	U19D-9	VCC
U4A	U19D-13	U19C-12	U19E-12	U19D-11	U19D-9	VCC
U5A	U19D-13	U19C-11	U19E-11	U19D-11	U19D-9	VCC
U6A	U19D-13	U19C-10	U19E-10	U19D-11	U19D-9	VCC
U7A	U19D-13	U19C-9	U19E-9	U19D-11	U19D-9	VCC
U8A	U19D-13	U19C-7	U19E-7	U19D-11	U19D-9	VCC
U9A	U19D-13	U19C-15	U19E-15	U19D-11	U19D-9	VCC
U10A	U19D-13	U19C-14	U19E-14	U19D-11	U19D-9	VCC
U11A	U19D-13	U19C-13	U19E-13	U19D-11	U19D-9	VCC
U12A	U19D-13	U19C-12	U19E-12	U19D-11	U19D-9	VCC
U13A	U19D-13	U19C-11	U19E-11	U19D-11	U19D-9	VCC
U14A	U19D-13	U19C-10	U19E-10	U19D-11	U19D-9	VCC
U15A	U19D-13	U19C-9	U19E-9	U19D-11	U19D-9	VCC
U16A	U19D-13	U19C-7	U19E-7	U19D-11	U19D-9	VCC
U1B	U19D-13	U19C-15	U19E-15	U19D-11	U19D-9	VCC
U2B	U19D-13	U19C-14	U19E-14	U19D-11	U19D-9	VCC
U3B	U19D-13	U19C-13	U19E-13	U19D-11	U19D-9	VCC
U4B	U19D-13	U19C-12	U19E-12	U19D-11	U19D-9	VCC
U5B	U19D-13	U19C-11	U19E-11	U19D-11	U19D-9	VCC
U6B	U19D-13	U19C-10	U19E-10	U19D-11	U19D-9	VCC
U7B	U19D-13	U19C-9	U19E-9	U19D-11	U19D-9	VCC
U8B	U19D-13	U19C-7	U19E-7	U19D-11	U19D-9	VCC
U9B	U19D-13	U19C-15	U19E-15	U19D-11	U19D-9	VCC
U10B	U19D-13	U19C-14	U19E-14	U19D-11	U19D-9	VCC
U11B	U19D-13	U19C-13	U19E-13	U19D-11	U19D-9	VCC
U12B	U19D-13	U19C-12	U19E-12	U19D-11	U19D-9	VCC
U13B	U19D-13	U19C-11	U19E-11	U19D-11	U19D-9	VCC
U14B	U19D-13	U19C-10	U19E-10	U19D-11	U19D-9	VCC
U15B	U19D-13	U19C-9	U19E-9	U19D-11	U19D-9	VCC
U16B	U19D-13	U19C-7	U19E-7	U19D-11	U19D-9	VCC

MEMORY TABLE-D

RAM	PIN-13	PIN-14	PIN-15	PIN-16	PIN-17	PIN-18
U1C	U17C-13	U18C-3	U18C-6	U18C-10	U18C-13	U19B-11
U2C	U17C-13	U18C-3	U18C-6	U18C-10	U18C-13	U19B-11
U3C	U17C-13	U18C-3	U18C-6	U18C-10	U18C-13	U19B-11
U4C	U17C-13	U18C-3	U18C-6	U18C-10	U18C-13	U19B-11
U5C	U17C-13	U18C-3	U18C-6	U18C-10	U18C-13	U19B-11
U6C	U17C-13	U18C-3	U18C-6	U18C-10	U18C-13	U19B-11
U7C	U17C-13	U18C-3	U18C-6	U18C-10	U18C-13	U19B-11
U8C	U17C-13	U18C-3	U18C-6	U18C-10	U18C-13	U19B-11
U9C	U17C-13	U18C-3	U18C-6	U18C-10	U18C-13	U19B-10
U10C	U17C-13	U18C-3	U18C-6	U18C-10	U18C-13	U19B-10
U11C	U17C-13	U18C-3	U18C-6	U18C-10	U18C-13	U19B-10
U12C	U17C-13	U18C-3	U18C-6	U18C-10	U18C-13	U19B-10
U13C	U17C-13	U18C-3	U18C-6	U18C-10	U18C-13	U19B-10
U14C	U17C-13	U18C-3	U18C-6	U18C-10	U18C-13	U19B-10
U15C	U17C-13	U18C-3	U18C-6	U18C-10	U18C-13	U19B-10
U16C	U17C-13	U18C-3	U18C-6	U18C-10	U18C-13	U19B-10
U1D	U17D-13	U18D-3	U18D-6	U18D-10	U18D-13	U19B-9
U2D	U17D-13	U18D-3	U18D-6	U18D-10	U18D-13	U19B-9
U3D	U17D-13	U18D-3	U18D-6	U18D-10	U18D-13	U19B-9
U4D	U17D-13	U18D-3	U18D-6	U18D-10	U18D-13	U19B-9
U5D	U17D-13	U18D-3	U18D-6	U18D-10	U18D-13	U19B-9
U6D	U17D-13	U18D-3	U18D-6	U18D-10	U18D-13	U19B-9
U7D	U17D-13	U18D-3	U18D-6	U18D-10	U18D-13	U19B-9
U8D	U17D-13	U18D-3	U18D-6	U18D-10	U18D-13	U19B-9
U9D	U17D-13	U18D-3	U18D-6	U18D-10	U18D-13	U19B-7
U10D	U17D-13	U18D-3	U18D-6	U18D-10	U18D-13	U19B-7
U11D	U17D-13	U18D-3	U18D-6	U18D-10	U18D-13	U19B-7
U12D	U17D-13	U18D-3	U18D-6	U18D-10	U18D-13	U19B-7
U13D	U17D-13	U18D-3	U18D-6	U18D-10	U18D-13	U19B-7
U14D	U17D-13	U18D-3	U18D-6	U18D-10	U18D-13	U19B-7
U15D	U17D-13	U18D-3	U18D-6	U18D-10	U18D-13	U19B-7
U16D	U17D-13	U18D-3	U18D-6	U18D-10	U18D-13	U19B-7

MEMORY TABLE-D (CONTINUED)

RAM	PIN-19	PIN-20	PIN-21	PIN-22	PIN-23	PIN-24
U1C	U19D-13	U19C-15	U19E-15	U19D-11	U19D-9	VCC
U2C	U19D-13	U19C-14	U19E-14	U19D-11	U19D-9	VCC
U3C	U19D-13	U19C-13	U19E-13	U19D-11	U19D-9	VCC
U4C	U19D-13	U19C-12	U19E-12	U19D-11	U19D-9	VCC
U5C	U19D-13	U19C-11	U19E-11	U19D-11	U19D-9	VCC
U6C	U19D-13	U19C-10	U19E-10	U19D-11	U19D-9	VCC
U7C	U19D-13	U19C-9	U19E-9	U19D-11	U19D-9	VCC
U8C	U19D-13	U19C-7	U19E-7	U19D-11	U19D-9	VCC
U9C	U19D-13	U19C-15	U19E-15	U19D-11	U19D-9	VCC
U10C	U19D-13	U19C-14	U19E-14	U19D-11	U19D-9	VCC
U11C	U19D-13	U19C-13	U19E-13	U19D-11	U19D-9	VCC
U12C	U19D-13	U19C-12	U19E-12	U19D-11	U19D-9	VCC
U13C	U19D-13	U19C-11	U19E-11	U19D-11	U19D-9	VCC
U14C	U19D-13	U19C-10	U19E-10	U19D-11	U19D-9	VCC
U15C	U19D-13	U19C-9	U19E-9	U19D-11	U19D-9	VCC
U16C	U19D-13	U19C-7	U19E-7	U19D-11	U19D-9	VCC
U1D	U19D-13	U19C-15	U19E-15	U19D-11	U19D-9	VCC
U2D	U19D-13	U19C-14	U19E-14	U19D-11	U19D-9	VCC
U3D	U19D-13	U19C-13	U19E-13	U19D-11	U19D-9	VCC
U4D	U19D-13	U19C-12	U19E-12	U19D-11	U19D-9	VCC
U5D	U19D-13	U19C-11	U19E-11	U19D-11	U19D-9	VCC
U6D	U19D-13	U19C-10	U19E-10	U19D-11	U19D-9	VCC
U7D	U19D-13	U19C-9	U19E-9	U19D-11	U19D-9	VCC
U8D	U19D-13	U19C-7	U19E-7	U19D-11	U19D-9	VCC
U9D	U19D-13	U19C-15	U19E-15	U19D-11	U19D-9	VCC
U10D	U19D-13	U19C-14	U19E-14	U19D-11	U19D-9	VCC
U11D	U19D-13	U19C-13	U19E-13	U19D-11	U19D-9	VCC
U12D	U19D-13	U19C-12	U19E-12	U19D-11	U19D-9	VCC
U13D	U19D-13	U19C-11	U19E-11	U19D-11	U19D-9	VCC
U14D	U19D-13	U19C-10	U19E-10	U19D-11	U19D-9	VCC
U15D	U19D-13	U19C-9	U19E-9	U19D-11	U19D-9	VCC
U16D	U19D-13	U19C-7	U19E-7	U19D-11	U19D-9	VCC

BASIC PROGRAM LISTING

GRAPH.ASC

```
100     PRINT: PRINT: PRINT "FILE: GRAPH.ASC"
110     CLEAR
1940    R%=INP (236): S%=R% AND 1: IF S%=1 THEN 1940    'LOCKUP
ON VERT.SYNC=1
1980    R%=INP (236): S%=R% AND 16: IF S%=0 THEN 1940   'CHECK FIELD
1990    OUT 236,64       'INITIALIZE GRAPHICS GENERATOR
1992    R%=INP (236): S%=R% AND 1
1993    IF S%=0 THEN 1992        'LOCKUP ON VERT.SYNC=0
1994    OUT 236,0                          'COMMAND LOAD, RUN-BAR
1995        OUT 238, 246: OUT 237, 0: OUT 236,128: OUT 236,0
'X-ROW MSB
1996        OUT 238, 247: OUT 237, 0: OUT 236,128: OUT 236,0
'X-ROW LSB
1997        OUT 238,242: OUT 237, 0:  OUT 236,128: OUT 236,0
'X-PIXEL SLOPE MSB
1998        OUT 238,245: OUT 237, 0:  OUT 236,128: OUT 236,0
'Y-PIXEL SLOPE MSB
1999        OUT 238,248: OUT 237, 0:  OUT 236,128: OUT 236,0
'X-ROW SLOPE MSB
2000        OUT 238,251: OUT 237, 0:  OUT 236,128: OUT 236,0
'Y-ROW SLOPE MSB
2001        OUT 238,244: OUT 237, 0:  OUT 236,128: OUT 236,0
'Y-PIXEL SLOPE LSB
2002        OUT 238,240: OUT 237, 0:  OUT 236,128: OUT 236,0
'X-ROW SLOPE LSB
2003        OUT 238,243: OUT 237, 255:  OUT 236,128: OUT 236,0
'X-PIXEL SLOPE LSB
2004        OUT 238,241: OUT 237, 255:  OUT 236,128: OUT 236,0
'Y-ROW SLOPE LSB
2005    OUT 236,80  'COMMAND RUN, LOAD-BAR ;PULSE-1 BRACKETING
COMPUTATION PERIOD
2006    R%=INP (236): S%=R% AND 1: IF S%=1 THEN 2006    'LOCKUP
ON VERT.SYNC=1
2007    R%=INP (236): S%=R% AND 16: IF S%=0 THEN 2006   'CHECK FIELD
2060  'ITERATIVE PROCESSING
2100    OUT 236,64
2140    'RESYNCHRONIZATION AND FIELD CONTROL PROCESSOR
2220    R%=INP (236): S%=R% AND 1
2300    IF S%=0 THEN 2220        'LOCKUP ON VERT.SYNC=0
3060            'INTERLACED SCAN CALCULATIONS
3100            'INPUT BYTE   128 064 032 016 008 004 002 001
3140            '                  F2       F1       LS       FS
3180    OUT 236,0                          'COMMAND LOAD, RUN-BAR
3220    R%=INP (236): S%=R% AND 16: IF S%=0 THEN 3540 ELSE 3260
'CHECK FIELD
3260                    'FIELD-2
3300      'OUTPUT  POSITION PARAMETERS
3340        OUT 238, 249: OUT 237, 0: OUT 236,128: OUT 236,0
'Y-ROW MSB
3380        OUT 238, 250: OUT 237, 4: OUT 236,128: OUT 236,0
'Y-ROW LSB
3500    GOTO 4140
```

```
3540                        'FIELD-1
3580       'OUTPUT  POSITION PARAMETERS
3620         OUT 238, 249: OUT 237, 0: OUT 236,128: OUT 236,0
'Y-ROW MSB
3660         OUT 238, 250: OUT 237, 0: OUT 236,128: OUT 236,0
'Y-ROW LSB
4140     OUT 236,80  'COMMAND RUN, LOAD-BAR ;PULSE-1 BRACKETING
COMPUTATION PERIOD
4220     GOTO 2060                  'LOOP BACK FOR NEXT FIELD
20000    END
```

BASIC PROGRAM LISTING

LD.ASC

```
50      PRINT "ACCESSED "LD" FILE TO LOAD IMAGE MEMORY:
REV.5/15/84 09:00"
55      INPUT "MURPHY (M) OR CAMILLE (C)";K200$
100     INT1%=0: D%=0: K8%=1: K9%=1
112     PRINT: PRINT "*********************************************"
114     PRINT "   SELECT OPERATION"
116     PRINT "*********************************************": PRINT
118     PRINT "RETURN TO OPERATING SYSTEM ..................... 0"
120     PRINT "SELECT OVERLAY FOR LOADING INTO IMAGE MEMORY ... 1"
122     PRINT "SELECT IMAGE TO BE LOADED INTO IMAGE MEMORY"
124     PRINT "       CONCENTRIC SQUARE FRAMES ................ 2"
126     PRINT "       RECTANGLES AND LINES .................... 3"
128     PRINT "       SPIRALS ................................. 4"
130     PRINT "       VIEWPORT COORDINATE SYMBOLS ............. 5"
132     PRINT "       PATTERN #6 .............................. 6"
134     PRINT "       PATTERN #7 .............................. 7"
136     PRINT "       SQUARE PATTERN  ......................... 8"
138     PRINT "       SQUARE FRAMES ........................... 9"
140     PRINT "       PERIPHERAL SQUARES ..................... 10"
141     PRINT "       PERIPHERAL TRIANGLES ................... 11"
142     PRINT "       HOUSE ................................... 12"
151     INPUT "                                    SELECT OPERATION
NUMBER";A20%
152     IF A20%<13 THEN 155
153     PRINT "******************": PRINT "IMPROPER SELECTION":
PRINT "******************"
154     GOTO 112
155     IF A20%>0 THEN 158
156             SYSTEM
158     ON A20% GOSUB 170, 4400, 4530, 5500, 4500, 7500, 8500,
9000, 9040, 9180, 9280, 11070
159     GOTO 112
170     PRINT: PRINT "************************************************"
171     PRINT "   SELECT OVERLAY FOR LOADING INTO IMAGE MEMORY"
172     PRINT "************************************************": PRINT
173     PRINT "  RETURN TO MAIN MENU ........................... 0"
174     PRINT "  SELECT RECTANGULAR IMAGE MEMORY PATTERN"
180     PRINT "      HORIZONTAL BARS"
200     PRINT "         3-2-2 WIDTH BARS, INTENSITY VARIATIONS . 1"
220     PRINT "         1-1-1 WIDTH BARS, MAXIMUM INTENSITY ... 2"
240     PRINT "         LINEAR COUNT, ALL COLOR COMBINATIONS .. 8"
260     PRINT "      SOLID SINGLE COLORED IMAGES"
265     PRINT "         RECTANGLE ............................. 3"
270     PRINT "         BACKGROUND ............................ 4"
400     PRINT "      CHECKERBOARD"
420     PRINT "         4-COLORS .............................. 6"
440     PRINT "         2-COLORS .............................. 7"
442     PRINT "      VARIABLE SINGLE COLORS"
443     PRINT "         GREEN SAWTOOTH ........................ 10"
460     PRINT "      CENTER ELEMENT"
480     PRINT "         9-PIXEL SQUARE ........................ 11"
482     PRINT "  SELECT SLOPING LINE ........................... 12"
484     INPUT "                                    SELECT PATTERN
```

```
500             RETURN
502     IF A5%<13 THEN 520
503     PRINT "*****************": PRINT "IMPROPER SELECTION":
PRINT "*****************"
504     GOTO 170
520     IF A5%=3 OR A5%=4 OR A5%=12 THEN 523 ELSE 535
523     PRINT "COLOR CODE"
524     PRINT "       BLACK .........  0"
526     PRINT "       GREEN .........  1  TO   7"
527     PRINT "       RED ...........  8, 16, 24"
528     PRINT "       BLUE ..........  32, 64, 96"
529     INPUT "                                        SELECT COLOR
CODE SUM";INT1%
530     IF INT1%<128 THEN 535
531     PRINT:PRINT "****************************************"
532     PRINT "IMPROPER COLOR CODE; ENTER COLOR CODE AGAIN"
533     PRINT "****************************************":PRINT
534     GOTO 523
535     IF A5%=11 THEN 2040
540     IF A5%=6 OR A5%=7 GOTO 560 ELSE 570
560             INPUT "CHECKERBOARD RESOLUTION, PIXELS PER
SIDE";A6%
570     IF A5%=4 THEN 575 ELSE 580
575             A5%=3: XB%=0: YB%=0: XE%=511: YE%=511: GOTO 623
580     INPUT "   START PIXEL COORDINATE";XB%,YB%
620     INPUT "   STOP  PIXEL COORDINATE";XE%,YE%
623     GOSUB 630
624     GOTO 170
630     '*******************************************************
632     'SUBROUTINE TO OVERLAY A RECTANGLE
635             XB%=(XB%+1)*8: YB%=(YB%+1)*8
640             XE%=(XE%+1)*8: YE%=(YE%+1)*8
642'    IF XB%=>8 AND XB%<XE% AND XE%=>8 AND XB%=<512*8 AND
XE%=<512*8 THEN 643 ELSE 656
643'    IF YB%=>8 AND YB%<YE% AND YE%=>8 AND YB%=<512*8 AND
YE%=<512*8 THEN 660 ELSE 656
656'    PRINT:PRINT "****************************************"
657'    PRINT "IMPROPER PIXEL COORDINATES, ENTER PIXEL
COORDINATES AGAIN"
658'    PRINT "****************************************":PRINT
659'    GOTO 580
660'    PRINT: PRINT "****************************************"
665'    PRINT "       IMAGE MEMORY IS BEING LOADED"    'PRINT
"ROW","COLOR INTENSITY"
666'    PRINT "*******************************************": PRINT
667     IF A5%=12 THEN 4200
690     XPS%=256: YPS%=0: XRP%=XB%-8
695     GOSUB 3000
700     FOR OUTLP1%=YB% TO YE% STEP 8           'ROW LOOP
710     YRP%=OUTLP1%-8          'UPDATE TO NEXT ROW
711     XRP%=XB%-8
712     GOSUB 3000              'LOAD IMP REGISTERS
948     OUT 236,32              'SET SEQUENTIAL LOAD COMMAND
1230    'DETERMINE INTENSITY (INT1%)
```

```
1260,1460,1720,1250,1250,1920,1980,1800,1250,1820
1250    PRINT "**************": PRINT "SELECT A DIFFERENT IMAGE":
PRINT "**************"
1260    IF D%<8 THEN 1340          'IMAGE PATTERN 1
1280    IF D%<32 THEN 1380         ' !-64-32-!-16-08-!-04-02-01-!
1300    IF D%<128 THEN 1420        ' !  BLUE !  RED  !  GREEN   !
1320    INT1%=0: D%=0: GOTO 1980
1340    INT1%=D% AND 7
1360            D%=D%+1: GOTO 1980
1380    INT1%=D% AND 24
1400            D%=D%+8: GOTO 1980
1420    INT1%=D% AND 96
1440            D%=D%+32: GOTO 1980
1460    A3%=FIX ((OUTLP1%-8)/8)                    'IMAGE PATTERN 2
1480    GOSUB 1520
1500    GOTO 1980
1520    '***** SUBROUTINE, MAXIMUM COLOR *********************
1540            A4%=A3% AND 3
1560            A7%=A4%+1
1580            ON A7% GOTO 1600,1620,1640,1660
1600            INT1%=0: GOTO 1680
1620            INT1%=7: GOTO 1680
1640            INT1%=24: GOTO 1680
1660            INT1%=96
1680    RETURN
1700 '*************************************************************
1720            INT1%=INT1%: GOTO 1980          'PATTERN-3, SOLID
COLOR
1800            K2%=(OUTLP1%-8)/8: INT1%= K2% AND 127: GOTO 1980
'PATTERN 8, LINEAR COUNT
1820    INT1%=K8%: K10%=K9% AND 1
1840    IF K10%=0 THEN 1920
1860            K8%=K8%+1                          'UPCOUNT, ADD
1880            IF K8%<8 THEN 1980
1900              K9%=K9%+1: K8%=6: GOTO 1980           'CHANGE
COUNT DIRECTION
1920            K8%=K8%-1                          'DOWNCOUNT, SUBT
1940            IF K8%>0 THEN 1980
1960              K9%=K9%+1: K8%=2: GOTO 1980
'CHANGE COUNT DIRECTION
1980    SP1%=INIT1% AND 1: SP2%= INIT1% AND 3: SP3%=INT1% AND 7:
SP4%=INT1% AND 15: SP5%=INT1% AND 31: SP6%=INT1% AND 63:
SP7%=INT1% AND 127
1985    OUT 238, 252: OUT 237, SP1%: OUT 237, SP2%: OUT 237,
SP3%: OUT 237, SP4%: OUT 237,SP5%: OUT 237,SP6%: OUT 237, SP7%:
OUT 237, INT1%  'DATA TO LOAD IN IMAGE MEMORY
1991    ON A5% GOTO
1994,1994,1994,1994,1994,1994,1993,1994,1994,1994
1992    A3%=FIX((2*OUTLP1%+INLP1%)/A6%): GOSUB 1520: GOTO 1994
1993    A3%=FIX((2*OUTLP1%+2*INLP1%)/A6%): GOSUB 1520: GOTO 1994
1994    FOR INLP1%=XB% TO XE% STEP 8               'PIXEL LOOP
1995    OUT 236,160: OUT 236,32
1996    NEXT INLP1%
1997    OUT 237, SP7%: OUT 237, SP6%: OUT 237, SP5%: OUT 237,
```

```
'DATA TO LOAD IN IMAGE MEMORY
1999     IF K200$="M" THEN
2000     A8%=INP (93): A8%=A8% AND 2: IF A8%=0 THEN 2009
'OPERATOR RESET
2001     A8%=INP (92): GOTO 2006
2002     A8%=INP (1): A8%=A8% AND 2: IF A8%=0 THEN 2009
'OPERATOR RESET
2003     A8%=INP (0)
2006         A9%=A8% XOR 155: IF A9%=0 THEN 100  'ESCAPE TO MENU
2007         A9%=A8% XOR 127: IF A9%=0 THEN 2008 ELSE 2009
'DELETE TO SYSTEM
2008              SYSTEM
2009     NEXT OUTLP1%
2010'    PRINT CHR$(7); :PRINT "MEMORY LOAD COMPLETE"
2020     RETURN             'RETURN TO OVERLAY MENU
2040     'PATTERN 11
2060     INT1%=7: K17%=(256-3)*8: K18%=(256+3)*8
2080     FOR OUTLP1%=K17% TO K18% STEP 8
2100       OUT 238, 249                          'Y-ROW MSB
2120           C%=FIX(OUTLP1%/64): OUT 237, C%: OUT 236,129: OUT 236,1
2140       OUT 238, 250                          'Y-ROW LSB
2160           C%=OUTLP1% AND 63: OUT 237, C%: OUT 236,129: OUT 236,1
2180     FOR INLP1%=K17% TO K18% STEP 8          'PIXEL LOOP
2200       OUT 238, 246                          'X-ROW MSB
2220           C%=FIX(INLP1%/64): OUT 237, C%: OUT 236,129: OUT 236,1
2240       OUT 238, 247                          'X-ROW LSB
2260           C%=INLP1% AND 63: OUT 237, C%: OUT 236,129: OUT 236,1
2280       OUT 238, 252                          'DATA TO LOAD IN IMAGE MEMORY
2300     OUT 237, INT1%: OUT 236,129: OUT 236,1
2320     NEXT INLP1%
2340     NEXT OUTLP1%
2360       OUTLP1%=(256-5)*8
2380       OUT 238, 249                          'Y-ROW MSB
2400           C%=FIX(OUTLP1%/64): OUT 237, C%: OUT 236,129: OUT 236,1
2420       OUT 238, 250                          'Y-ROW LSB
2440           C%=OUTLP1% AND 63: OUT 237, C%: OUT 236,129: OUT 236,1
2460     K17%=(256-6)*8: K18%=(256)*8
2480     FOR INLP1%=K17% TO K18% STEP 8          'PIXEL LOOP
2500       OUT 238, 246                          'X-ROW MSB
2520           C%=FIX(INLP1%/64): OUT 237, C%: OUT 236,129: OUT 236,1
2540       OUT 238, 247                          'X-ROW LSB
2560           C%=INLP1% AND 63: OUT 237, C%: OUT 236,129: OUT 236,1
2580       OUT 238, 252                          'DATA TO LOAD IN IMAGE MEMORY
2600     OUT 237, INT1%: OUT 236,129: OUT 236,1
2620     NEXT INLP1%
2640     GOTO 2000
3000     '*************** SUBROUTINE TO OUTPUT  POSITION AND SLOPE PARAME
3001     OUT 236,0     'DOA5 TURNED OFF TO DISABLE SEQUENCING
DURING LOADING OF REGISTERS
3002     'SLOPE SCALE FACTOR-256*PIXELS/STEP
3003     'POSITION SCALE FACTOR -8*PIXELS
3004     XPSM%=FIX(XPS%/64):     XPSL%=XPS% AND 63
3005         OUT 238,242: OUT 237,XPSM%: OUT 236,128: OUT 236,0
'X-PIXEL SLOPE MSB
3006         OUT 238,243: OUT 237,XPSL%: OUT 236,128: OUT 236,0
```

```
'X-PIXEL SLOPE LSH
3007    YPSM%=FIX(YPS%/64):    YPSL%=YPS% AND 63
3008        OUT 238,245: OUT 237,YPSM%: OUT 236,128: OUT 236,0
'Y-PIXEL SLOPE MSH
3009        OUT 238,244: OUT 237,YPSL%: OUT 236,128: OUT 236,0
'Y-PIXEL SLOPE LSH
3010'   OUT 236, 0       'SUBROUTINE ENTRY POINT
3020    XRPM%=FIX(XRP%/64):    XRPL%=XRP% AND 63
3091    YRPM%=FIX(YRP%/64):    YRPL%=YRP% AND 63
'FORMAT POSITION OUTPUTS
3095        OUT 238,249: OUT 237,YRPM%: OUT 236,128: OUT 236,0
'Y-ROW MSH (Y-PIXEL MSH)
3096        OUT 238,250: OUT 237,YRPL%: OUT 236,128: OUT 236,0
'Y-ROW LSH (Y-PIXEL LSH)
3097        OUT 238,246: OUT 237,XRPM%: OUT 236,128: OUT 236,0
'X-ROW MSH (X-PIXEL MSH)
3098        OUT 238,247: OUT 237,XRPL%: OUT 236,128: OUT 236,0
'X-ROW LSH (X-PIXEL LSH)
3690    RETURN
4200    '*************************************************************
4210    'DRAW A LINE
4220    DX=XE%-XB%: DY=YE%-YB%
4221    DTG=0
4222    IF DX=0 AND DY=0 THEN 4228
4224    IF ABS(DX)>ABS(DY) THEN 4227
4226    YPS%=(DY*256)/ABS(DY): XPS%=(DX*256)/ABS(DY):
DTG=ABS(DY): GOTO 4228
4227    YPS%=(DY*256)/ABS(DX): XPS%=(DX*256)/ABS(DX):
DTG=ABS(DX)
4228    XRP%=XB%-8: YRP%=YB%-8
4255    GOSUB 3000
4270    OUT 238, 252: OUT 237, INT1%            'DATA TO LOAD IN
IMAGE MEMORY
4273    OUT 236,32              'SET SEQUENTIAL LOAD COMMAND
4274    DTG=DTG+8
4276    IF DTG>8 THEN 4288
4287    OUT 236,160: OUT 236,32: GOTO 4305
4288    FOR INLP1=8 TO DTG STEP 8               'PIXEL LOOP
4290    OUT 236,160: OUT 236,32
4300    NEXT INLP1
4305    OUT 236,0               'RESET SEQUENTIAL LOAD COMMAND
4350    RETURN
4400    '*************************************************************
4410    INIT1%=7: XB%=225: YB%=255: YPS%=0: XPS%=256
4420    FOR OUTLP1%=1 TO 10
4435    XRP%=XB%: YRP%=YB%
4437    XB%=XB%-1: YB%=YB%+1
4440    DX=2*OUTLP1%+1
4470    GOSUB 3000
4480    OUT 238, 252: OUT 237, INT1%            'DATA TO LOAD IN
IMAGE MEMORY
4484    OUT 236,32              'SET SEQUENTIAL LOAD COMMAND
4488    FOR INLP1=8 TO DX STEP 8                'PIXEL LOOP
4492    OUT 236,160: OUT 236,32
```

```
4495    OUT 236,0                'RESET SEQUENTIAL LOAD COMMAND
4496    NEXT OUTLP1%
4497    RETURN
4500    '*********************************************************
4510    'BLACK BACKGROUND WITH COORDINATE SYMBOLS
4520'   A5%=3:  INT1%=0:   XB%=0:    YB%=0:    XE%=511:  YE%=511:
GOSUB 630
4522    A5%=12: INT1%=3:   XB%=0:    YB%=0:    XE%=0:    YE%=511:
GOSUB 630
4523    A5%=12: INT1%=3:   XB%=0:    YB%=0:    XE%=511:  YE%=0:
GOSUB 630
4524    A5%=3:  INT1%=3:   XB%=252:  YB%=252:  XE%=258:  YE%=258:
GOSUB 630
4525    A5%=3:  INT1%=3:   XB%=250:  YB%=250:  XE%=260:  YE%=260:
GOSUB 630
4526    A5%=3:  INT1%=3:   XB%=0:    YB%=0:    XE%=10:   YE%=10:
GOSUB 630
4527    RETURN
4530    '*********************************************************
4531    'RECTANGLE AND LINE PATTERN
4540    A5%=3:  INT1%=24:  XB%=100:  YB%=400:  XE%=200:  YE%=500:
GOSUB 630
4550    A5%=1:             XB%=400:  YB%=100:  XE%=500:  YE%=200:
GOSUB 630
4555    A5%=10:            XB%=100:  YB%=100:  XE%=200:  YE%=200:
GOSUB 630
4556    A5%=12: INT1%=24:  XB%=0:    YB%=0:    XE%=511:  YE%=511:
GOSUB 630
4557    A5%=12: INT1%=24:  XB%=0:    YB%=511:  XE%=511:  YE%=0:
GOSUB 630
4561    RETURN
5500    '*********************************************************
5510    'SPIRAL LINES
5535    A5%=12: INT1%=24:  XB%=0:    YB%=0:    XE%=10000:
YE%=200:  GOSUB 630
5540    A5%=12: INT1%=96:  XB%=0:    YB%=511:  XE%=30000:
YE%=200:  GOSUB 630
5561    RETURN
6500    '*********************************************************
6520    A5%=3:  INT1%=96:  XB%=0:    YB%=0:    XE%=511:  YE%=511:
GOSUB 630
6530    A5%=3:  INT1%=24:  XB%=100:  YB%=500:  XE%=200:  YE%=400:
GOSUB 630
6550    A5%=1:             XB%=500:  YB%=100:  XE%=400:  YE%=200:
GOSUB 630
6560    A5%=10:            XB%=100:  YB%=100:  XE%=200:  YE%=200:
GOSUB 630
6561    RETURN
7500    '*********************************************************
7520    A5%=3:  INT1%=96:  XB%=0:    YB%=0:    XE%=511:  YE%=511:
GOSUB 630
7530    A5%=3:  INT1%=24:  XB%=100:  YB%=500:  XE%=200:  YE%=400:
GOSUB 630
7535    A5%=12: INT1%=24:  XB%=0:    YB%=0:    XE%=511:  YE%=511:
```

```
7540    A5%=12: INT1%=24:  XB%=0:    YB%=511:  XE%=511:  YE%=0:
GOSUB 630
7550    A5%=1:             XB%=500:  YB%=100:  XE%=400:  YE%=200:
GOSUB 630
7560    A5%=10:            XB%=100:  YB%=100:  XE%=200:  YE%=200:
GOSUB 630
7561    RETURN
8500    '*****************************************************
8520    A5%=3:  INT1%=96:  XB%=0:    YB%=0:    XE%=511:  YE%=511:
GOSUB 630
8530    A5%=3:  INT1%=24:  XB%=100:  YB%=500:  XE%=200:  YE%=400:
GOSUB 630
8535    A5%=12: INT1%=24:  XB%=0:    YB%=0:    XE%=511:  YE%=511:
GOSUB 630
8540    A5%=12: INT1%=24:  XB%=0:    YB%=511:  XE%=511:  YE%=0:
GOSUB 630
8550    A5%=1:             XB%=500:  YB%=100:  XE%=400:  YE%=200:
GOSUB 630
8560    A5%=10:            XB%=100:  YB%=100:  XE%=200:  YE%=200:
GOSUB 630
8561    RETURN
9000    '*************************************************************
9001    A5%=3:  INT1%=7:   XB%=128:  YB%=128:  XE%=256:  YE%=256:
GOSUB 630
9010    A5%=3:  INT1%=16:  XB%=256:  YB%=128:  XE%=384:  YE%=256:
GOSUB 630
9020    A5%=3:  INT1%=96:  XB%=256:  YB%=256:  XE%=384:  YE%=384:
GOSUB 630
9030    A5%=3:  INT1%=24:  XB%=128:  YB%=256:  XE%=256:  YE%=386:
GOSUB 630
9031    RETURN
9032    '*************************************************************
9040    A5%=3:  INT1%=32:  XB%=0:    YB%=0:    XE%=511:  YE%=511:
GOSUB 630
9050    A5%=3:  INT1%=7:   XB%=104:  YB%=104:  XE%=127:  YE%=407:
GOSUB 630
9060    A5%=3:  INT1%=7:   XB%=104:  YB%=104:  XE%=407:  YE%=127:
GOSUB 630
9070    A5%=3:  INT1%=7:   XB%=104:  YB%=384:  XE%=407:  YE%=407:
GOSUB 630
9080    A5%=3:  INT1%=7:   XB%=384:  YB%=104:  XE%=407:  YE%=407:
GOSUB 630
9090    A5%=3:  INT1%=24:  XB%=150:  YB%=150:  XE%=173:  YE%=361:
GOSUB 630
9100    A5%=3:  INT1%=24:  XB%=150:  YB%=150:  XE%=361:  YE%=173:
GOSUB 630
9110    A5%=3:  INT1%=24:  XB%=150:  YB%=338:  XE%=361:  YE%=361:
GOSUB 630
9120    A5%=3:  INT1%=24:  XB%=338:  YB%=150:  XE%=361:  YE%=361:
GOSUB 630
9130    A5%=3:  INT1%=96:  XB%=196:  YB%=196:  XE%=219:  YE%=315:
GOSUB 630
9140    A5%=3:  INT1%=96:  XB%=196:  YB%=196:  XE%=315:  YE%=219:
GOSUB 630
```

```
GOSUB 630
9160    A5%=3:  INT1%=96:  XB%=292:  YB%=196:  XE%=315:  YE%=315:
GOSUB 630
9170    A5%=3:  INT1%=7:   XB%=242:  YB%=242:  XE%=269:  YE%=269:
GOSUB 630
9171    RETURN
9172    '*************************************************************
9180    A5%=3:  INT1%=96:  XB%=0:    YB%=0:    XE%=511:  YE%=511:
GOSUB 630
9190    A5%=1:             XB%=96:   YB%=96:   XE%=159:  YE%=159:
GOSUB 630
9200    A5%=1:             XB%=352:  YB%=352:  XE%=415:  YE%=415:
GOSUB 630
9210    A5%=10:            XB%=96:   YB%=352:  XE%=159:  YE%=415:
GOSUB 630
9220    A5%=10:            XB%=352:  YB%=96:   XE%=415:  YE%=159:
GOSUB 630
9230    A5%=3:  INT1%=24:  XB%=224:  YB%=224:  XE%=287:  YE%=287:
GOSUB 630
9240    A5%=12: INT1%=7:   XB%=159:  YB%=159:  XE%=224:  YE%=224:
GOSUB 630
9250    A5%=12: INT1%=7:   XB%=287:  YB%=287:  XE%=352:  YE%=352:
GOSUB 630
9260    A5%=12: INT1%=7:   XB%=159:  YB%=352:  XE%=224:  YE%=287:
GOSUB 630
9270    A5%=12: INT1%=7:   XB%=287:  YB%=224:  XE%=352:  YE%=159:
GOSUB 630
9271    RETURN
9272    '*************************************************************
9280    A5%=3:  INT1%=96:  XB%=0:    YB%=0:    XE%=511:  YE%=511:
GOSUB 630
9300    A5%=12: INT1%=7:   XB%=5:    YB%=6:    XE%=252:  YE%=253:
GOSUB 630
9310    A5%=12: INT1%=7:   XB%=259:  YB%=260:  XE%=506:  YE%=507:
GOSUB 630
9320    A5%=12: INT1%=7:   XB%=5:    YB%=507:  XE%=252:  YE%=260:
GOSUB 630
9330    A5%=12: INT1%=7:   XB%=259:  YB%=253:  XE%=506:  YE%=6:
GOSUB 630
9340    A5%=12: INT1%=96:  XB%=5:    YB%=5:    XE%=252:  YE%=252:
GOSUB 630
9350    A5%=12: INT1%=96:  XB%=259:  YB%=259:  XE%=506:  YE%=506:
GOSUB 630
9360    A5%=12: INT1%=96:  XB%=5:    YB%=506:  XE%=252:  YE%=259:
GOSUB 630
9370    A5%=12: INT1%=96:  XB%=259:  YB%=252:  XE%=506:  YE%=5:
GOSUB 630
9380    A5%=12: INT1%=24:  XB%=5:    YB%=4:    XE%=252:  YE%=251:
GOSUB 630
9390    A5%=12: INT1%=24:  XB%=259:  YB%=258:  XE%=506:  YE%=505:
GOSUB 630
9400    A5%=12: INT1%=24:  XB%=5:    YB%=505:  XE%=252:  YE%=258:
GOSUB 630
9410    A5%=12: INT1%=24:  XB%=259:  YB%=251:  XE%=506:  YE%=4:
```

```
9420    A5%=3:  INT1%=7:   XB%=0:    YB%=0:    XE%=511:  YE%=0:
GOSUB 630
9430    A5%=3:  INT1%=7:   XB%=0:    YB%=0:    XE%=0:    YE%=511:
GOSUB 630
9440    A5%=3:  INT1%=7:   XB%=511:  YB%=0:    XE%=511:  YE%=511:
GOSUB 630
9450    A5%=3:  INT1%=7:   XB%=0:    YB%=511:  XE%=511:  YE%=511:
GOSUB 630
9460    A5%=3:  INT1%=96:  XB%=1:    YB%=1:    XE%=510:  YE%=1:
GOSUB 630
9470    A5%=3:  INT1%=96:  XB%=1:    YB%=1:    XE%=1:    YE%=510:
GOSUB 630
9480    A5%=3:  INT1%=96:  XB%=510:  YB%=1:    XE%=510:  YE%=510:
GOSUB 630
9490    A5%=3:  INT1%=96:  XB%=1:    YB%=510:  XE%=510:  YE%=510:
GOSUB 630
9500    A5%=3:  INT1%=24:  XB%=2:    YB%=2:    XE%=509:  YE%=2:
GOSUB 630
9510    A5%=3:  INT1%=24:  XB%=2:    YB%=2:    XE%=2:    YE%=509:
GOSUB 630
9520    A5%=3:  INT1%=24:  XB%=509:  YB%=2:    XE%=509:  YE%=509:
GOSUB 630
9530    A5%=3:  INT1%=24:  XB%=2:    YB%=509:  XE%=509:  YE%=509:
GOSUB 630
9540    A5%=3:  INT1%=7:   XB%=3:    YB%=3:    XE%=508:  YE%=3:
GOSUB 630
9550    A5%=3:  INT1%=7:   XB%=3:    YB%=3:    XE%=3:    YE%=508:
GOSUB 630
9560    A5%=3:  INT1%=7:   XB%=508:  YB%=3:    XE%=508:  YE%=508:
GOSUB 630
9570    A5%=3:  INT1%=7:   XB%=3:    YB%=508:  XE%=508:  YE%=508:
GOSUB 630
9580    A5%=3:  INT1%=96:  XB%=4:    YB%=4:    XE%=507:  YE%=4:
GOSUB 630
9590    A5%=3:  INT1%=96:  XB%=4:    YB%=4:    XE%=4:    YE%=507:
GOSUB 630
9600    A5%=3:  INT1%=96:  XB%=507:  YB%=4:    XE%=507:  YE%=507:
GOSUB 630
9610    A5%=3:  INT1%=96:  XB%=4:    YB%=507:  XE%=507:  YE%=507:
GOSUB 630
9620    A5%=3:  INT1%=24:  XB%=5:    YB%=5:    XE%=506:  YE%=5:
GOSUB 630
9630    A5%=3:  INT1%=24:  XB%=5:    YB%=5:    XE%=5:    YE%=506:
GOSUB 630
9640    A5%=3:  INT1%=24:  XB%=506:  YB%=5:    XE%=506:  YE%=506:
GOSUB 630
9650    A5%=3:  INT1%=24:  XB%=5:    YB%=506:  XE%=506:  YE%=506:
GOSUB 630
9660    A5%=12: INT1%=7:   XB%=192:  YB%=128:  XE%=319:  YE%=128:
GOSUB 630
9670    A5%=12: INT1%=96:  XB%=193:  YB%=129:  XE%=318:  YE%=129:
GOSUB 630
9680    A5%=12: INT1%=24:  XB%=194:  YB%=130:  XE%=317:  YE%=130:
GOSUB 630
```

```
GOSUB 630
9700    A5%=12: INT1%=96:  XB%=201:  YB%=137:  XE%=310:  YE%=137:
GOSUB 630
9710    A5%=12: INT1%=24:  XB%=202:  YB%=138:  XE%=309:  YE%=138:
GOSUB 630
9720    A5%=12: INT1%=7:   XB%=208:  YB%=144:  XE%=303:  YE%=144:
GOSUB 630
9730    A5%=12: INT1%=96:  XB%=209:  YB%=145:  XE%=302:  YE%=145:
GOSUB 630
9740    A5%=12: INT1%=24:  XB%=210:  YB%=146:  XE%=301:  YE%=146:
GOSUB 630
9750    A5%=12: INT1%=7:   XB%=216:  YB%=152:  XE%=295:  YE%=152:
GOSUB 630
9760    A5%=12: INT1%=96:  XB%=217:  YB%=153:  XE%=294:  YE%=153:
GOSUB 630
9770    A5%=12: INT1%=24:  XB%=218:  YB%=154:  XE%=293:  YE%=154:
GOSUB 630
9780    A5%=12: INT1%=7:   XB%=224:  YB%=160:  XE%=287:  YE%=160:
GOSUB 630
9790    A5%=12: INT1%=96:  XB%=225:  YB%=161:  XE%=286:  YE%=161:
GOSUB 630
9800    A5%=12: INT1%=24:  XB%=226:  YB%=162:  XE%=285:  YE%=162:
GOSUB 630
9810    A5%=12: INT1%=7:   XB%=232:  YB%=168:  XE%=279:  YE%=168:
GOSUB 630
9820    A5%=12: INT1%=96:  XB%=233:  YB%=169:  XE%=278:  YE%=169:
GOSUB 630
9830    A5%=12: INT1%=24:  XB%=234:  YB%=170:  XE%=277:  YE%=170:
GOSUB 630
9840    A5%=12: INT1%=7:   XB%=240:  YB%=176:  XE%=271:  YE%=176:
GOSUB 630
9850    A5%=12: INT1%=96:  XB%=241:  YB%=177:  XE%=270:  YE%=177:
GOSUB 630
9860    A5%=12: INT1%=24:  XB%=242:  YB%=178:  XE%=269:  YE%=178:
GOSUB 630
9870    A5%=12: INT1%=7:   XB%=248:  YB%=184:  XE%=263:  YE%=184:
GOSUB 630
9890    A5%=12: INT1%=96:  XB%=249:  YB%=185:  XE%=262:  YE%=185:
GOSUB 630
9900    A5%=12: INT1%=24:  XB%=250:  YB%=186:  XE%=261:  YE%=186:
GOSUB 630
9910    A5%=3:  INT1%=7:   XB%=255:  YB%=192:  XE%=256:  YE%=192:
GOSUB 630
9920    A5%=3:  INT1%=7:   XB%=255:  YB%=420:  XE%=256:  YE%=420:
GOSUB 630
9930    A5%=12: INT1%=7:   XB%=250:  YB%=426:  XE%=261:  YE%=426:
GOSUB 630
9940    A5%=12: INT1%=96:  XB%=249:  YB%=427:  XE%=262:  YE%=427:
GOSUB 630
9950    A5%=12: INT1%=24:  XB%=248:  YB%=428:  XE%=263:  YE%=428:
GOSUB 630
9960    A5%=12: INT1%=7:   XB%=242:  YB%=434:  XE%=269:  YE%=434:
GOSUB 630
9970    A5%=12: INT1%=96:  XB%=241:  YB%=435:  XE%=270:  YE%=435:
GOSUB 630
```

```
9980    A5%=12: INT1%=24:  XB%=240:  YB%=436:  XE%=271:  YE%=436:
GOSUB 630
9990    A5%=12: INT1%=7:   XB%=234:  YB%=442:  XE%=277:  YE%=442:
GOSUB 630
10000   A5%=12: INT1%=96:  XB%=233:  YB%=443:  XE%=278:  YE%=443:
GOSUB 630
10010   A5%=12: INT1%=24:  XB%=232:  YB%=444:  XE%=279:  YE%=444:
GOSUB 630
10020   A5%=12: INT1%=7:   XB%=226:  YB%=450:  XE%=285:  YE%=450:
GOSUB 630
10030   A5%=12: INT1%=96:  XB%=225:  YB%=451:  XE%=286:  YE%=451:
GOSUB 630
10040   A5%=12; INT1%=24:  XB%=224:  YB%=452:  XE%=287:  YE%=452:
GOSUB 630
10050   A5%=12: INT1%=7:   XB%=218:  YB%=458:  XE%=293:  YE%=458:
GOSUB 630
10060   A5%=12: INT1%=96:  XB%=217:  YB%=459:  XE%=294:  YE%=459:
GOSUB 630
10070   A5%=12: INT1%=24:  XB%=216:  YB%=460:  XE%=295:  YE%=460:
GOSUB 630
10080   A5%=12: INT1%=7:   XB%=210:  YB%=466:  XE%=301:  YE%=466:
GOSUB 630
10090   A5%=12: INT1%=96:  XB%=209:  YB%=467:  XE%=302:  YE%=467:
GOSUB 630
11000   A5%=12: INT1%=24:  XB%=208:  YB%=468:  XE%=303:  YE%=468:
GOSUB 630
11010   A5%=12: INT1%=7:   XB%=202:  YB%=474:  XE%=309:  YE%=474:
GOSUB 630
11020   A5%=12: INT1%=96:  XB%=201:  YB%=475:  XE%=310:  YE%=475:
GOSUB 630
11030   A5%=12: INT1%=24:  XB%=200:  YB%=476:  XE%=311:  YE%=476:
GOSUB 630
11040   A5%=12: INT1%=7:   XB%=194:  YB%=482:  XE%=317:  YE%=482:
GOSUB 630
11050   A5%=12: INT1%=96:  XB%=193:  YB%=483:  XE%=318:  YE%=483:
GOSUB 630
11059   A5%=12: INT1%=24:  XB%=192:  YB%=484:  XE%=319:  YE%=484:
GOSUB 630
11060   A5%=3:  INT1%=24:  XB%=248:  YB%=248:  XE%=263:  YE%=263:
GOSUB 630
11061   RETURN
11062   '*************************************************************
11070   A5%=3:  INT1%=7:   XB%=0:    YB%=0:    XE%=511:  YE%=256:
GOSUB 630
11080   A5%=3:  INT1%=96:  XB%=0:    YB%=256:  XE%=511:  YE%=511:
GOSUB 630
11090   A5%=3:  INT1%=24:  XB%=256:  YB%=128:  XE%=352:  YE%=256:
GOSUB 630
12000   A5%=3:  INT1%=16:  XB%=352:  YB%=128:  XE%=432:  YE%=256:
GOSUB 630
12010   A5%=12: INT1%=0:   XB%=256:  YB%=256:  XE%=296:  YE%=296:
GOSUB 630
12020   A5%=12: INT1%=0:   XB%=256:  YB%=255:  XE%=296:  YE%=295:
GOSUB 630
```

```
GOSUB 630
12040   A5%=12: INT1%=0:   XB%=296:  YB%=296:  XE%=392:  YE%=296:
GOSUB 630
12050   A5%=12: INT1%=0:   XB%=296:  YB%=295:  XE%=392:  YE%=295:
GOSUB 630
12060   A5%=12: INT1%=0:   XB%=296:  YB%=397:  XE%=392:  YE%=297:
GOSUB 630
12070   A5%=12: INT1%=0:   XB%=392:  YB%=296:  XE%=352:  YE%=256:
GOSUB 630
12080   A5%=12: INT1%=0:   XB%=392:  YB%=295:  XE%=352:  YE%=255:
GOSUB 630
12090   A5%=12: INT1%=0:   XB%=392:  YB%=297:  XE%=352:  YE%=257:
GOSUB 630
13000   A5%=12: INT1%=0:   XB%=256:  YB%=256:  XE%=352:  YE%=256:
GOSUB 630
13010   A5%=12: INT1%=0:   XB%=256:  YB%=255:  XE%=352:  YE%=255:
GOSUB 630
13020   A5%=12: INT1%=0:   XB%=256:  YB%=257:  XE%=352:  YE%=257:
GOSUB 630
13030   A5%=12: INT1%=0:   XB%=256:  YB%=128:  XE%=256:  YE%=256:
GOSUB 630
13040   A5%=12: INT1%=0:   XB%=256:  YB%=127:  XE%=256:  YE%=255:
GOSUB 630
13050   A5%=12: INT1%=0:   XB%=256:  YB%=129:  XE%=256:  YE%=257:
GOSUB 630
13060   A5%=12: INT1%=0:   XB%=256:  YB%=128:  XE%=432:  YE%=128:
GOSUB 630
13070   A5%=12: INT1%=0:   XB%=256:  YB%=127:  XE%=432:  YE%=127:
GOSUB 630
13080   A5%=12: INT1%=0:   XB%=256:  YB%=129:  XE%=432:  YE%=129:
GOSUB 630
13090   A5%=12: INT1%=0:   XB%=352:  YB%=128:  XE%=352:  YE%=256:
GOSUB 630
14000   A5%=12: INT1%=0:   XB%=352:  YB%=127:  XE%=352:  YE%=255:
GOSUB 630
14010   A5%=12: INT1%=0:   XB%=352:  YB%=129:  XE%=352:  YE%=257:
GOSUB 630
14020   A5%=12: INT1%=0:   XB%=392:  YB%=296:  XE%=432:  YE%=256:
GOSUB 630
14030   A5%=12: INT1%=0:   XB%=392:  YB%=295:  XE%=432:  YE%=255:
GOSUB 630
14040   A5%=12: INT1%=0:   XB%=392:  YB%=297:  XE%=432:  YE%=257:
GOSUB 630
14050   A5%=12: INT1%=0:   XB%=432:  YB%=256:  XE%=432:  YE%=128:
GOSUB 630
14060   A5%=12: INT1%=0:   XB%=432:  YB%=255:  XE%=432:  YE%=127:
GOSUB 630
14070   A5%=12: INT1%=0:   XB%=432:  YB%=257:  XE%=432:  YE%=129:
GOSUB 630
14080   A5%=12: INT1%=127: XB%=12:   YB%=480:  XE%=12:   YE%=496:
GOSUB 630
14090   A5%=12: INT1%=127: XB%=12:   YB%=496:  XE%=16:   YE%=500:
GOSUB 630
15000   A5%=12: INT1%=127: XB%=16:   YB%=500:  XE%=32:   YE%=500:
```

```
15010   A5%=12: INT1%=127: XB%=32:   YB%=500:  XE%=36:   YE%=496:
GOSUB 630
15020   A5%=12: INT1%=127: XB%=36:   YB%=496:  XE%=36:   YE%=480:
GOSUB 630
15030   A5%=12: INT1%=127: XB%=36:   YB%=480:  XE%=32:   YE%=476:
GOSUB 630
15040   A5%=12: INT1%=127: XB%=32:   YB%=476:  XE%=16:   YE%=476:
GOSUB 630
15050   A5%=12: INT1%=127: XB%=16:   YB%=476:  XE%=12:   YE%=480:
GOSUB 630
15060   A5%=12: INT1%=127: XB%=6:    YB%=476:  XE%=12:   YE%=480:
GOSUB 630
15070   A5%=12: INT1%=127: XB%=6:    YB%=500:  XE%=12:   YE%=496:
GOSUB 630
15080   A5%=12: INT1%=127: XB%=12:   YB%=506:  XE%=16:   YE%=500:
GOSUB 630
15090   A5%=12: INT1%=127: XB%=36:   YB%=506:  XE%=32:   YE%=500:
GOSUB 630
16000   A5%=12: INT1%=127: XB%=42:   YB%=500:  XE%=36:   YE%=496:
GOSUB 630
16010   A5%=12: INT1%=127: XB%=36:   YB%=470:  XE%=32:   YE%=476:
GOSUB 630
16020   A5%=12: INT1%=127: XB%=12:   YB%=470:  XE%=16:   YE%=476:
GOSUB 630
16030   A5%=12: INT1%=127: XB%=42:   YB%=476:  XE%=36:   YE%=480:
GOSUB 630
16031   RETURN
16032   '*************************************************************
40000   END
```

BASIC PROGRAM LISTING

FTR.ASC

```
10      LPRINT "FTR2.ASC"        '8/15/84          REV.8/22/4    09:30"
20      'PREFILTER THE DATABASE IMAGE
30              OPEN "R", #1, "PRESENT.BIN",128
40              FIELD 1,128 AS IA$
50      'SET UP INTEGETER CONSTANTS FOR SPEED
60      K1=1/256
70      K2=1/8
80      K3=1/32
90      RC1=0    'INITIALIZE TO ZERO
100     F5%=66          'INPUT "NUMBER OF LINES TO BE
FILTERED";F5%
110 '   INPUT "ENABLE SMOOTHING PRINTOUTS; 'Y' OR 'N'"; A15$
120 '   INPUT "ENABLE STORING PRINTOUTS; 'Y' OR 'N'"; A16$
130 '   PRINT   "SELECT FIXED WEIGHTS"
140 '   INPUT   "   SELECT STANDARD WEIGHTS;  'Y' OR 'N'"; A1$
150 '   IF A1$ = "N" THEN 680
160 '   PRINT: PRINT
170 '   PRINT "   SELECT", "  1  ",  "  2  ",  "  3  ": PRINT
180 '   PRINT           , "2 4 2",  "4 6 4",  "8 8 8"
190 '   PRINT           , "4 8 4",  "6 8 6",  "8 8 8"
200 '   PRINT           , "2 4 2",  "4 6 4",  "8 8 8"
210     A1%=3    'PRINT: INPUT "SELECT WEIGHTS '1', '2', OR '3'";A1%
220     ON A1% GOTO 260, 290, 320
230     PRINT "*****************************"
240     PRINT "IMPROPER WEIGHT SELECTION, MAKE ANOTHER SELECTION"
250     PRINT "*****************************"; PRINT: PRINT: PRINT:
GOTO 130
260     W1% = 2: W2% = 4: W3% = 2                    'WEIGHT KERNEL 1
270     W4% = 4: W5% = 8: W6% = 4
280     W7% = 2: W8% = 4: W9% = 2: GOTO 390
290     W1% = 4: W2% = 6: W3% = 4                    'WEIGHT KERNEL 2
300     W4% = 6: W5% = 8: W6% = 6
310     W7% = 4: W8% = 6: W9% = 4: GOTO 390
320     W1% = 8: W2% = 8: W3% = 8                    'WEIGHT KERNEL 3
330     W4% = 8: W5% = 8: W6% = 8
340     W7% = 8: W8% = 8: W9% = 8: GOTO 390
350     PRINT: PRINT    "INPUT FIXED WEIGHTS"
360     INPUT   "INPUT WEIGHTS; W1, W2, W3"; W1%, W2%, W3%
370     INPUT   "INPUT WEIGHTS; W4, W5, W6"; W4%, W5%, W6%
380     INPUT   "INPUT WEIGHTS; W7, W8, W9"; W7%, W8%, W9%
390     WTS1%=W1%+W2%+W3%+W4%+W5%+W6%+W7%+W8%+W9%       'WEIGHT
SCALE FACTOR
400     WTS2=1/WTS1%                                 'RECIPROCAL
WEIGHT SCALE FACTOR
410     PRINT: PRINT ,"  WEIGHTS SELECTED": PRINT
420     PRINT ,"W1=";W1%, "W2=";W2%, "W3=";W3%
430     PRINT ,"W4=";W4%, "W5=";W5%, "W6=";W6%
440     PRINT ,"W7=";W7%, "W8=";W8%, "W9=";W9%, "WTS1=";WTS1%: PRINT
450     WRR2% = 0: WRG2% = 0: WRB2% = 0: S1%=0: S2%=0
460     FOR KRLP1% = 1 TO F5%    'KERNEL ROW LOOP
465     IF KRLP1% > 1 THEN TST$="Y" ELSE TST$="N"
470     LPRINT "START KERNEL ROW=";KRLP1%
480     FOR KPLP1% = 1 TO 512    'KERNEL PIXEL LOOP
```

```
510     XE% = XB% + 2: YE% = YB% + 2
520     X = (XB%/128)  'FIND PIXEL COORDINATE FOR RECORD LOCATION
530     BDC = XB%: IF BDC <=128 THEN 570
540     BDC = ABS(BDC-128)       'FIND BEGINNING DATA COUNT IN RECORD
550     'IF TST$ = "Y" THEN PRINT "PIXEL LOOP ";KPLP1%
560     IF BDC>128 THEN GOTO 540
570     FOR OUTLP1% = YB% TO YE%         'LINE LOOP
580     OUT 236,1
590     GOSUB 1820
600     GOSUB 2180       'DEFINE RECORD NO.
610     'IF TST$ = "Y" THEN PRINT "OUTLP1% ";OUTLP1%
620     'IF TST$ = "Y" THEN PRINT "RC ";RC
630     IF (RC >4) AND (RC < 261) THEN 640 ELSE 710
640     RC = RC-4        'SUBTRACT 4 SO LINES GO FROM 1-64
650     IF TOGL$="T" THEN 660 ELSE 860
660       CLOSE #1
670       OPEN "R",#1,"PRESENT.BIN",128 'REOPEN PRESENT FILE IF ANOTHER
680       FIELD 1,128 AS IA$     ' FILE WAS USED
690       TOGL$="F"
700     GOTO 860
710     IF RC < 5 THEN 720 ELSE 790
720     'GET RECORD FROM PREVIOUS FILE
730       CLOSE #1
740       OPEN "R",#1,"PRIOR.BIN",128
750       FIELD 1,128 AS IA$
760       TOGL$ = "T"    'FILE MUST BE OPEN FOR INNER LOOP
770       RC=252+RC      'SET RC TO LAST LINE IN PRIOR FILE
780       GOTO 860       'GET RECORD FROM FILE
790     'ELSE
800     'GET RECORD FROM NEXT FILE
810       CLOSE #1
820       OPEN "R",#1,"NEXT.BIN",128
830       FIELD 1,128 AS IA$
840       TOGL$ = "T"    'FILE MUST BE OPEN FOR INNER LOOP
850       RC=RC-260      'SET RC TO FIRST LINE IN NEXT ;FILE
860     GET #1,RC
870     FOR INLP1% = XB% TO XE% STEP 2  'PIXEL LOOP
880     OUT 236,1: OUT 236,0
890     '        CHECK FOR EVEN BYTE STARTING ADDRESS
900     IF A15$="Y" THEN GOSUB 1970
910       IF (INLP1% = XB% ) AND ((XB% MOD 2) = 0)  THEN DC=BDC-1
920       IF (INLP1% = XB% ) AND ((XB% MOD 2) <> 0) THEN DC = BDC
930      A$=MID$(IA$,DC,2) :' GET 2 BYTES
940 'X    IF CVI(A$) = 0 THEN K%=0: GOTO 1220
950      K% = CVI(A$)
960      PIXA% = K% AND 255 : ' GET FIRST BYTE
970      PIXB% = K% * K1 : 'GET SECOND BYTE
975     'IF TST$ = "Y" THEN PRINT "PIXA%, PIXB% ";PIXA%,PIXB%
980 'X  OUT 236,16: OUT 236,0
990     ' UNPACK RED, GREEN, AND BLUE INTENSITIES
1000    IF S1%=0 THEN 1010 ELSE 1020
1010    RDG2%=PIXB% AND 7: RDR2%=(PIXB% AND 24)*K2: RDB2%=(PIXB%
AND 96)*K3
```

```
1030 'X OUT 236,16: OUT 236,0
1040    S3%=OUTLP1%-YB%+1: ON S3% GOTO 1060, 1070, 1080
1050            LPRINT "ERROR AT LINE 1610
1060            WS1%=W1%: WS2%=W2%: WS3%=W3%: GOTO 1090
1070            WS1%=W4%: WS2%=W5%: WS3%=W6%: GOTO 1090
1080            WS1%=W7%: WS2%=W8%: WS3%=W9%
1090 'X OUT 236,16: OUT 236,0
1100    IF S1%=0 THEN 1140
1110    WRR2% = RDR1%*WS3% + WRR2%
1120    WRG2% = RDG1%*WS3% + WRG2%
1130    WRB2% = RDB1%*WS3% + WRB2%:                    GOTO 1170
1140    WRR2% = RDR1%*WS1% + RDR2%*WS2% + WRR2%
1150    WRG2% = RDG1%*WS1% + RDG2%*WS2% + WRG2%
1160    WRB2% = RDB1%*WS1% + RDB2%*WS2% + WRB2%: S1%=1
1170 'X OUT 236,16: OUT 236,0
1180    DC=DC+2: IF DC>=128 THEN 1190 ELSE 1200 'UPDATE DATA COUNT
1190    DC=1: RC=RC+1: GET #1,RC          'CONDITIONALLY UPDATE
RECORD COUNT
1200    NEXT INLP1%
1210    S1%=0
1220    NEXT OUTLP1%
1230    OUT 236,16
1240    IF S2%>0 THEN 1280
1250    S2%=1
1260    WRR1%=WRR2%*WTS2: WRG1%=WRG2%*WTS2: WRB1%=WRB2%*WTS2
1270    IF A15$="Y" THEN GOSUB 1270: GOTO 1310
1280    WRR2%=WRR2%*WTS2: WRG2%=WRG2%*WTS2: WRB2%=WRB2%*WTS2
1290    IF A15$="Y" THEN GOSUB 2000
1300    S2%=0: GOSUB 1410                  'STORE
1310    WRR2%=0: WRG2%=0: WRB2%=0
1320    OUT 236,0
1330    NEXT KPLP1%
1340    NEXT KRLP1%
1350'   CLOSE #1
1360'   OPEN "R",#2,"FILTERED.BIN",128
1370'   FIELD 2,128 AS IB$
1380'   PUT #2,RC1
1390    CLOSE
1400    SYSTEM
1410
'-----------------------------------------------------------------
1420    '
1430    '       CODE TO PUT NEW BYTES TO SPECIFIED WRITE FILE
1440    '          THE NEW BYTES SHOULD BE IN THE WRITE VARIABLES
1450    '
1460    '       CLOSE READ FILE AND OPEN WRITE FILE
1470    '
1480    '
1490    '   CALCULATIONS FOR EXACT PIXEL LOCATION
1500    XX=XB%:  YY=YB%
1510    X = (XX/128) : 'FIND PIXEL COORDINATE FOR RECORD LOCATION
1520    BDC = XX: IF BDC <=128 THEN 1550          'MODULO 128
1530    BDC = ABS(BDC-128)      :'FIND BEGINNING DATA COUNT IN RECORD
```

```
1560     OUTLP1%=YY
1570     GOSUB 2180        'GET RECORD NO.
1580     'RC0=RC
1590     'IF TST$ = "Y" THEN PRINT "RC1, RC0 ";RC1,RC0
1600     'IF RC1 = RC0 THEN 1710
1610     CLOSE #1
1620     OPEN "R",#2,"FILTERED.BIN",128
1630     FIELD 2,128 AS IB$
1640     'IF RC1=0 THEN 1660
1645      ' IB$=IB2$
1650       'PUT #2,RC1: 'PRINT "EXECUTED PUT ";CVI(IB$)
1660       GET #2,RC
1665     'IB2$=IB$
1670     'RC1 = RC0
1680     'CLOSE #2
1690     'OPEN "R",#1,"PRESENT.BIN",128
1700     'FIELD 1,128 AS IA$
1710      ' PACK RED, GREEN, BLUE COLORS INTO THEIR RESPECTIVE BYTES
1720            WR1% = WRG1% OR 8 * WRR1%
1730            WR1% = WR1% OR 32 * WRB1%
1740            WR2% = WRG2% OR 8 * WRR2%
1750            WR2% = WR2% OR 32 * WRB2%
1760      N3 = (WR2%*256) OR WR1%          ' PACK 2 BYTES INTO 1 WORD
1770       A$ = MKI$(N3)
1780       'PRINT "N3 ";N3
1790       MID$(IB$,DC2,2)=A$
1795       'PRINT "A$ ";CVI(A$)
1796       PUT #2,RC
1797     CLOSE #2
1798     OPEN "R",#1,"PRESENT.BIN",128
1799     FIELD 1,128 AS IA$
1800     RETURN
1810     '
1820
'*****************************************************************
1830     'SUBROUTINE TO INTERROGATE TERMINAL
1840     A7%=INP (93):  A8%=INP (92)
1850     A7%=A7% AND 2: IF A7%=0 THEN 1940        'DATA READY TEST
1860     A8%=A8% AND 127                          'MASK PARITY BIT
1870     A9%=A8% XOR 127: IF A9%=0 THEN 1930 ELSE 1940    'DELETE TO CP
1880     CLOSE #1
1890     OPEN "R",#2,"FILTERED.BIN",128
1900     FIELD 2,128 AS IB$
1910     PUT #2,RC1
1920     CLOSE
1930         SYSTEM
1940     RETURN
1950
'*****************************************************************
1960     '*******
1970     LPRINT: LPRINT: LPRINT "LINE 342": GOTO 2030
1980     '*******
1990     LPRINT: LPRINT: LPRINT "LINE 1265": GOTO 2030
```

```
2020     '********
2030     LPRINT "KRLP1=";KRLP1%, "KPLP1=";KPLP1%,
"OUTLP1=";OUTLP1%, "INLP1=";INLP1%
2040     LPRINT "XB=";XB%, "YB=";YB%, "XE=";XE%, "YE=";YB%
2050     LPRINT "DC=";DC, "RC=";RC, "S1=";S1%, "S2=";S2%, "S3=";S3%
2060     LPRINT "RDG1=";RDG1%, "RDR1=";RDR1%, "RDB1=";RDB1%
2070     LPRINT "RDG2=";RDG2%, "RDR2=";RDR2%, "RDB2=";RDB2%
2080     LPRINT "WRG1=";WRG1%, "WRR1=";WRR1%, "WRB1=";WRB1%
2090     LPRINT "WRG2=";WRG2%, "WRR2=";WRR2%, "WRB2=";WRB2%
2100     LPRINT "WS1=";WS1%,   "WS2=";WS2%,   "WS3=";WS3%
2110     RETURN
2120
'*************************************************************************
2130     LPRINT : LPRINT : LPRINT "LINE 236"
2140     LPRINT "W1=";W1%, "W2=";W2%, "W3=";W3%
2150     LPRINT "W4=";W4%, "W5=";W5%, "W6=";W6%
2160     LPRINT "W7=";W7%, "W8=";W8%, "W9=";W9% : RETURN
2170
'*************************************************************************
2180          'DEFINE RECORD NO.
2190       RC = ((OUTLP1%-1)*4)+1          '4-RECORDS/LINE, RECORD-
1 TO RECORD-4
2200       IF (X>1) AND (X<=2) THEN RC=RC+1   'CHECK FOR PIXEL
OVERFLOWING A RECORD
2210       IF (X>2) AND (X<=3) THEN RC=RC+2
2220       IF (X>3) THEN RC=RC+3
2230     RETURN
2240     END
```

DISCLOSURE DOCUMENT

A disclosure document has been filed in the U. S. Patent and Trademark Office on October 17, 1984 NO. 131,747, which is herein incorporated by reference. This disclosure document has copies of many of the documents and specification sheets referenced herein as follows.

1. National Semiconductor specification sheet for the MM5321 synchronization generator.

2. Signetics specification sheet for the 8T95, 96, 97, 98 hex buffers/inverters.

3. National Semiconductor specification sheet for the ADC 0800 A/D convertar.

4. Texas Instruments specification sheet for the TMS-4016 RAM.

5. TRW specification sheet for the TDC1016J-8, TDC1016J-9, TDC1016J-10 video D/A converters.

6. Mitsubishi Electric specification sheet for the M58725P, S;P-15, S-15, RAMs.

7. Computer Compatible Joystick Instruction sheet.

8. CompuPro CPU 8085/88 Technical Manual.

9. Viewpoint/3A Plus User's Manual.

10. CompuPro RAM 17 Technical Manual.

11. CompuPro RAM 16 Technical Manual.

12. CompuPro 8080 Multi-User Monitor program listing.

13. CompuPro System Support 1 User Manual.

14. International Instrumentation Incremental [illegible]

15. Siemens OEM Floppy Disk Drive FDD 100-8 manual.

16. CompuPro Disk 1 User Manual.

* * * * * * *

MAIL ROOM
JUN 6 1995
PAT. & TRADEMARK OFF.

ABSTRACT

An improved memory architecture is provided having advantages of increased speed, lower cost, and efficiancy of implementation. Information stored in memory can be scanned out at a rate greater than the addressing rate associated with the memories. This permits higher speed operation with lower cost memories. Use of an output buffer, such as a FIFO, permits normalization of memory clock rates. A multiple buffer output arrangement provides a means and method for obtaining multiple buffer capability, such as double buffer capability, with reduced memory requirements and provides a means and method for multiple use of accessed information without the need for re-accessing the information from the main memory. A detailed implementation of an image processing system having spatial filter processing is provided to illustrate high speed image processing with lower speed memory accesses.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	
GILBERT P. HYATT	Group Art Unit: Not yet assigned
Serial No. Not yet assigned	Examiner: Not yet assigned
Docket No. 516	
Filed: Not yet assigned	
For: IMPROVED MEMORY ARCHITECTURE HAVING A MULTIPLE BUFFER OUTPUT ARRANGEMENT	

DECLARATION CLAIMING SMALL ENTITY STATUS

Hon. Assistant Commissioner For Patents
Washington, D.C. 20231

Sir:

I hereby declare that, as the inventor in the above referenced application, I qualify as an independent inventor as defined in 37 CFR 1.9(c) for purposes of paying reduced fees under section 41(a) and 41(b) of Title 35, United States Code, to the Patent and Trademark Office with regard to the invention identified above. I have not assigned, granted, conveyed, or licensed and am under no obligation under contract or law to assign, grant, convey, or license any rights in the instant application to any person who could not be classified as an independent inventor under 3 CFR 1.9(c) if that person had made the invention or to a concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such a willful false statement may jeopardize the validity of the application or any patent issuing thereon.

CERTIFICATION OF MAILING BY EXPRESS MAIL: I hereby certify that this correspondence is being deposited with the United States Postal Service with Express Mail post office to addressee service under 37 CFR 1.10, postage prepaid, is a package addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231 with the express mail label number EB-185-850-515 on the date set forth below.

Respectfully submitted,

Dated: June 6, 1995

Gilbert P. Hyatt
Registration No. 27,647
P.O. Box 81230
Las Vegas, NV 89180
Phone (702) 871-9899

DECLARATION FOR PATENT APPLICATION

As the below named inventor, I hereby declare as follows.

I am a citizen of the United States of America residing in Las Vegas, Nevada.

I believe I am the original, first, and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled IMPROVED MEMORY ARCHITECTURE HAVING A MULTIPLE BUFFER OUTPUT ARRANGEMENT, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I do not claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign applications for patent or inventor's certificate.

I hereby claim the benefit under Title 35, United States Code, Section 120 of my earlier filed United States patent applications listed below:

Serial No.	Filed	Status
06/849,243	April 7, 1986	Pending
08/_____	April ___, 1995	Pending
07/774,159	October 15, 1991	Pending
06/661,649	October 17, 1984	Abandoned
06/662,211	October 18, 1984	Abandoned
07/815,644	December 30, 1991	Abandoned
08/034,627	March 22, 1993	Pending
07/279,592	December 2, 1988	Pending

and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application(s) in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose information which is material to patentability as defined Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the filing date of this application.

Address all telephone calls to Gilbert P. Hyatt at (702) 871-8888

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

CERTIFICATION OF MAILING BY EXPRESS MAIL: I hereby certify that this correspondence is being deposited with the United States Postal Service with Express Mail post office to addressee service under 37 CFR 1.10, postage prepaid, in a package addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231 with the express mail label number EB-165-858-383 on the date set forth below.

Gilbert P. Hyatt, Inventor — June 6, 1995
Date

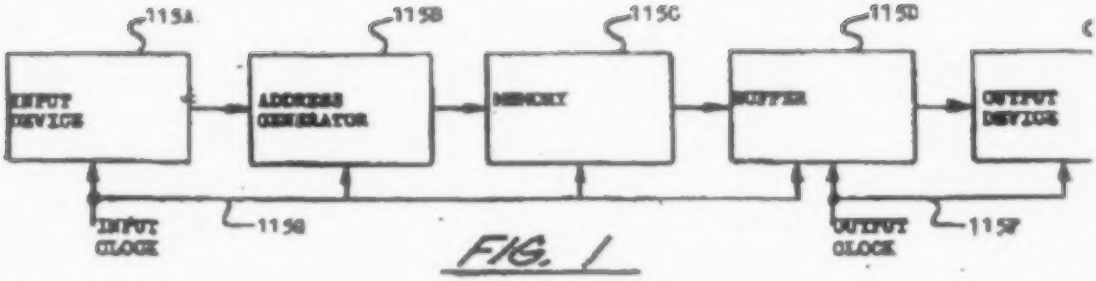

115A
115B
115C
115D
INPUT DEVICE
ADDRESS GENERATOR
MEMORY
BUFFER
OUTPUT DEVICE
INPUT CLOCK
115E
OUTPUT CLOCK
115F

FIG. 1

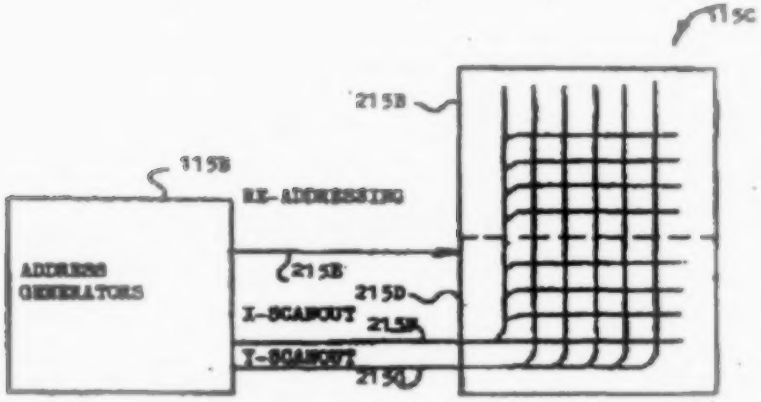

115C
215B
115B
RE-ADDRESSING
ADDRESS GENERATORS
215E
215D
I-SCANOUT
215F
I-SCANOUT
215G

FIG. 2

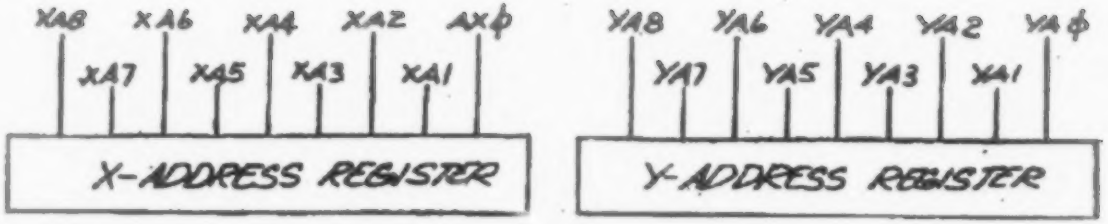


FIG. 3

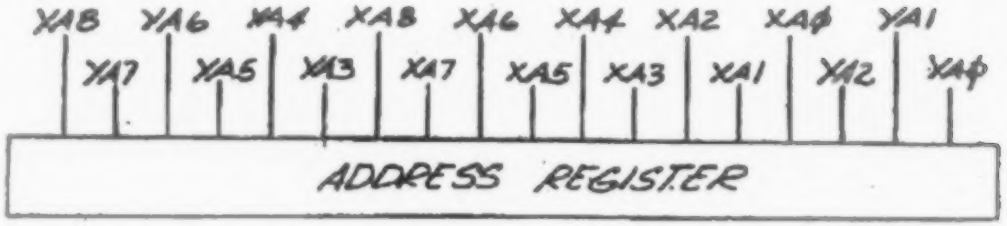


FIG. 4

M/A71712

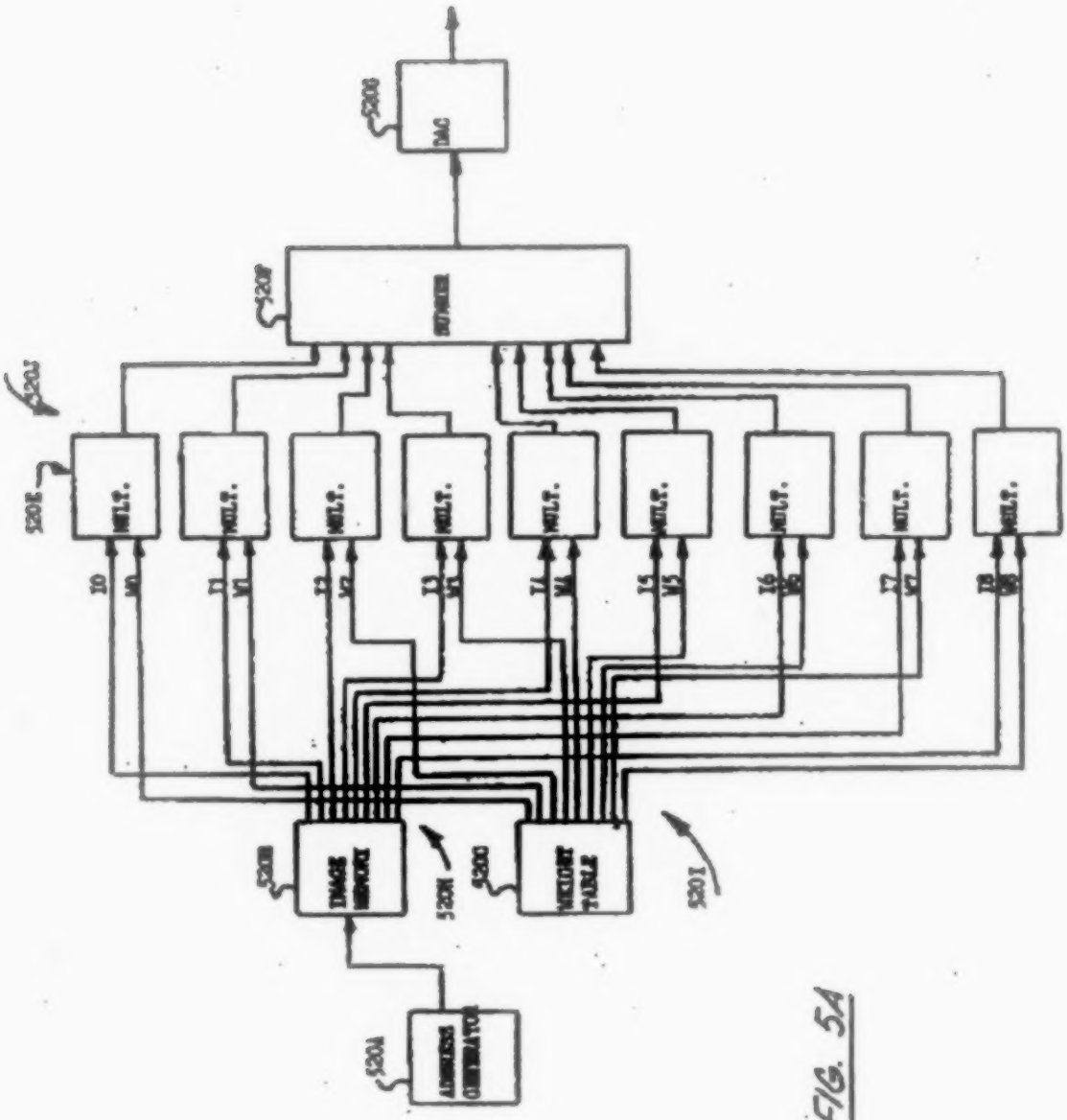

5206
DAC
5207
INTERFACE
5201
5202
MULT.
I0
I1
I2
I3
I4
I5
I6
I7
V0
V1
V2
V3
V4
V5
V6
V7
5203
IMAGE MEMORY
5205
5200
MICROSEQUENCER
5201
5204
ADDRESS GENERATOR

FIG. 5A

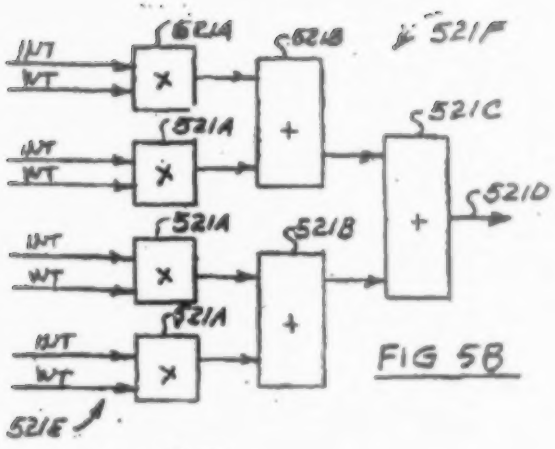

521A
521B
521F
521C
521D
INT
WT
521E

FIG 5B

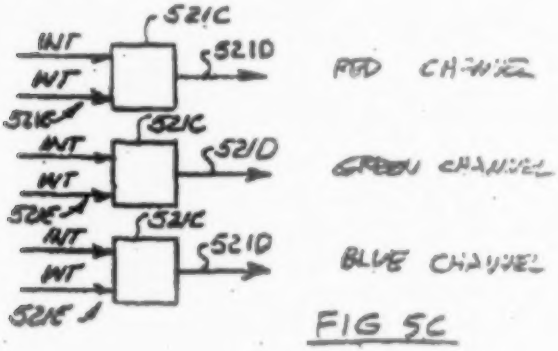

521C
521D
INT
WT
521E
RED CHANNEL
GREEN CHANNEL
BLUE CHANNEL

FIG 5C

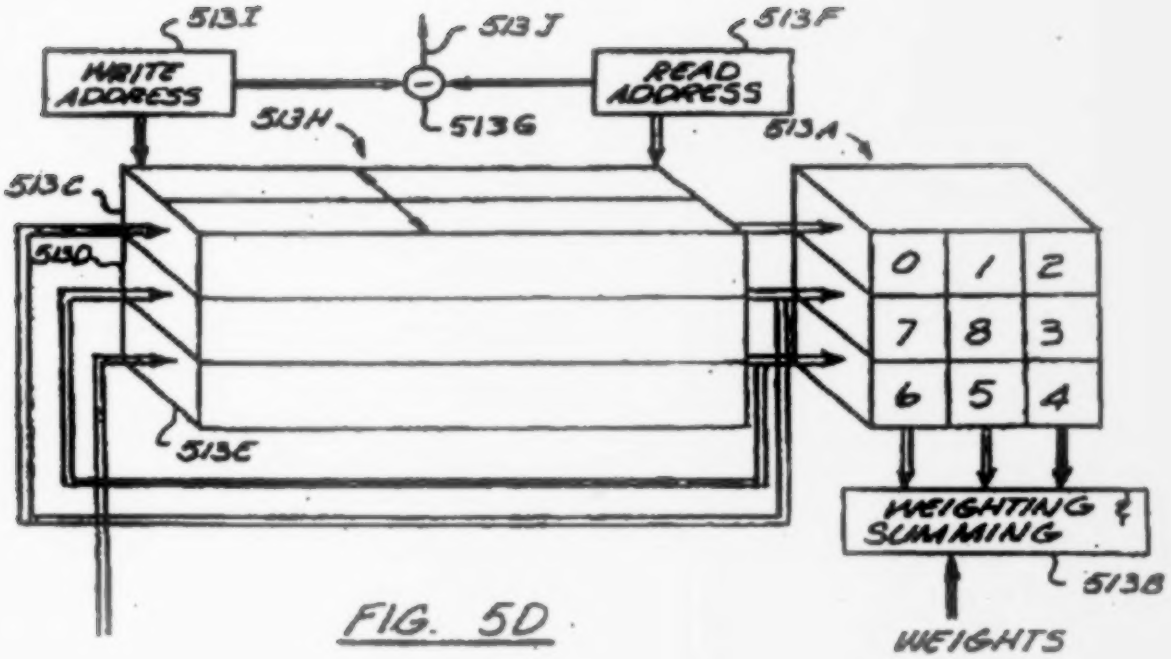

513I
513J
513F
WRITE ADDRESS
READ ADDRESS
513H
513G
513A
513C
513D
513E
0 1 2
7 8 3
6 5 4
WEIGHTING & SUMMING
513B
WEIGHTS

FIG. 5D

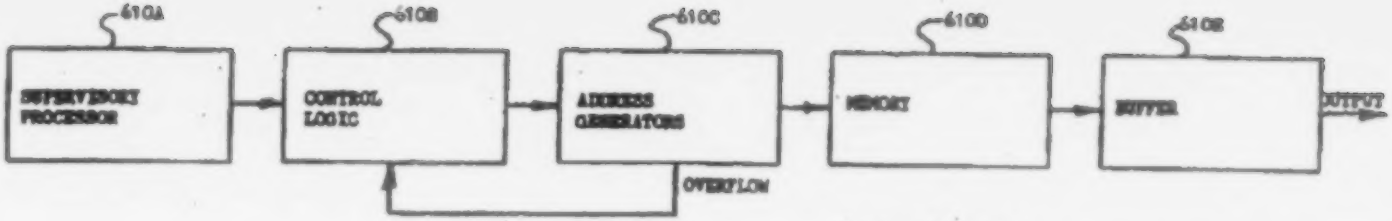


FIG. 6A

M/471702

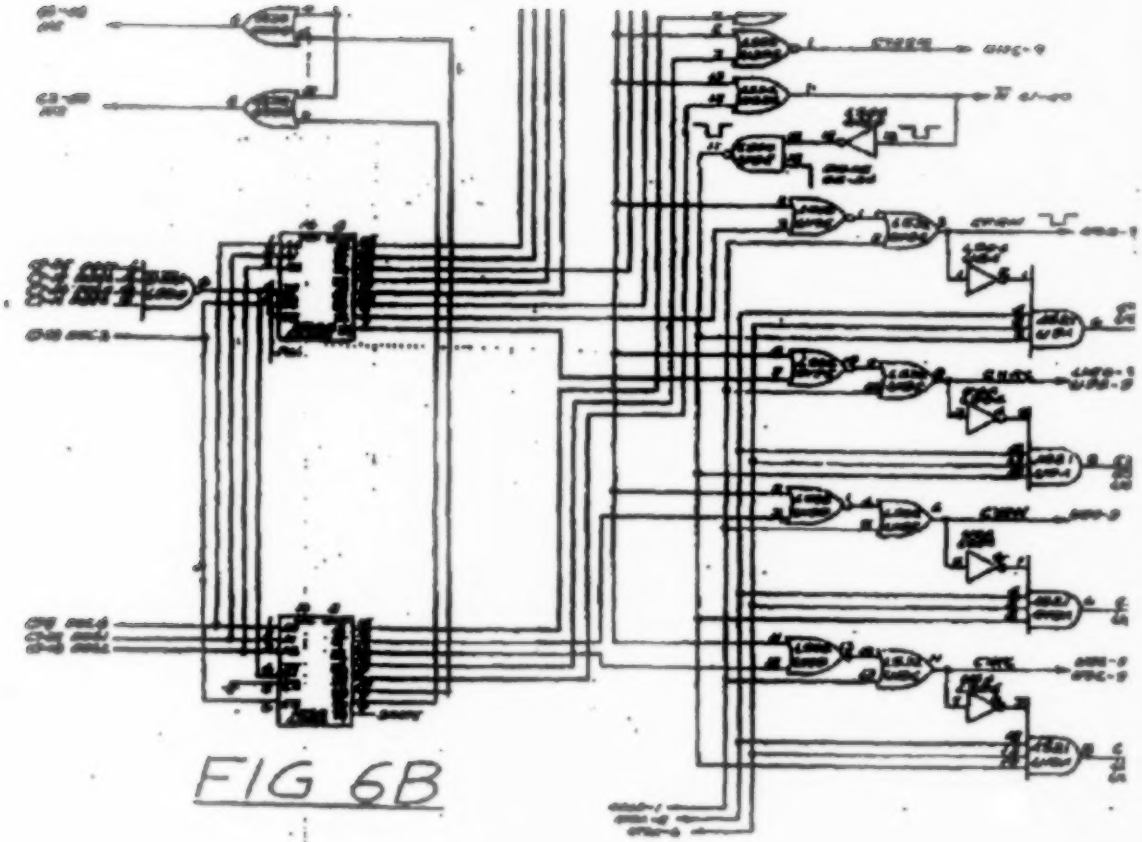
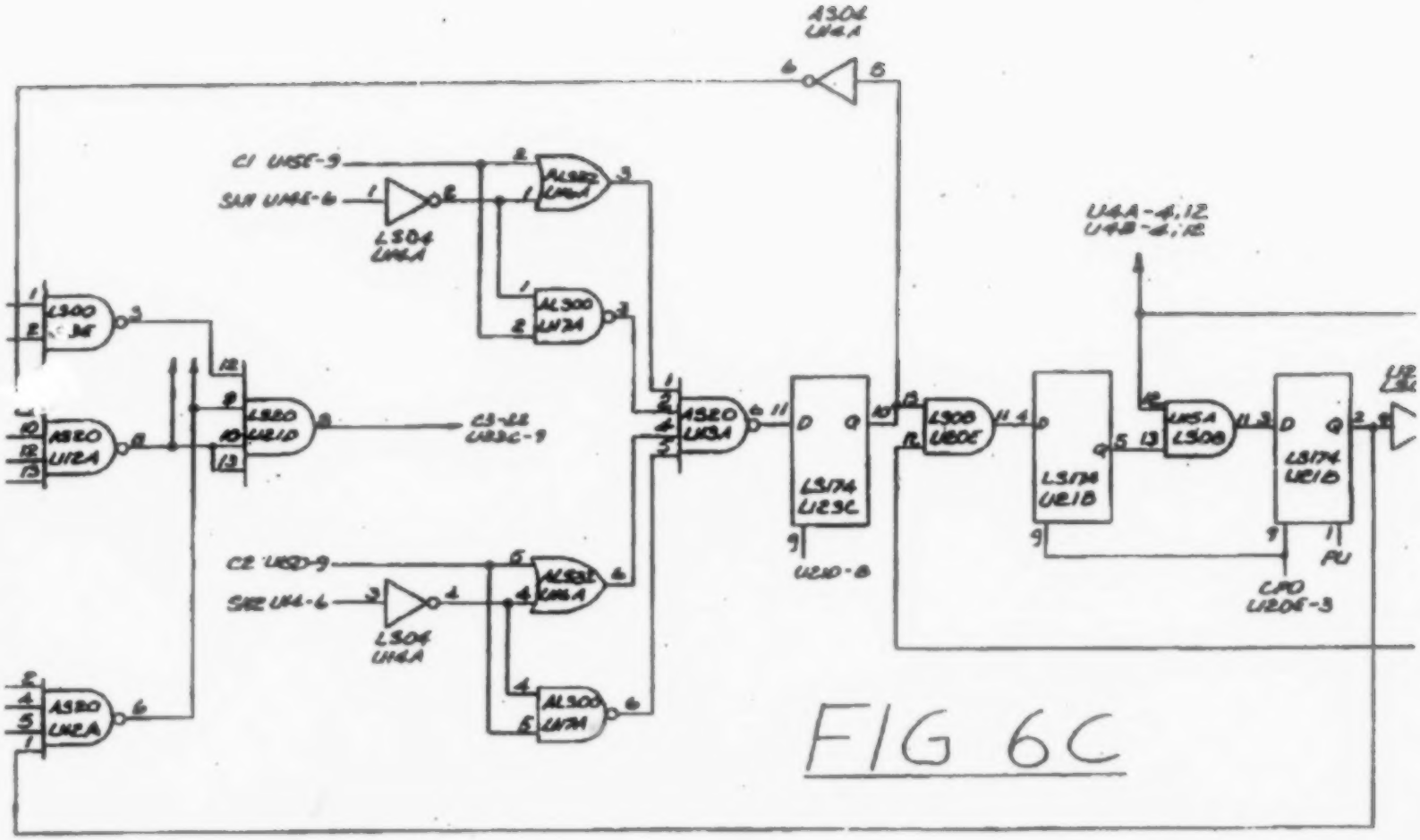


FIG 6B



AS04
U14A
C1 U15E-9
SA11 U14E-6
LS04
U14A
AL300
U17A
AS20
U13A
LS174
U23C
U21D-8
LS08
U20E
LS174
U21B
U4A-4,12
U4B-4,12
U15A
LS08
LS174
U21B
CPO
U20E-3
PU
LS00
AS20
U12A
LS20
U21D
C3-22
U23C-9
C2 U15D-9
SA2 U14-6
LS04
U14A
AS20
U12A

FIG 6C

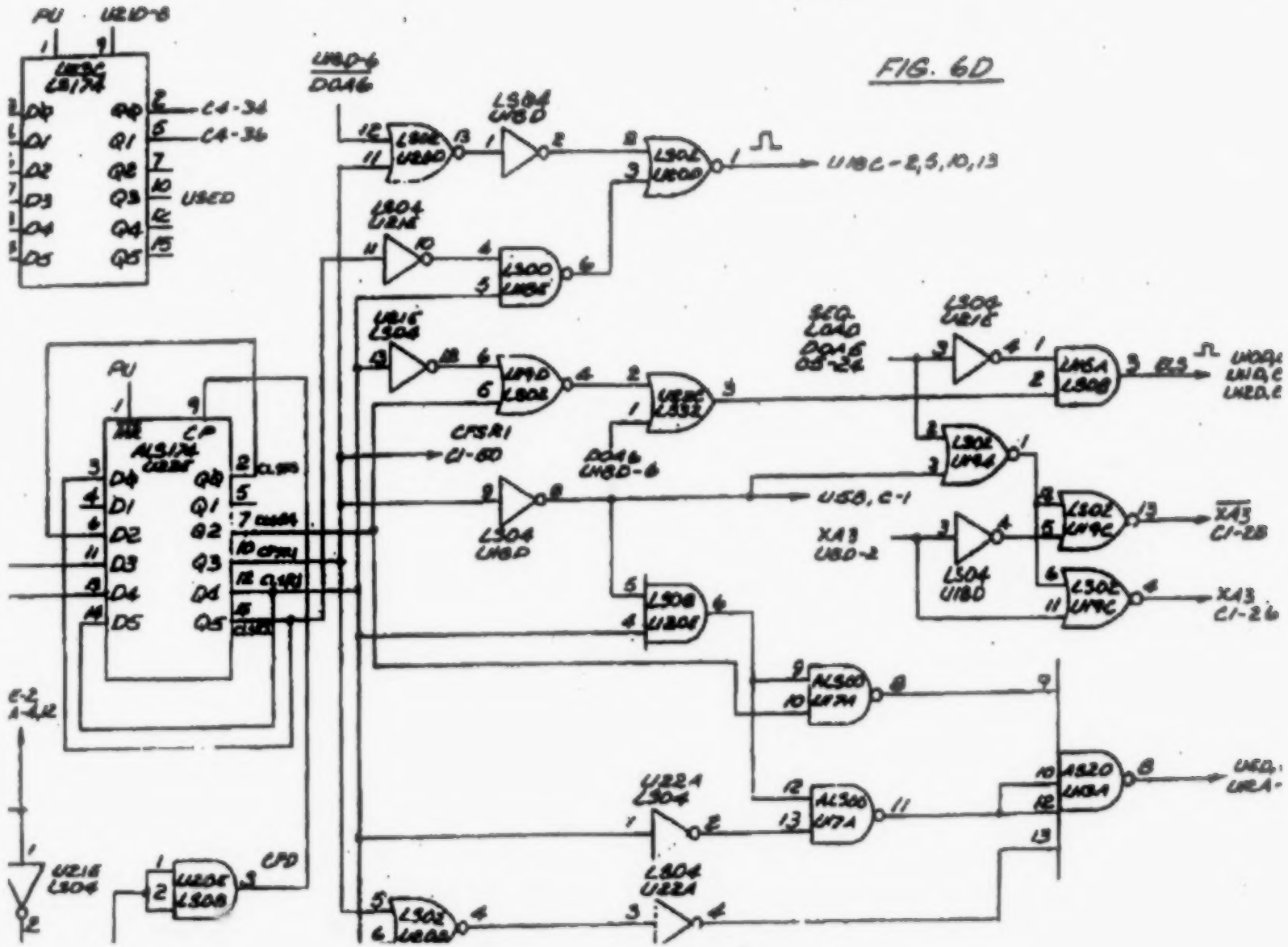
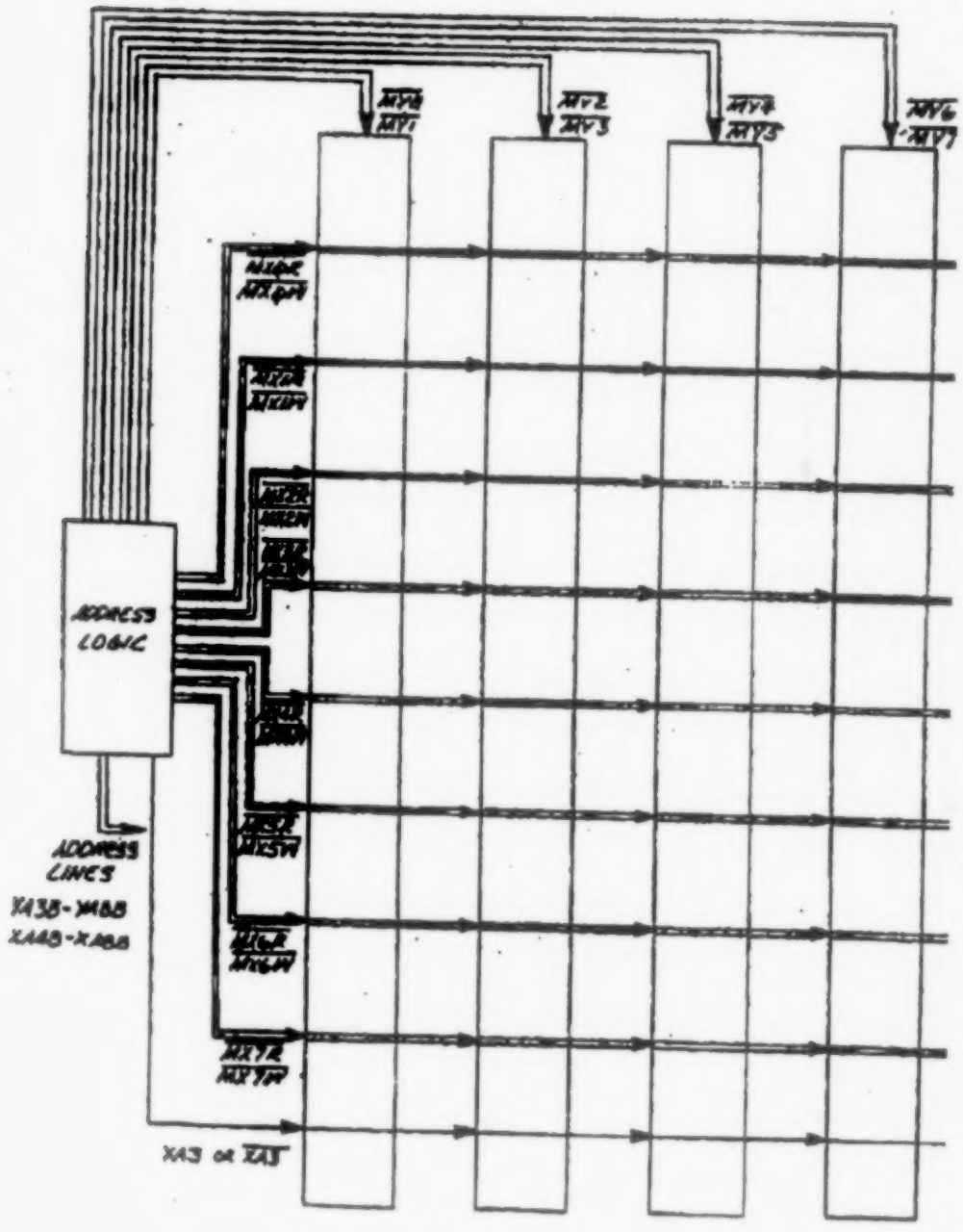
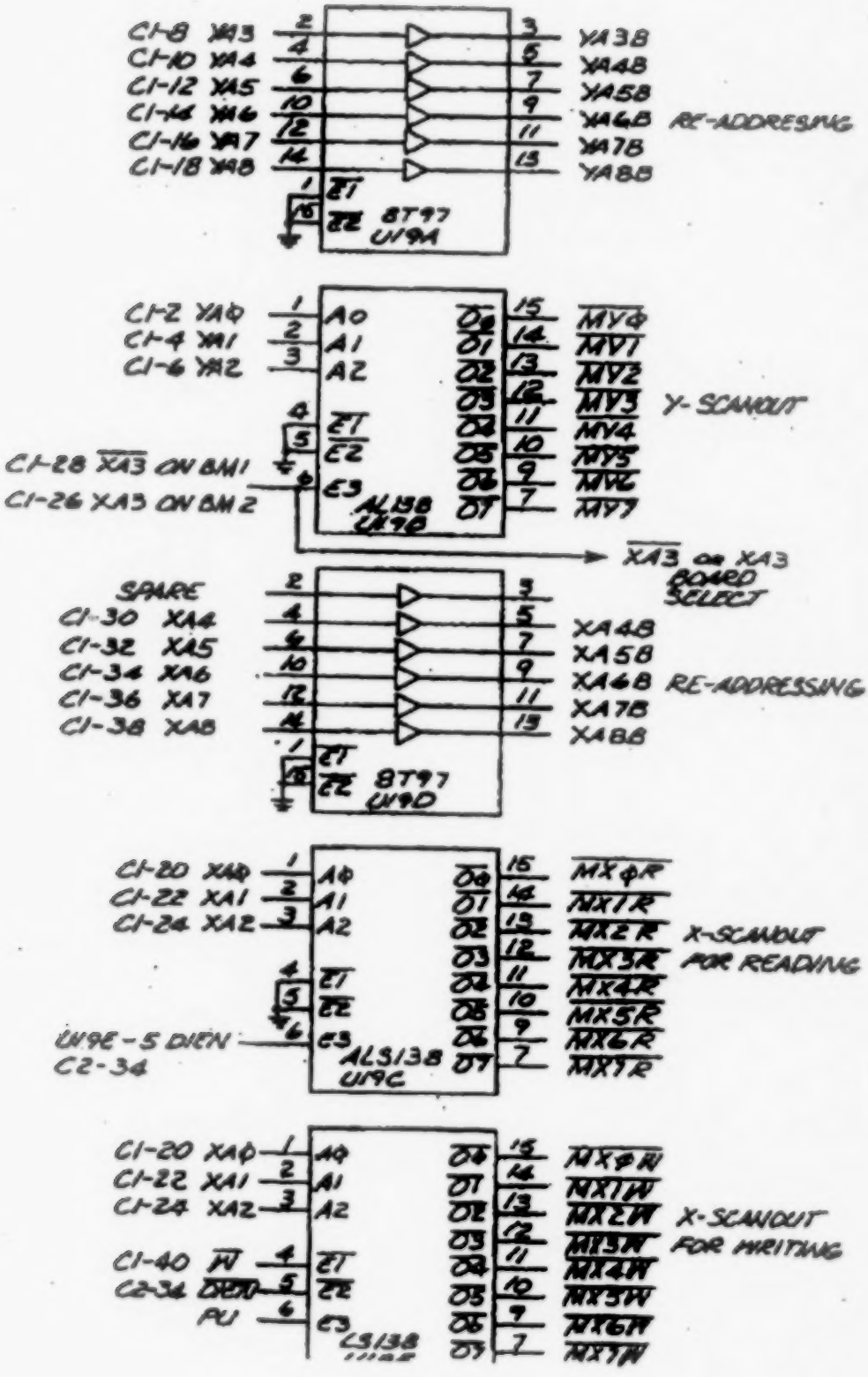

PU
U21D-8
U23C
LS174
C4-34
C4-36
USED
U18D-6
DOA6
LS04
U18D
U18C-2,5,10,13
U21E
LS04
U19D
LS02
U22C
LS32
CFSR1
C1-60
DOA6
U18D-6
U58, C-1
LS04
U18D
SEQ.
LOAD
DOA6
05-24
LS04
U21E
U16A
LS08
ELS
U19C
XA3
C1-28
XA3
C1-26
XA3
U18D-2
LS04
U18D
LS08
U20E
AL500
U17A
AS20
U13A
U22A
LS04
LS04
U22A
U21E
LS04
U20E
LS08
CPD
E-2
A-4,12

FIG. 6D


ADDRESS LOGIC
ADDRESS LINES
XA3B - XA8B
XA4B - XA8B
XA3 or XA3


C1-8 XA3
C1-10 XA4
C1-12 XA5
C1-14 XA6
C1-16 XA7
C1-18 XA8
YA3B
YA4B
YA5B
YA6B
YA7B
YA8B
RE-ADDRESSING
8T97
U19A
C1-2 XA0
C1-4 XA1
C1-6 XA2
MY0
MY1
MY2
MY3
MY4
MY5
MY6
MY7
Y-SCANOUT
C1-28 XA3 ON BM1
C1-26 XA3 ON BM2
ALS138
U19B
XA3 on XA3 BOARD SELECT
SPARE
C1-30 XA4
C1-32 XA5
C1-34 XA6
C1-36 XA7
C1-38 XA8
XA4B
XA5B
XA6B
XA7B
XA8B
RE-ADDRESSING
8T97
U19D
C1-20 XA0
C1-22 XA1
C1-24 XA2
MX0R
MX1R
MX2R
MX3R
MX4R
MX5R
MX6R
MX7R
X-SCANOUT FOR READING
U19E-5 DIEN
C2-34
ALS138
U19C
C1-20 XA0
C1-22 XA1
C1-24 XA2
C1-40 WI
C2-34 DIEN
PU
MX0W
MX1W
MX2W
MX3W
MX4W
MX5W
MX6W
MX7W
X-SCANOUT FOR WRITING
LS138

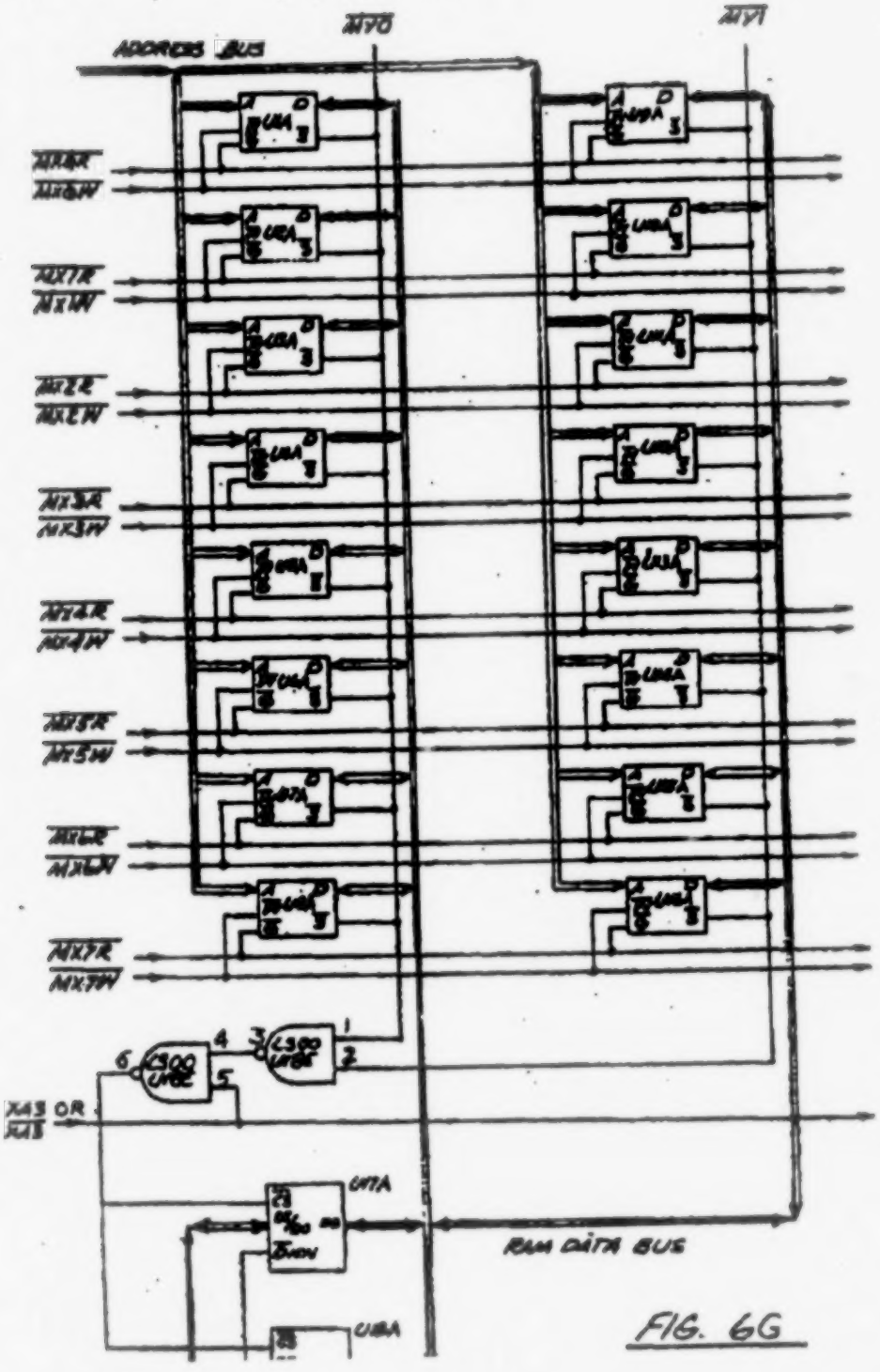


FIG. 6G

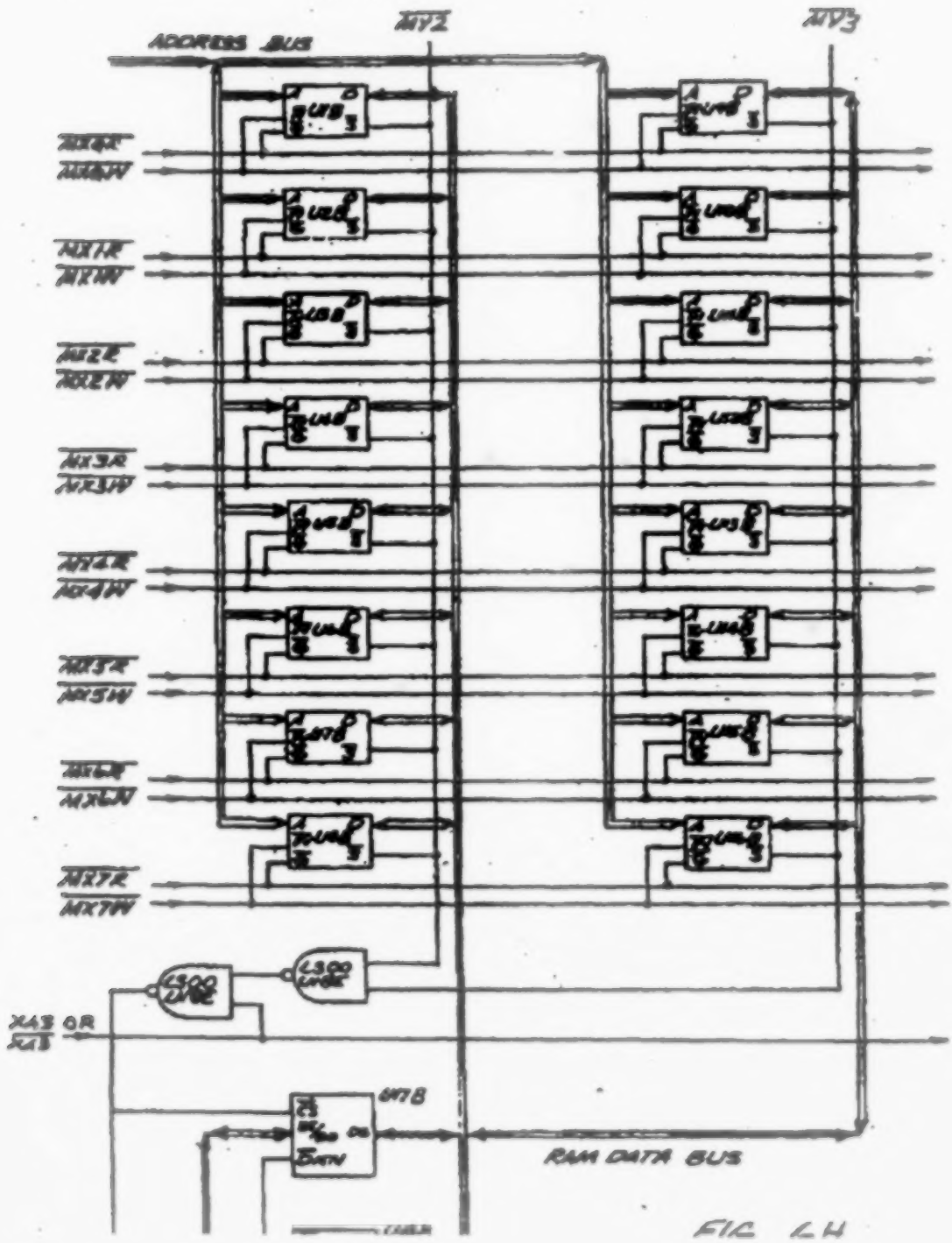


FIG 4

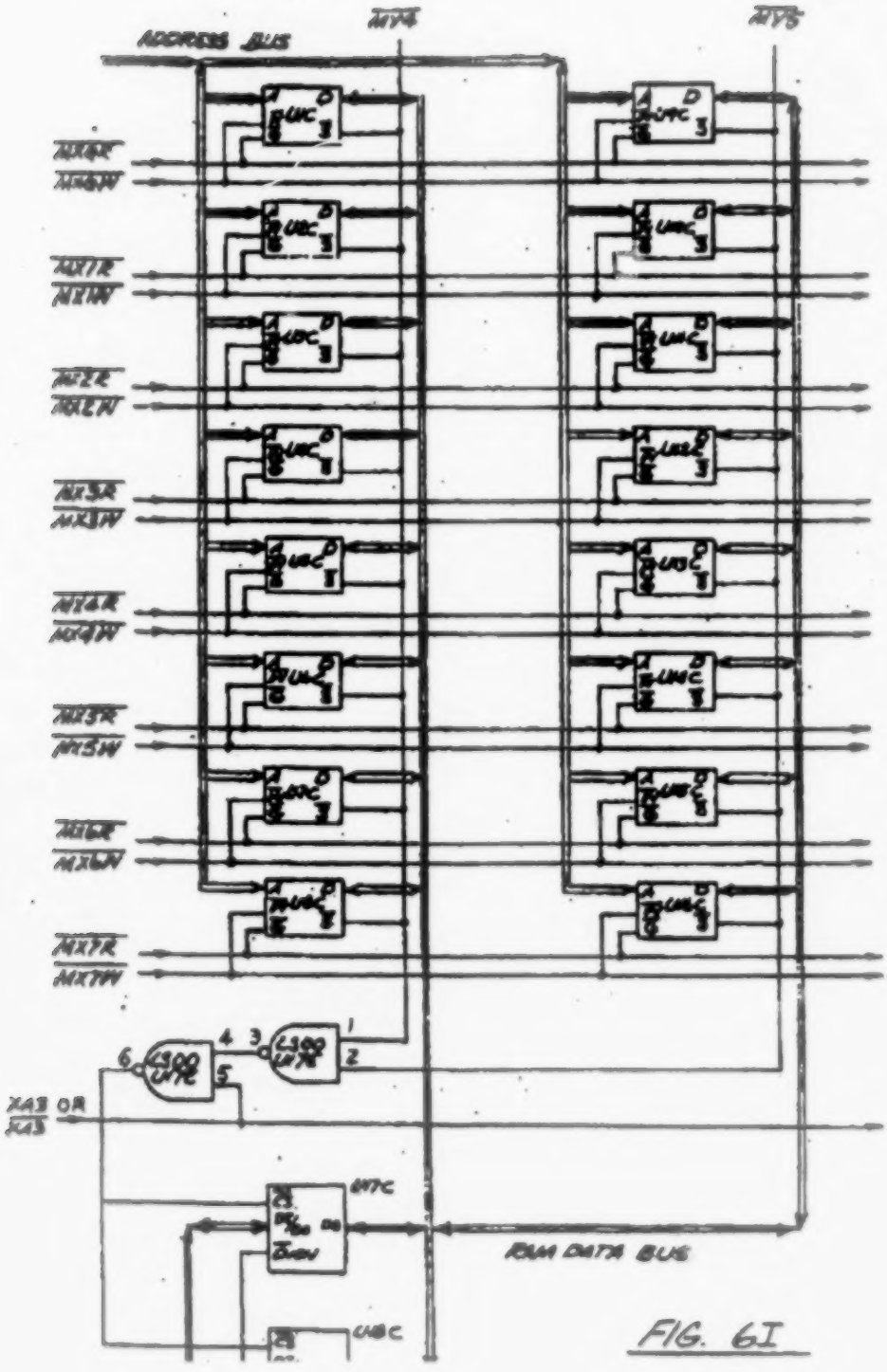
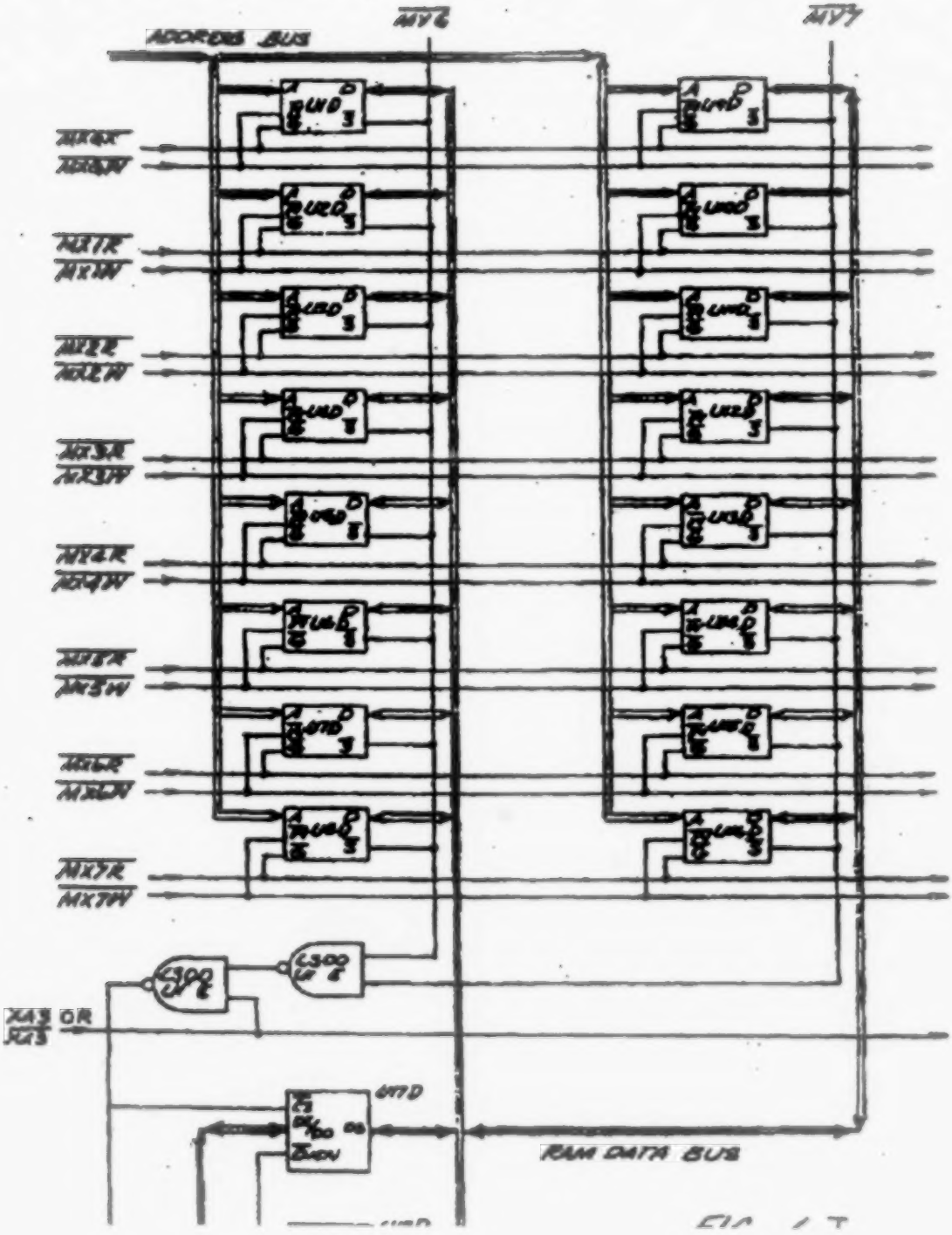
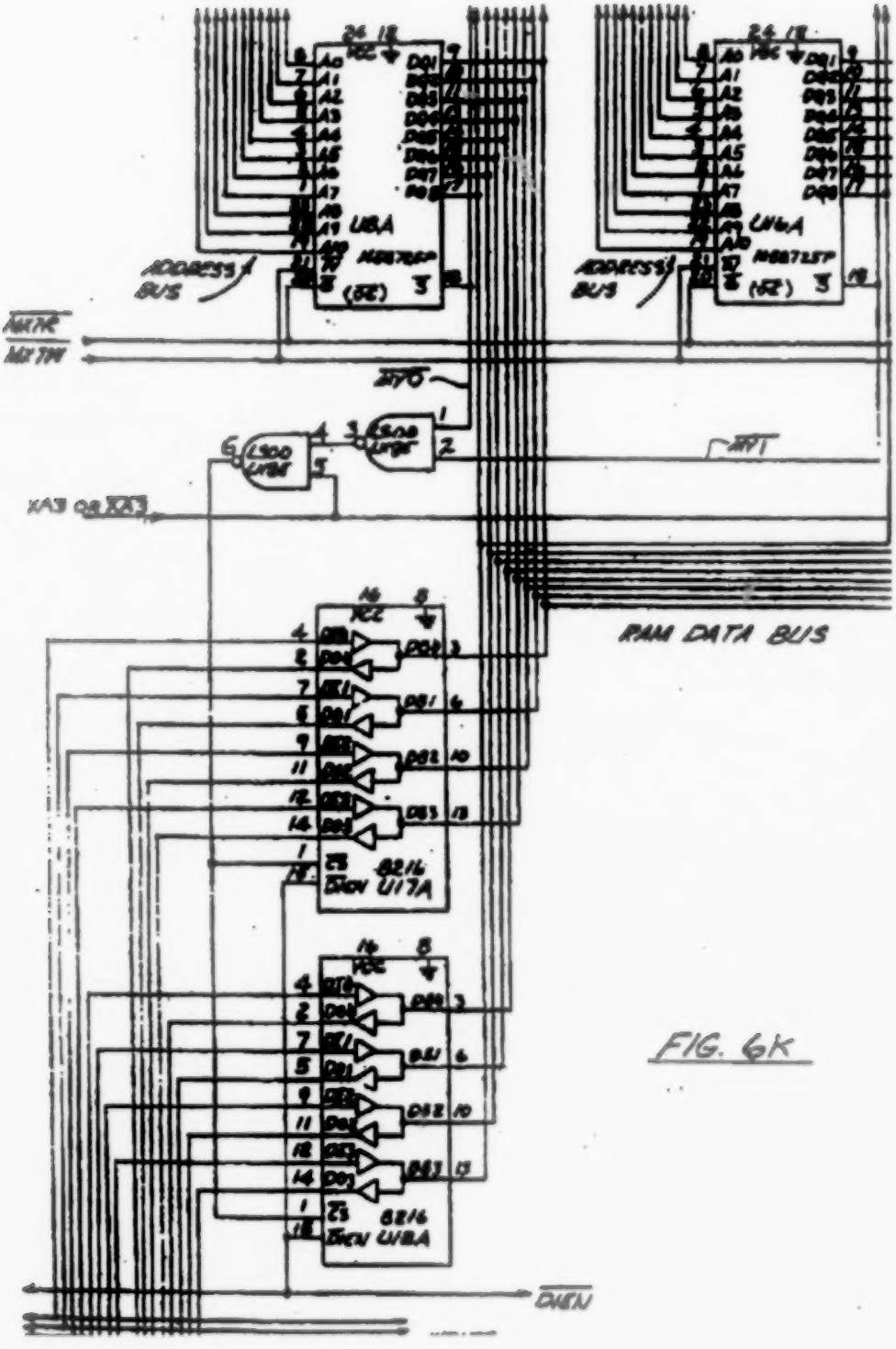


FIG. 6I


ADDRESS BUS
MY6
MY7
MX1R
MX1W
MX2R
MX2W
MX3R
MX3W
MX4R
MX4W
MX5R
MX5W
MX6R
MX6W
MX7R
MX7W
XA3 OR
RAM DATA BUS



ADDRESS BUS
ADDRESS BUS
RAM DATA BUS
8216
U17A
8216
U18A
DIEN

FIG. 6K

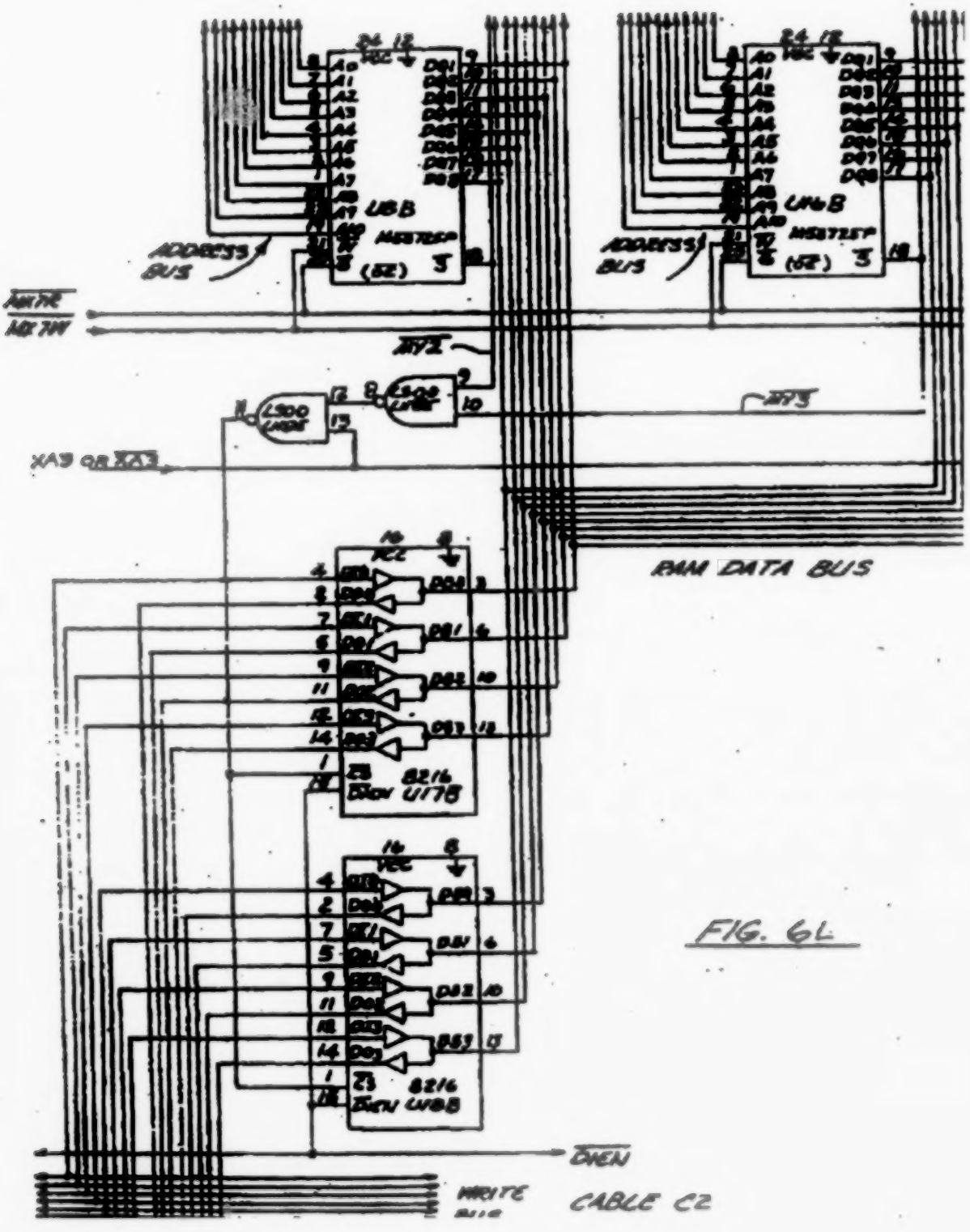


FIG. 6L

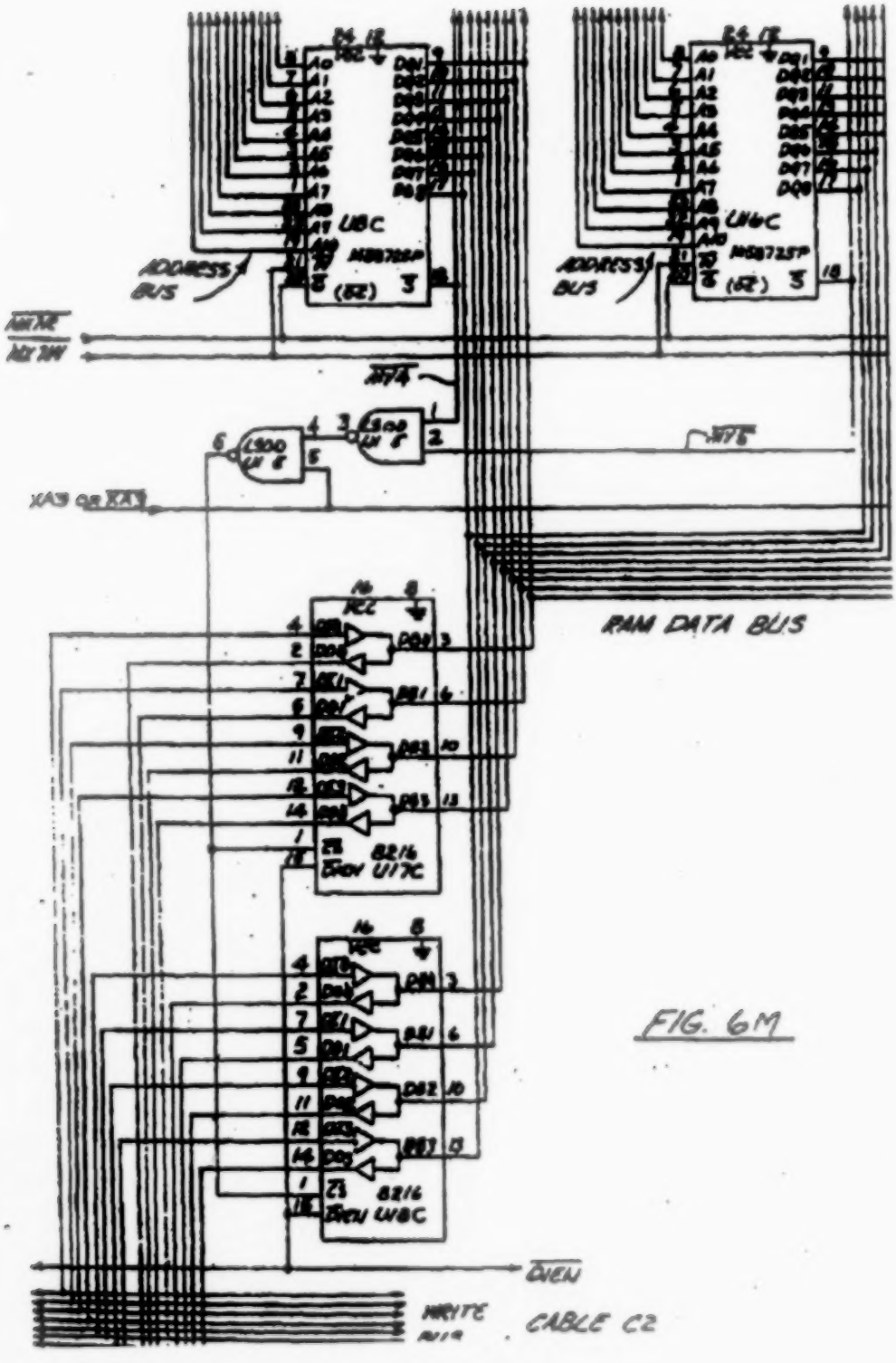
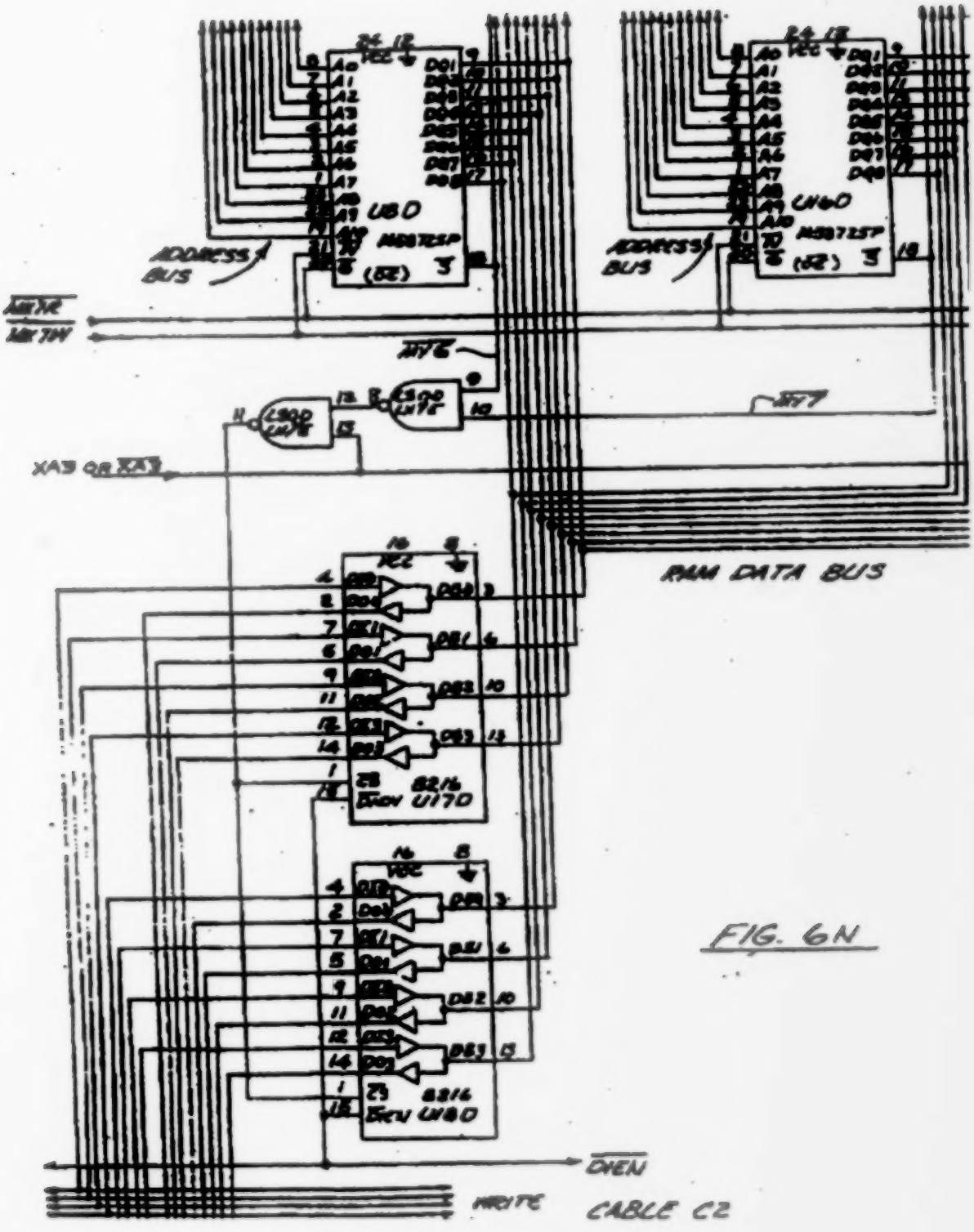
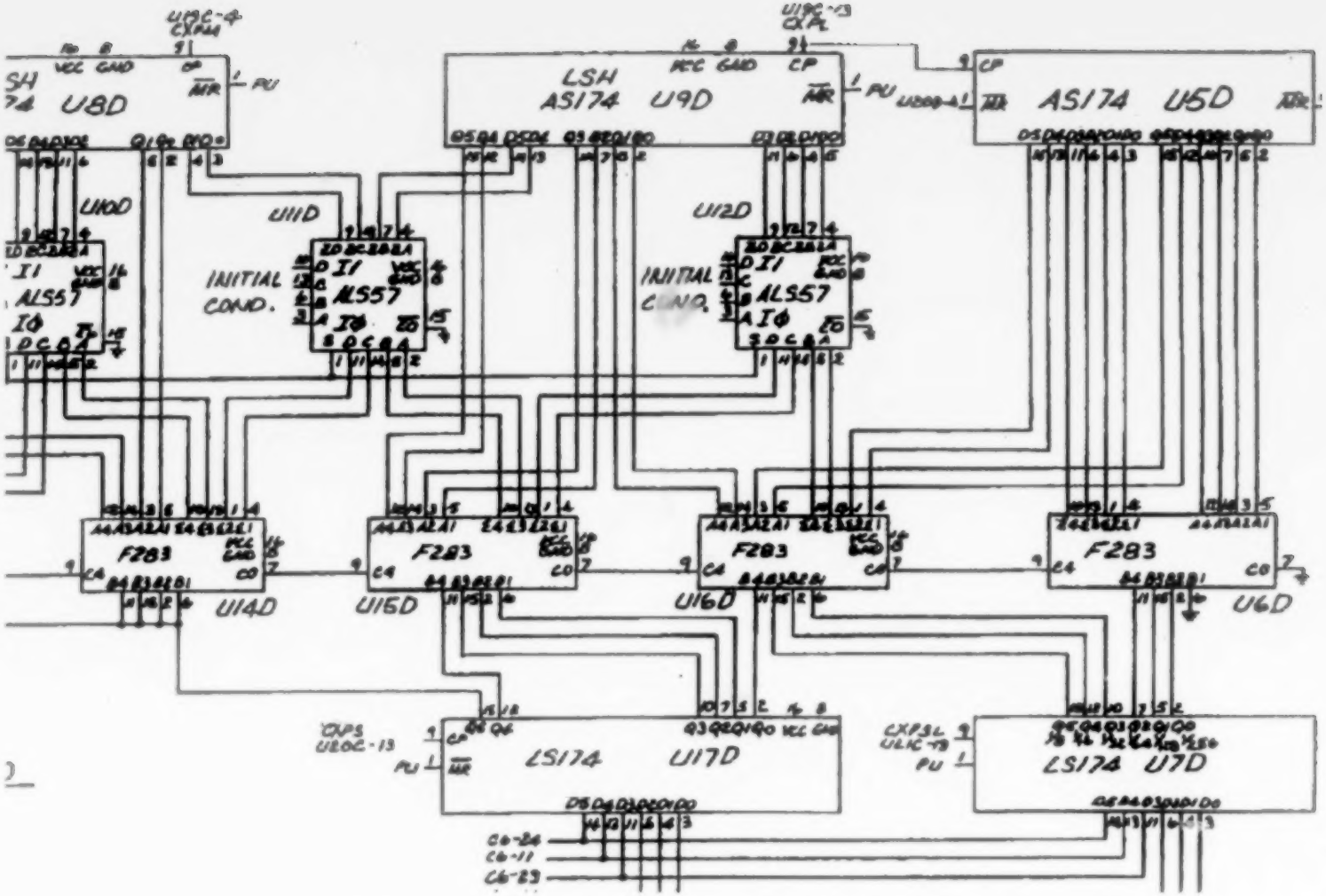


FIG. 6M

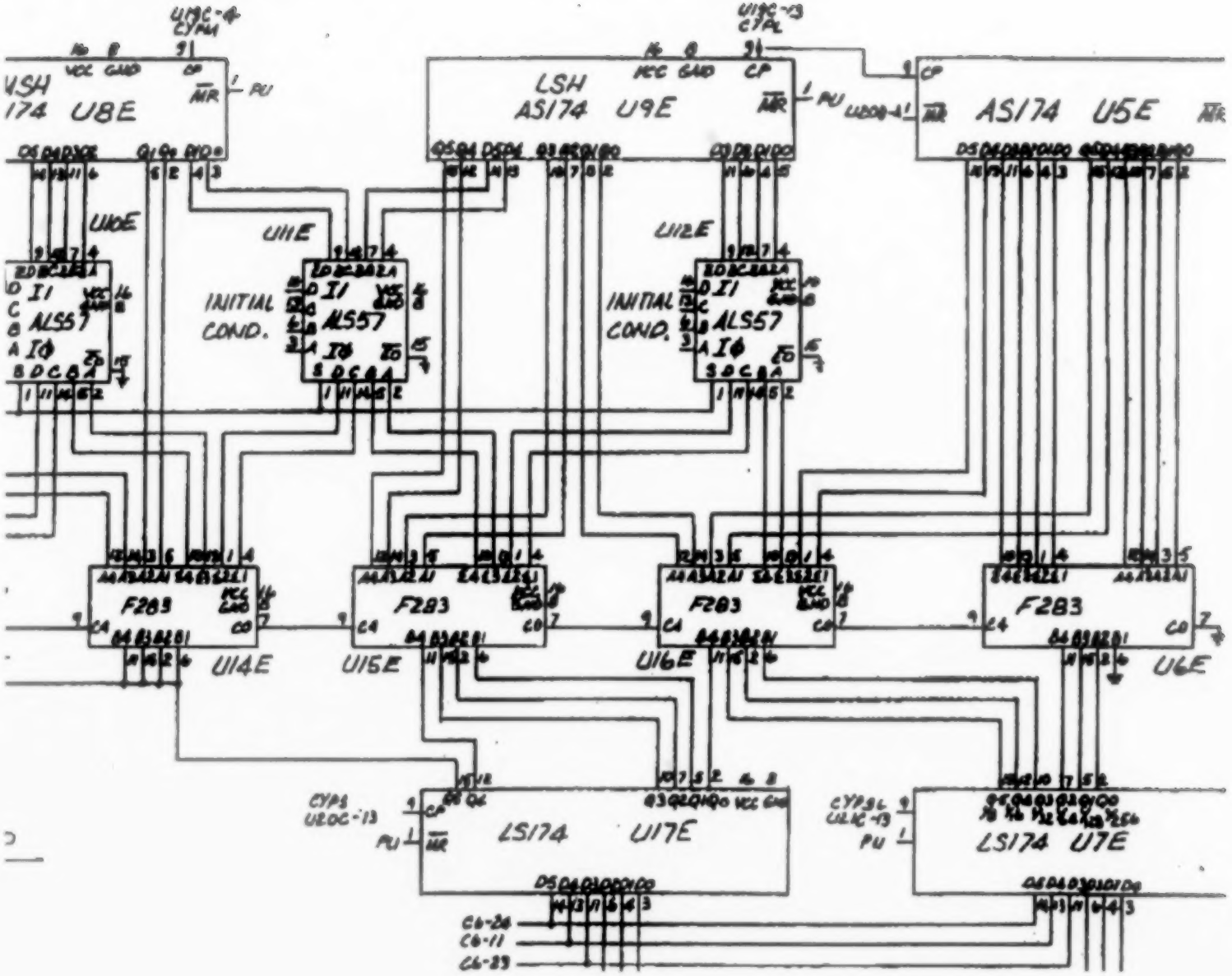


U8D
U16D
ADDRESS BUS
ADDRESS BUS
RAM DATA BUS
XA3 OR XA3
8216
U17D
8216
U18D
DIEN
WRITE
CABLE C2

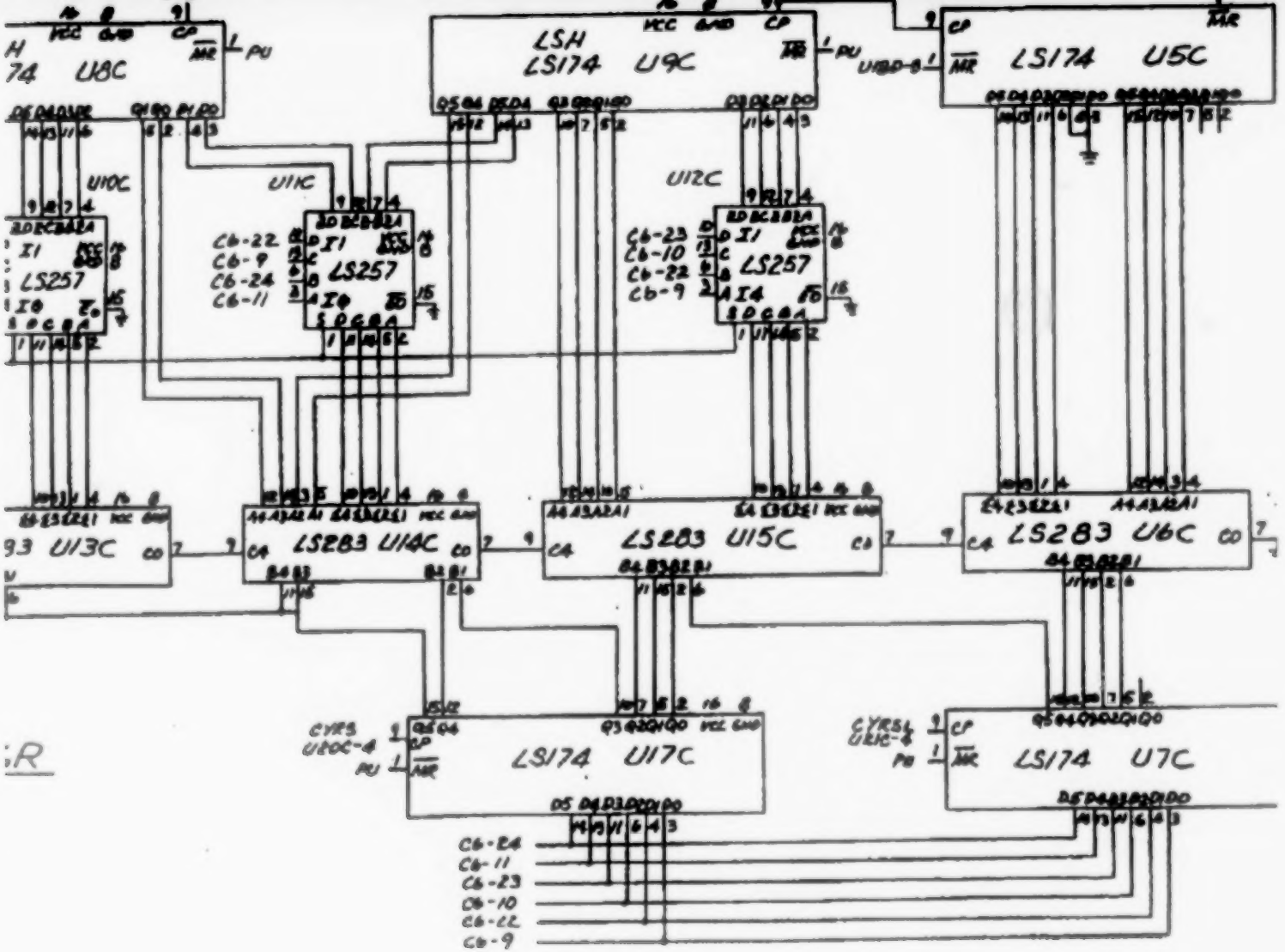
FIG. 6N

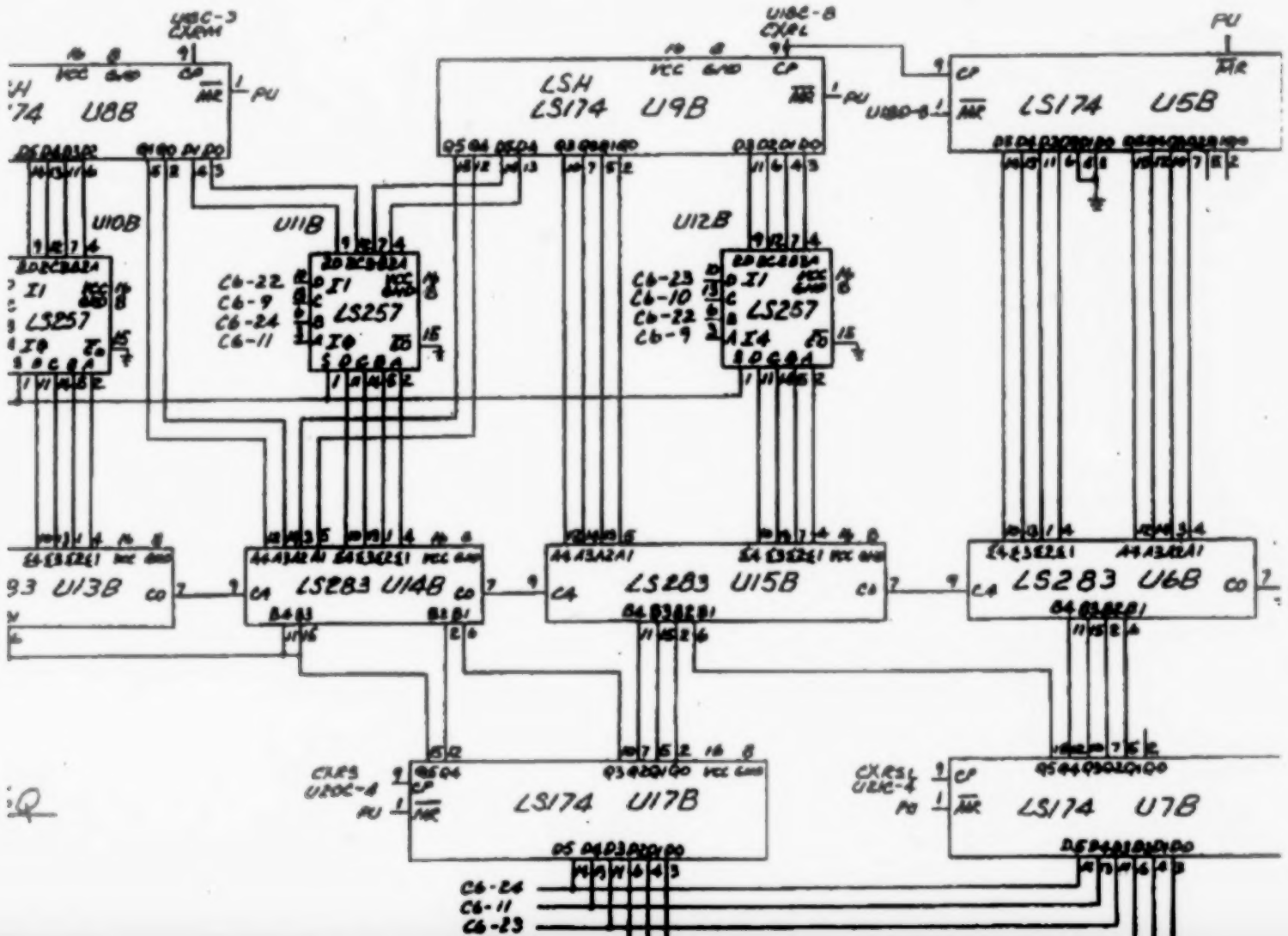


U8D
LSH
AS174 U9D
AS174 U5D
U10D
U11D
U12D
INITIAL COND.
ALS57
F283
U14D
U15D
U16D
U6D
LS174 U17D
LS174 U7D
C6-24
C6-11
C6-23



U8E
LSH
AS174 U9E
AS174 U5E
U10E
U11E
U12E
INITIAL COND.
INITIAL COND.
ALS57
ALS57
ALS57
F283
F283
F283
F283
U14E
U15E
U16E
U6E
LS174 U17E
LS174 U7E


LSH
LS174 U9C
LS174 U5C
U8C
U10C
U11C
U12C
LS257
C6-22
C6-9
C6-24
C6-11
C6-23
C6-10
C6-22
C6-9
LS283 U14C
LS283 U15C
LS283 U6C
U13C
LS174 U17C
LS174 U7C
C6-24
C6-11
C6-23
C6-10
C6-22
C6-9


LSH
LS174 U9B
LS174 U5B
U10B
U11B
U12B
LS257
C6-22
C6-9
C6-24
C6-11
C6-23
C6-10
C6-22
C6-9
LS283 U14B
LS283 U15B
LS283 U6B
LS174 U17B
LS174 U7B
C6-24
C6-11
C6-23

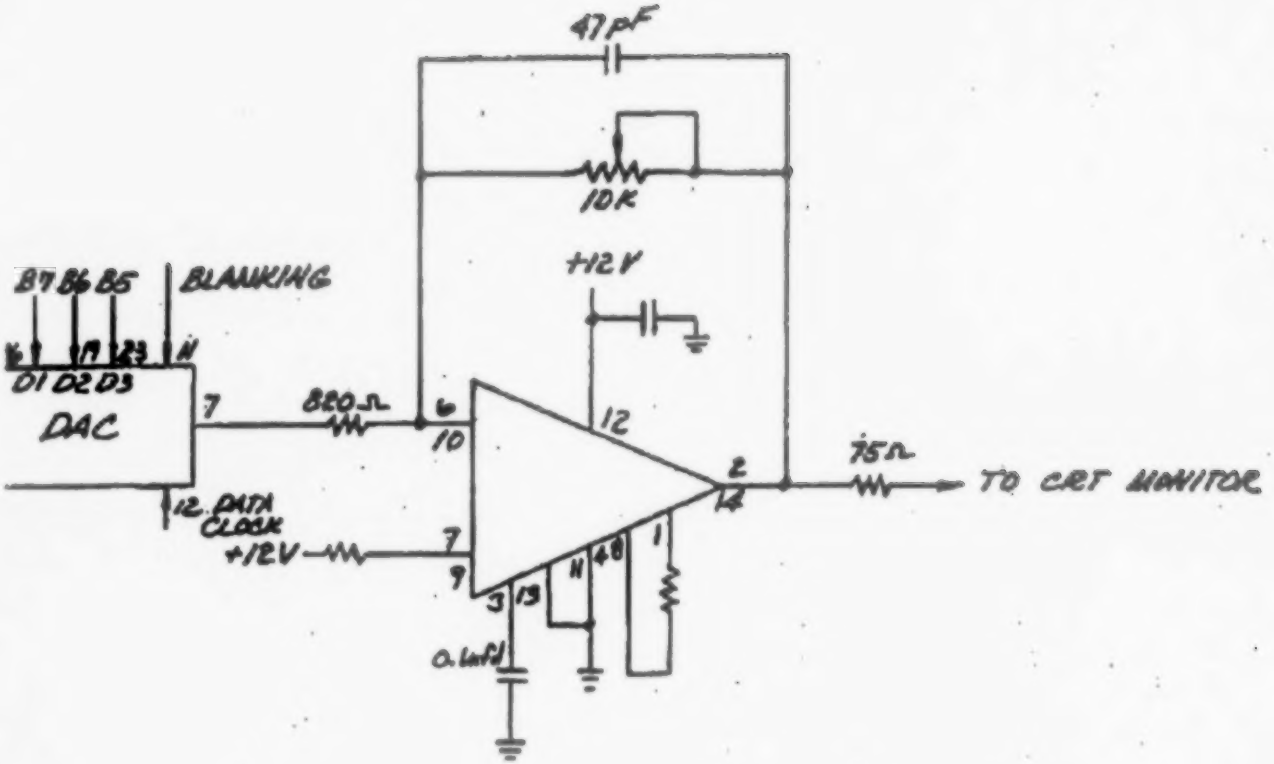
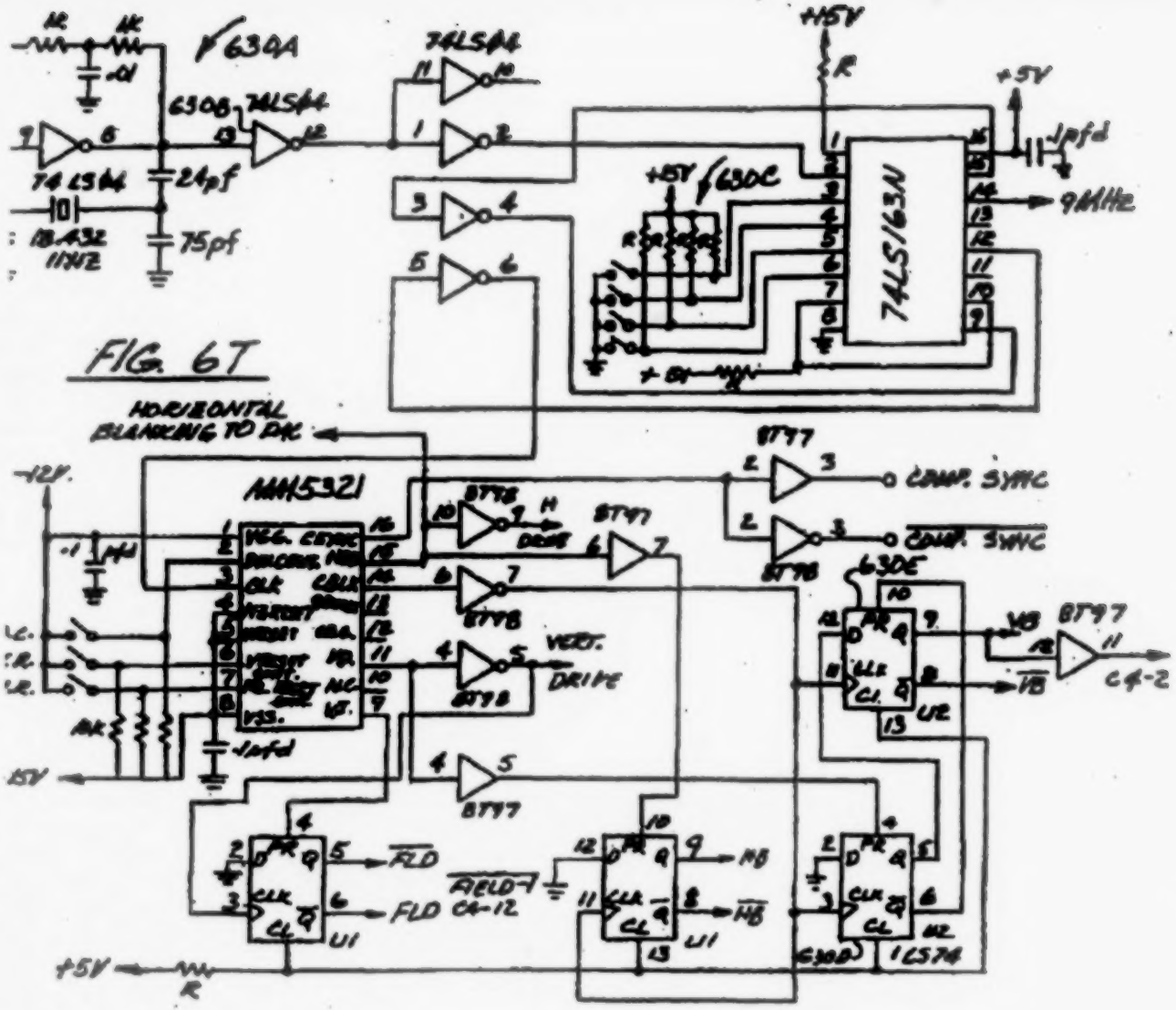

47pF
10K
+12V
B7 B6 B5
BLANKING
D1 D2 D3
DAC
7
820Ω
6
10
12
2
14
75Ω
TO CRT MONITOR
12. DATA CLOCK
+12V
7
9
3
13
11
48
1
0.1μfd

FIG. 6S



630A
630B
74LS04
74LS04
74LS04
24pf
75pf
18.432 MHz
+15V
R
+5V
.1pfd
9MHz
630C
74LS163N
HORIZONTAL BLANKING TO DAC
MM5321
-12V
.1pfd
BT97
BT98
COMP. SYNC
COMP. SYNC
VERT. DRIVE
630E
BT97
C4-2
FLD
FLD
FIELD-1 C4-12
HB
HB
U1
U2
630D
LS74
+5V
R

FIG. 6T

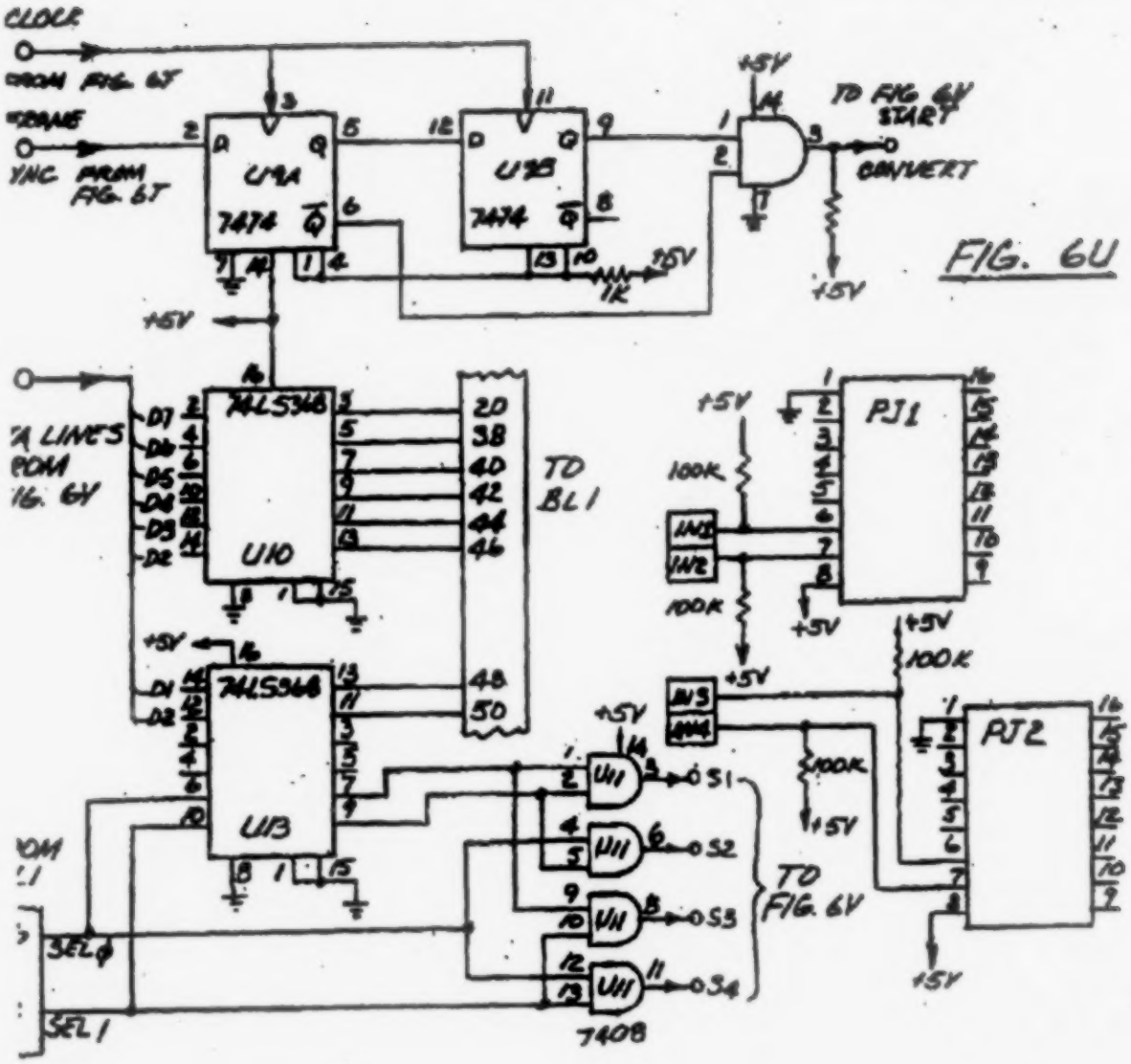

CLOCK
FROM FIG. 6T
FRAME
YNC FROM FIG. 6T
U9A
7474
U9B
7474
+5V
TO FIG 6V START
CONVERT
1K
74LS368
U10
U13
TO BL1
PJ1
PJ2
100K
TO FIG. 6V
7408
SEL 0
SEL 1

FIG. 6U

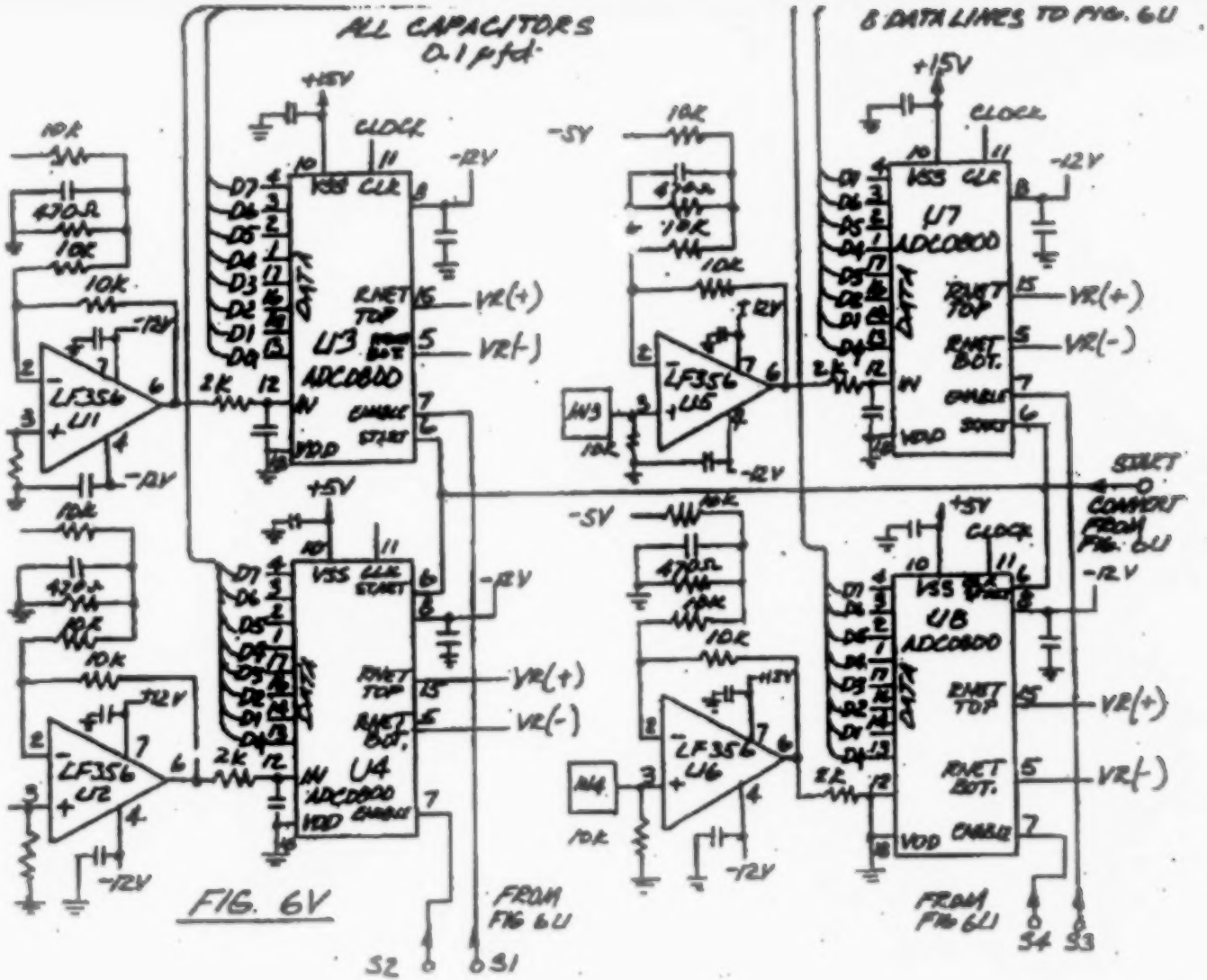
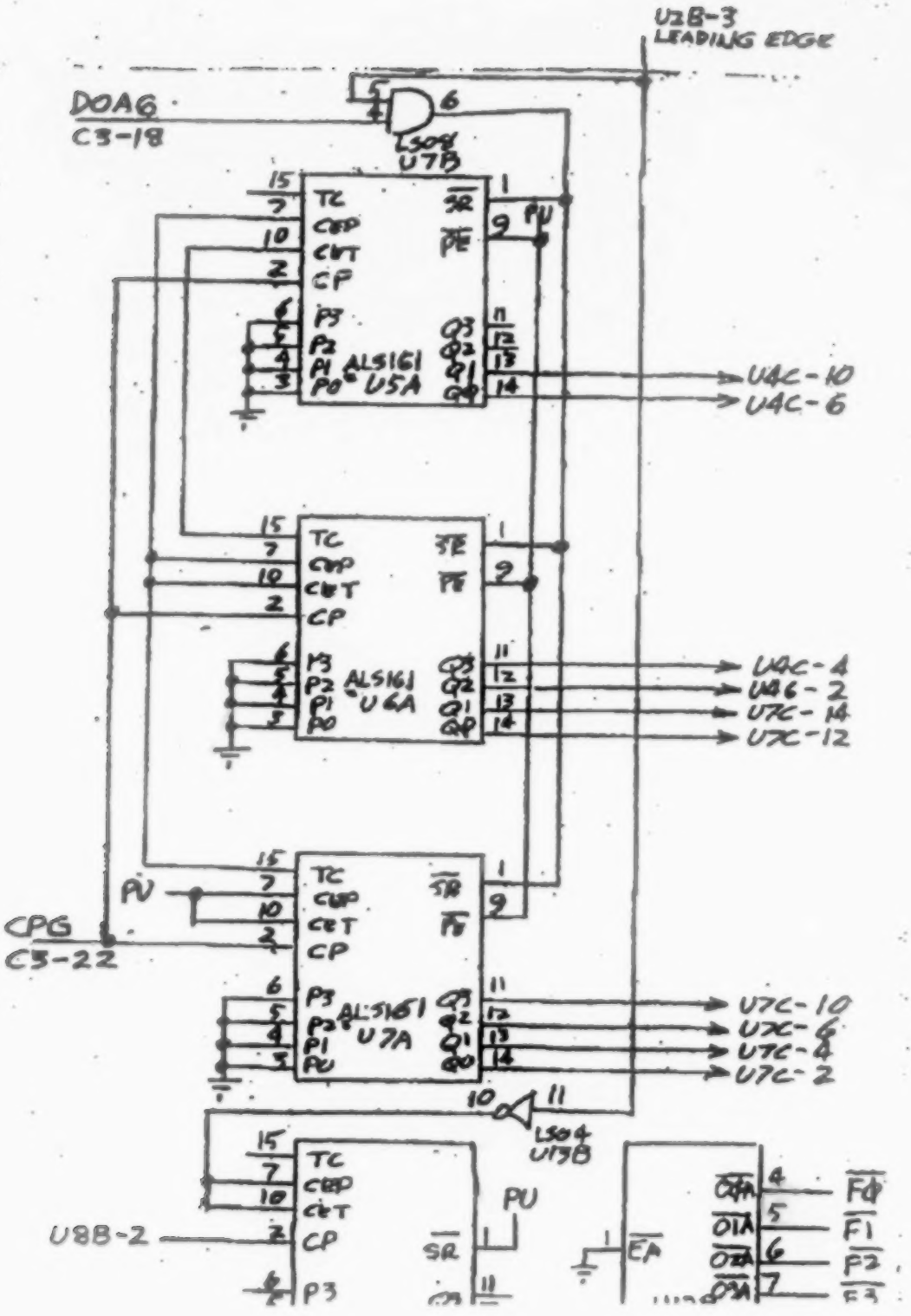

ALL CAPACITORS 0.1 μfd
8 DATA LINES TO FIG. 6U
+15V
CLOCK
-12V
-5V
+5V
10K
470Ω
2K
LF356 U1
LF356 U2
LF356 U5
LF356 U6
U3 ADC0800
U4 ADC0800
U7 ADC0800
U8 ADC0800
DATA
VSS
CLK
RNET TOP
RNET BOT.
ENABLE
START
VDD
IN
VR(+)
VR(-)
START
CONVERT FROM FIG. 6U
FROM FIG 6U
S1
S2
S3
S4

FIG. 6V


U2B-3
LEADING EDGE
DOAG
C3-18
LS08
U7B
TC
CEP
CET
CP
P3
P2
P1
P0
ALS161
U5A
PE
SR
PU
Q3
Q2
Q1
Q0
U4C-10
U4C-6
U6A
U4C-4
U4C-2
U7C-14
U7C-12
U7A
U7C-10
U7C-6
U7C-4
U7C-2
CPG
C3-22
LS04
U13B
U8B-2
EP
F0
F1
F2
F3

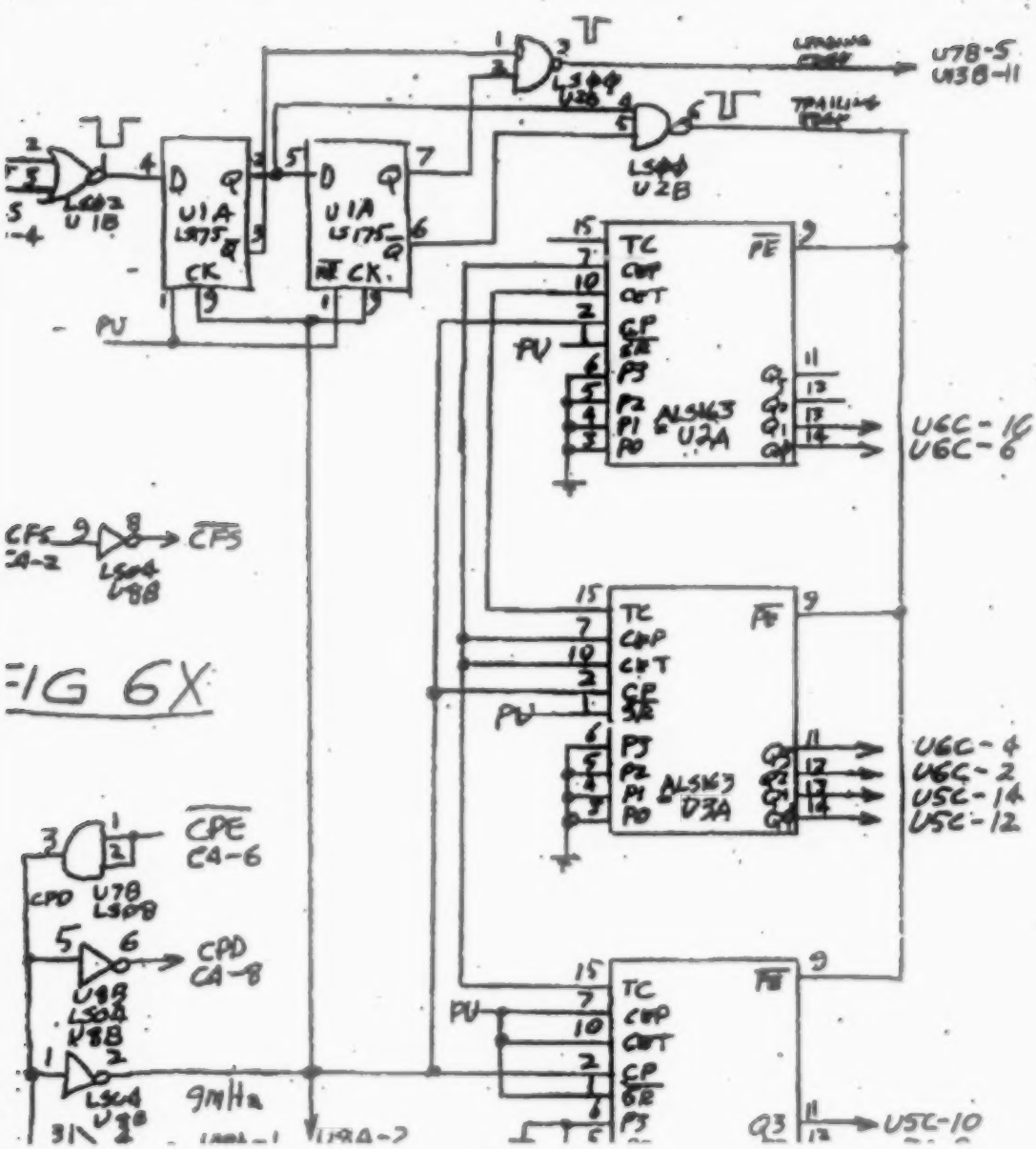
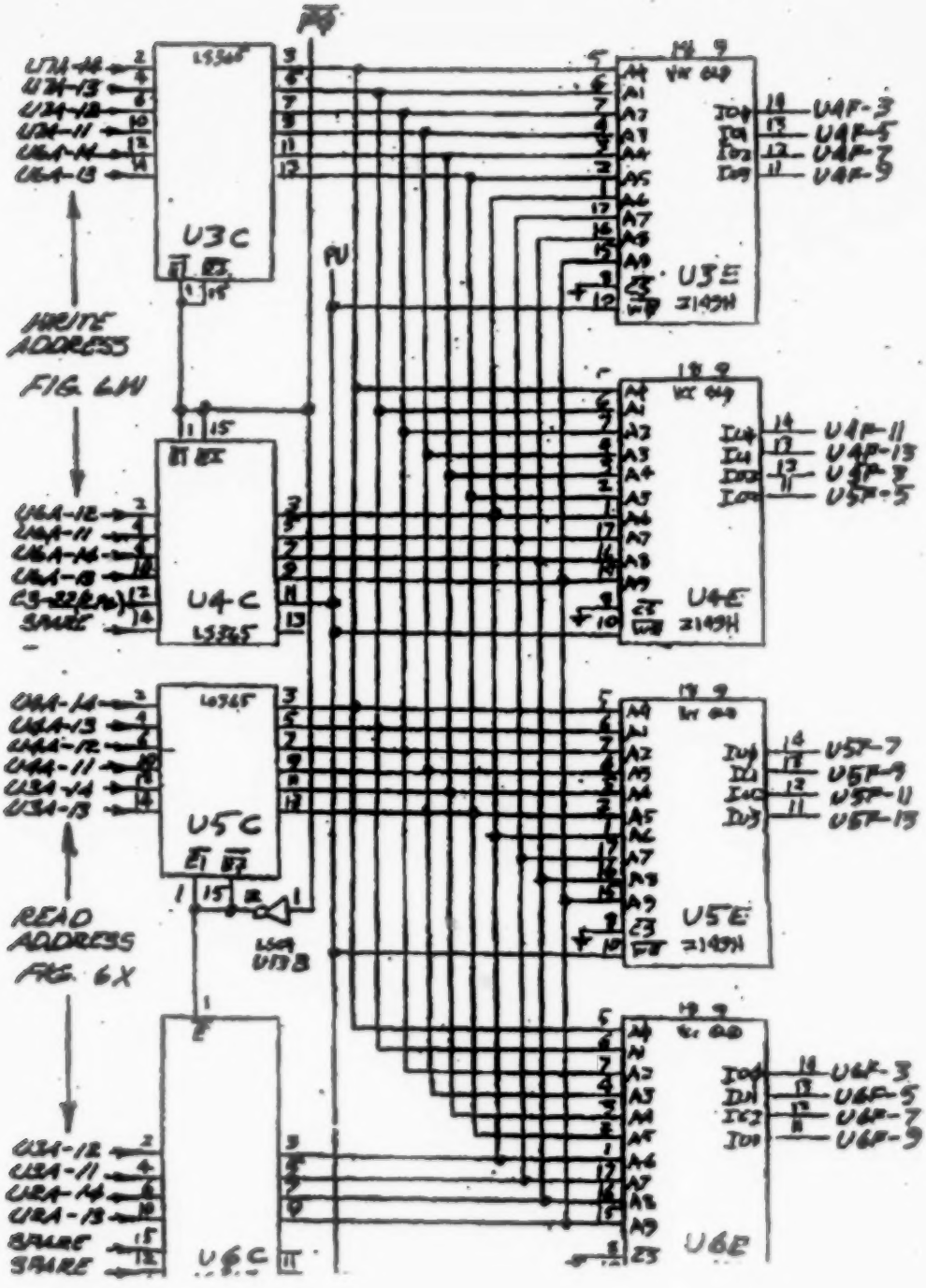
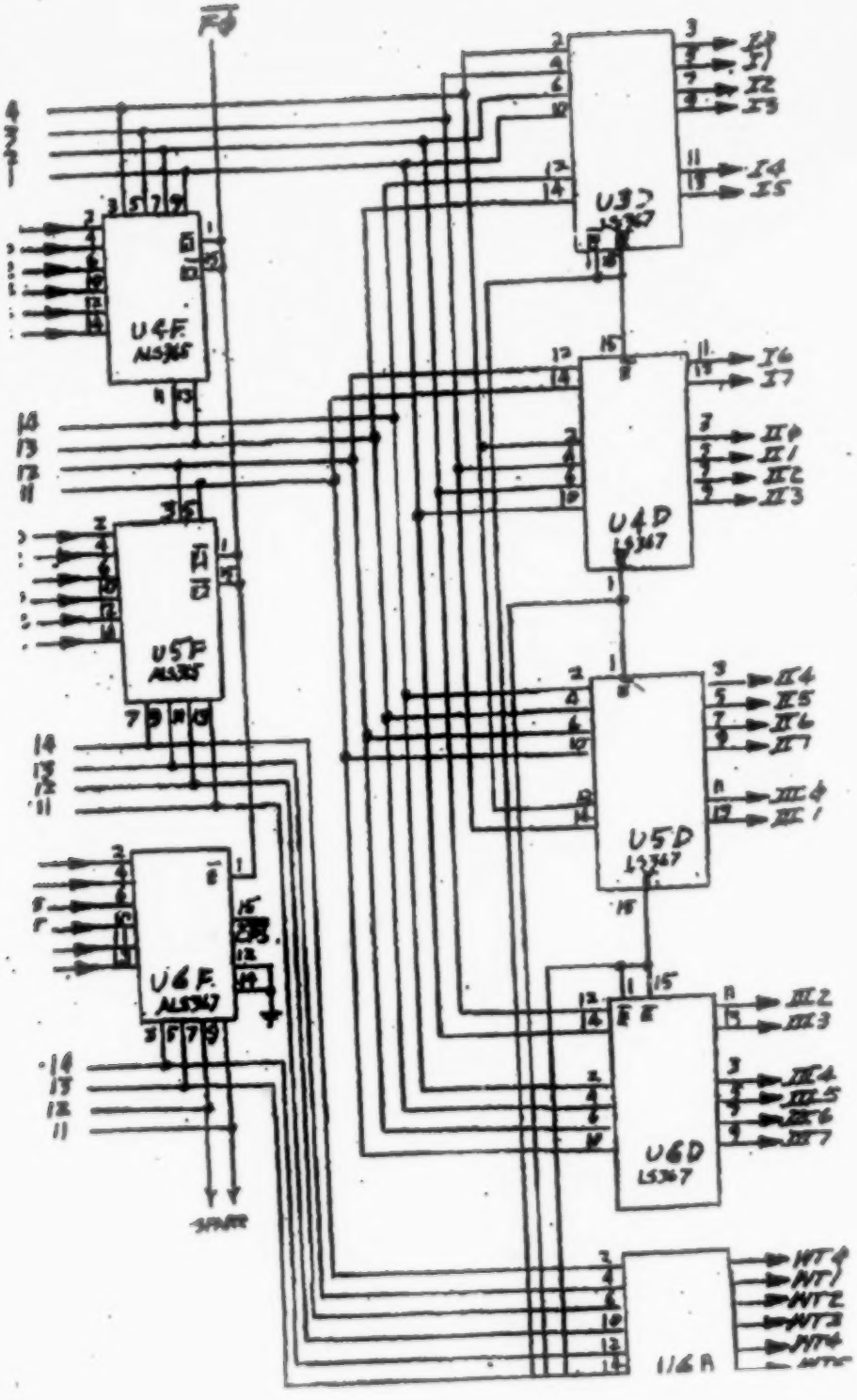
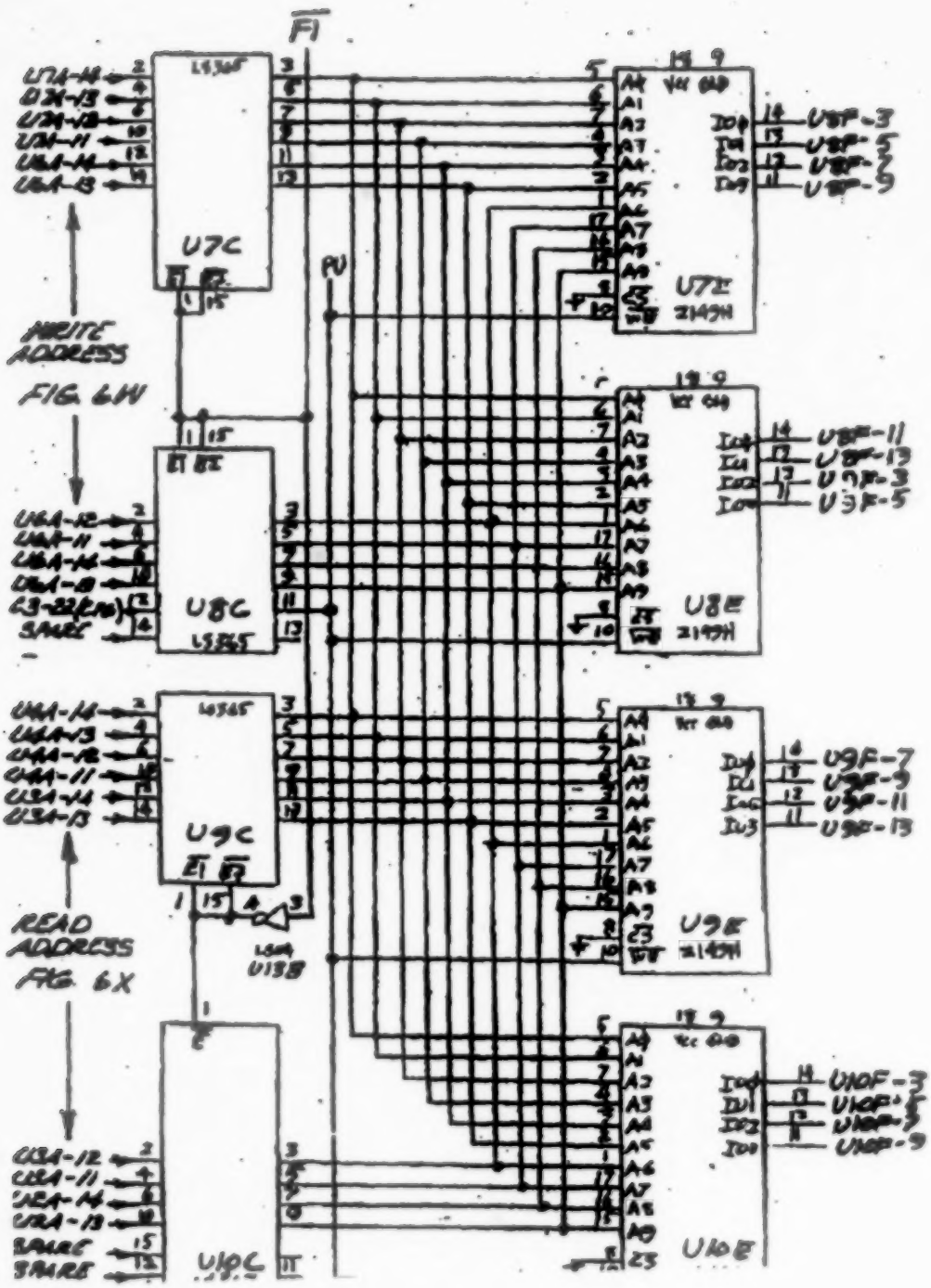
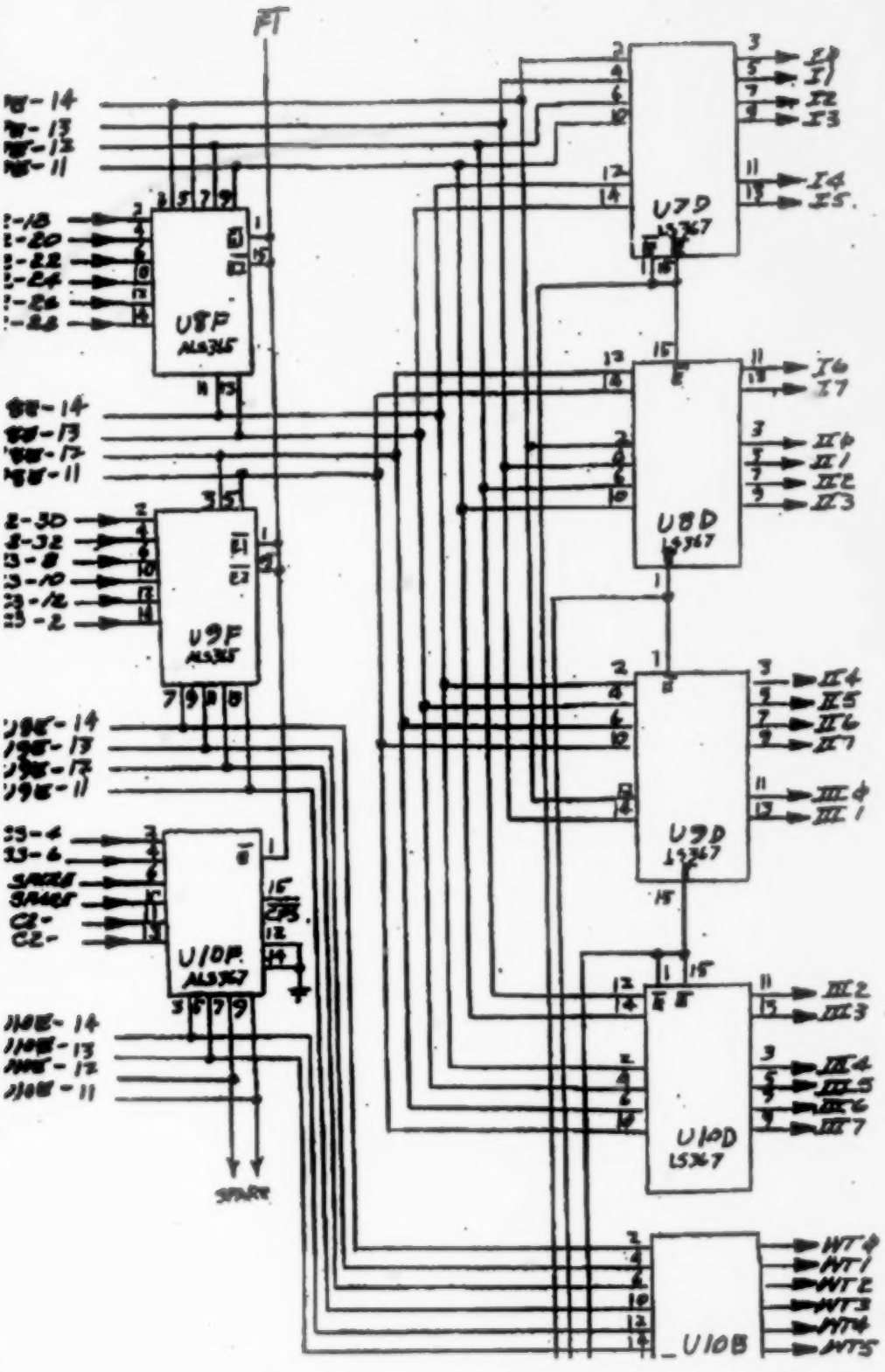

U7B-5
U13B-11
LS00
U2B
LS02
U1B
U1A
LS175
CK
PU
TC
CEP
CET
CP
SR
P3
P2
P1
P0
PE
ALS163
U2A
U6C-10
U6C-6
CFS
CA-2
LS04
U8B
U6C-4
U6C-2
U5C-14
U5C-12
U3A
CPE
CA-6
U7B
LS08
CPD
CA-8
U8B
LS04
U8B
9MHz
U5C-10
Q3

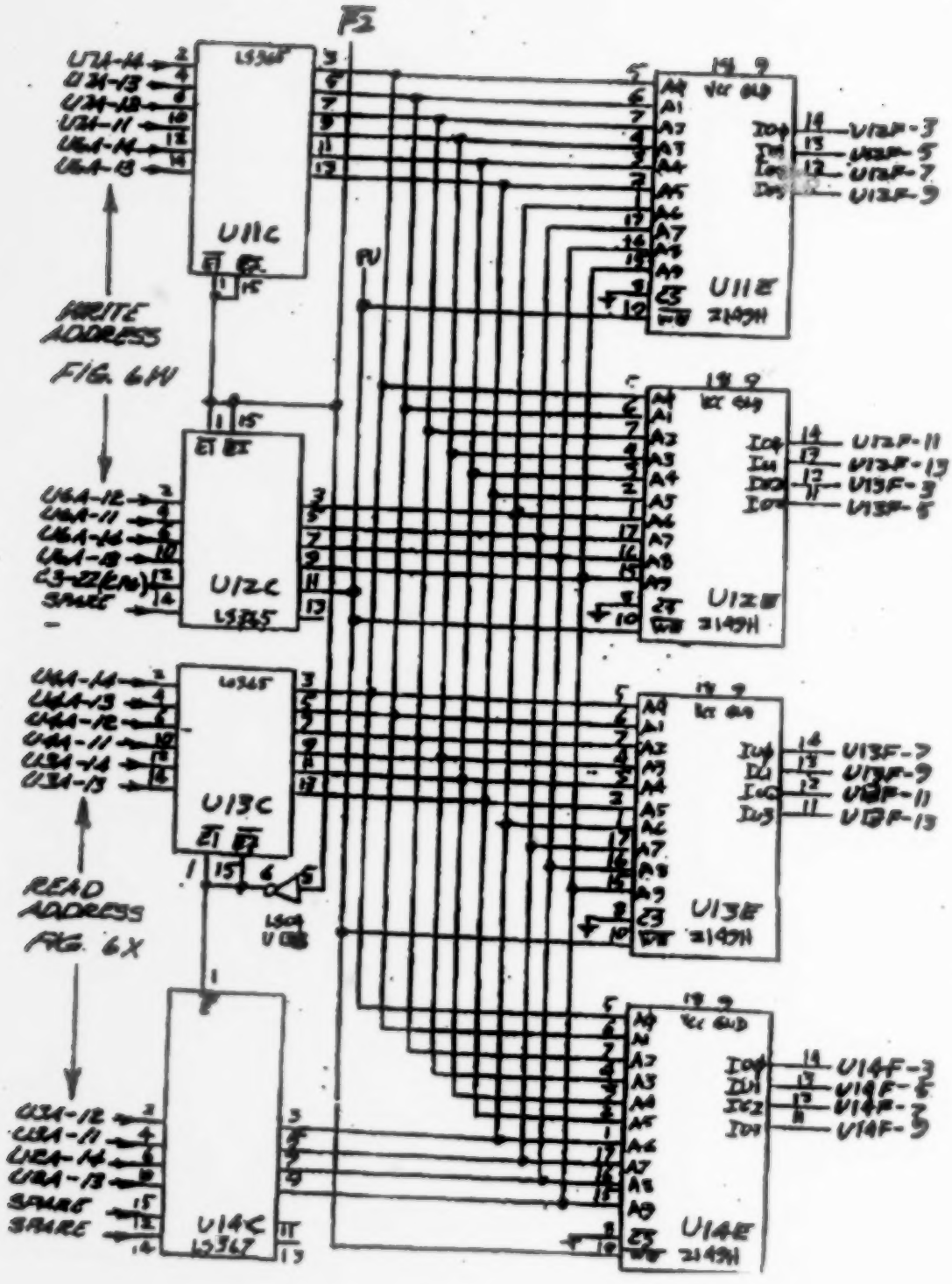
FIG 6X

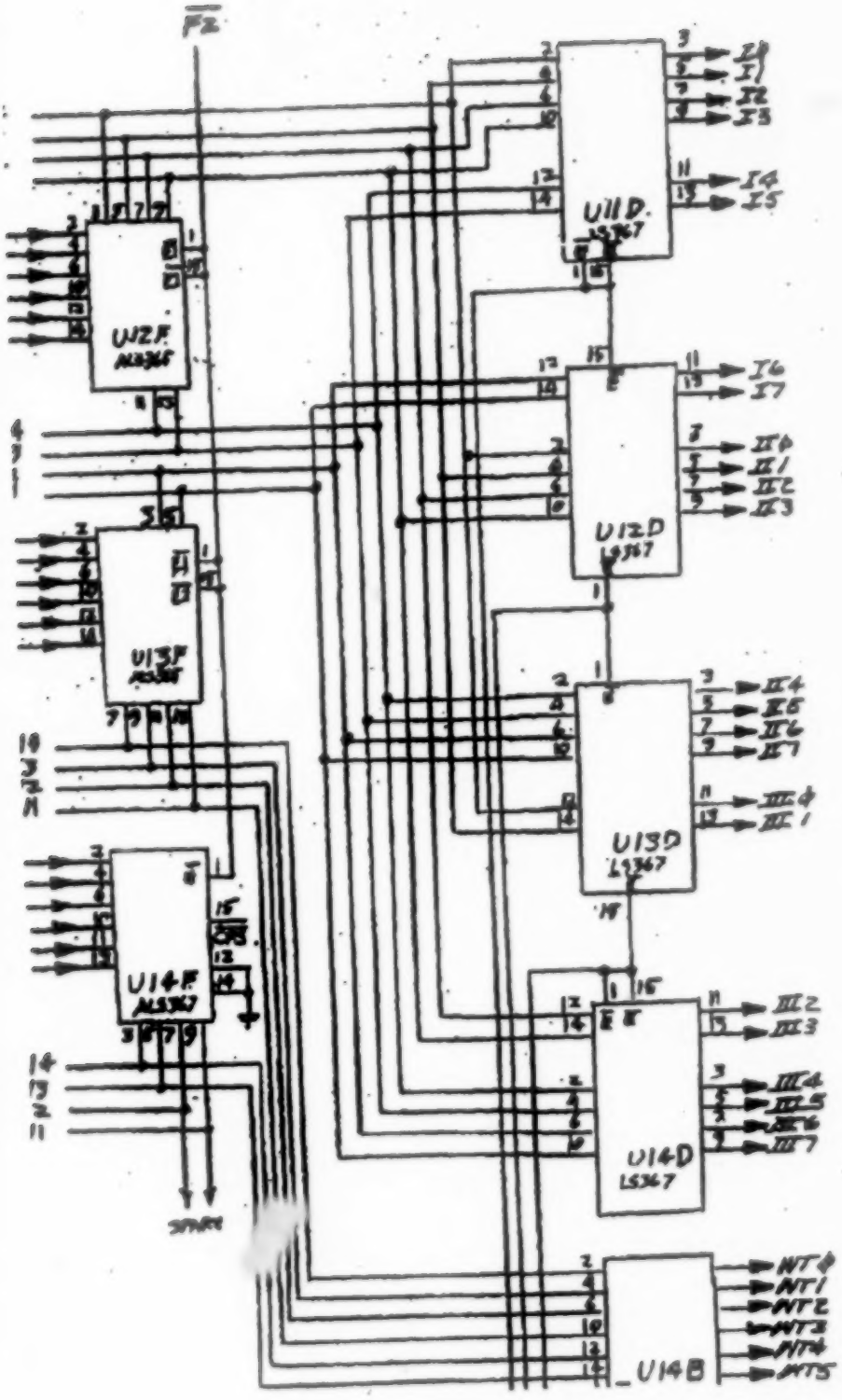

U3C
U4C
U5C
U6C
U3E
U4E
U5E
U6E
WRITE ADDRESS
FIG. 6H
READ ADDRESS
FIG. 6X
U4F-3
U4F-5
U4F-7
U4F-9
U4F-11
U4F-13
U5F-7
U5F-9
U5F-11
U5F-13
U6F-3
U6F-5
U6F-7
U6F-9

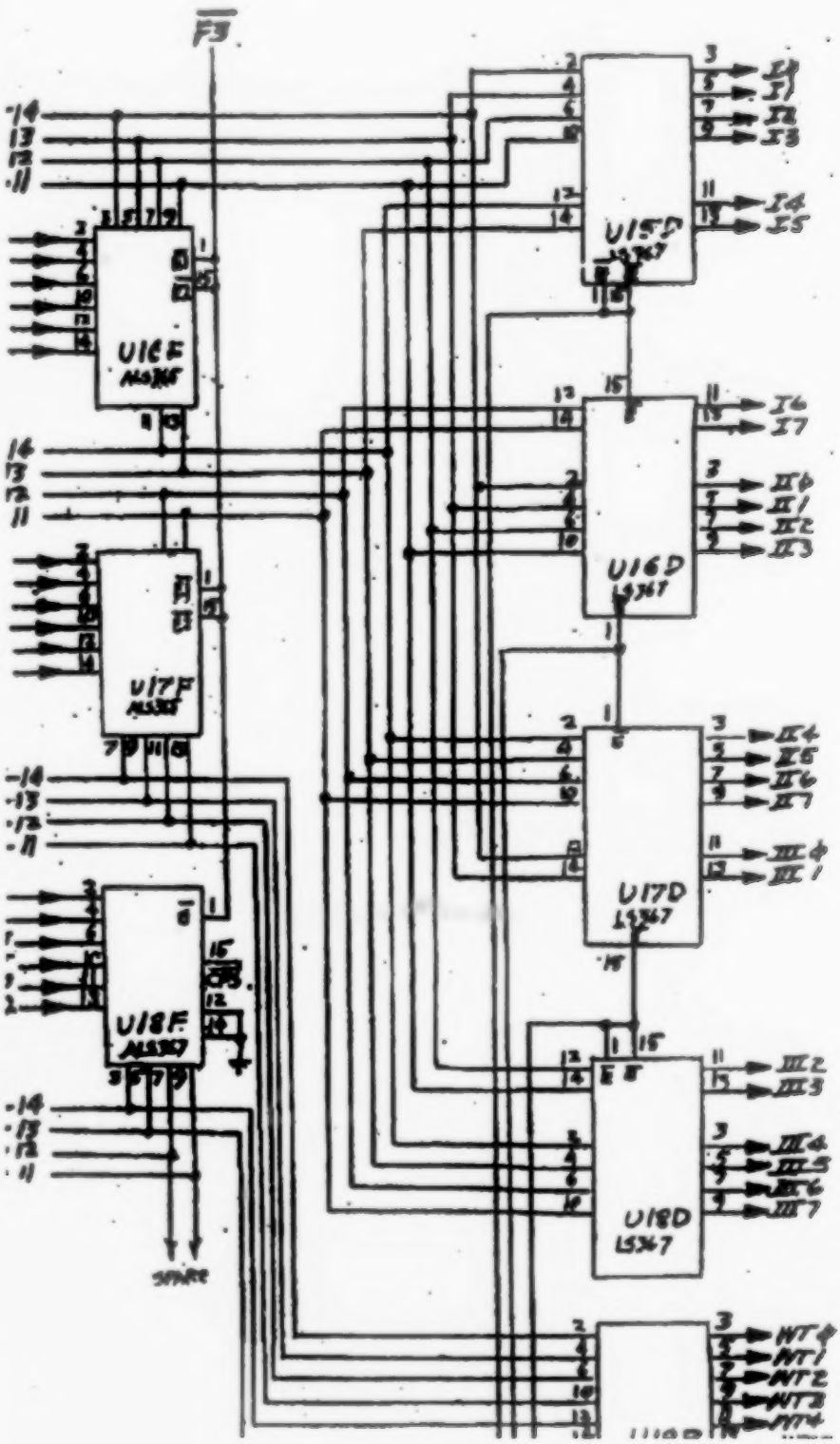

U3D
LS367
U4F
ALS365
U4D
LS367
U5F
ALS365
U5D
LS367
U6F
ALS367
U6D
LS367
116A


F1
PU
U7C
U8C
U9C
U10C
U7E
U8E
U9E
U10E
WRITE ADDRESS
FIG. 6H
READ ADDRESS
FIG. 6X


FT
U8F
ALS365
U9F
ALS365
U10F
ALS367
U7D
LS367
U8D
LS367
U9D
LS367
U10D
LS367
U10B
I0
I1
I2
I3
I4
I5
I6
I7
II0
II1
II2
II3
II4
II5
II6
II7
III0
III1
III2
III3
III4
III5
III6
III7
INT0
INT1
INT2
INT3
INT4
INT5


U11C
U12C
U13C
U14C
U11E
U12E
U13E
U14E
WRITE ADDRESS
FIG. 6H
READ ADDRESS
FIG. 6X
SPARE
SPARE


F2
U11D
LS367
U12F
LS367
U12D
LS367
U13F
LS367
U13D
LS367
U14F
LS367
U14D
LS367
U14B
I0
I1
I2
I3
I4
I5
I6
I7
II0
II1
II2
II3
II4
II5
II6
II7
III0
III1
III2
III3
III4
III5
III6
III7
NT0
NT1
NT2
NT3
NT4
NT5


F3
U16E
U15D
U16D
U17F
U17D
U18F
U18D
SPARE

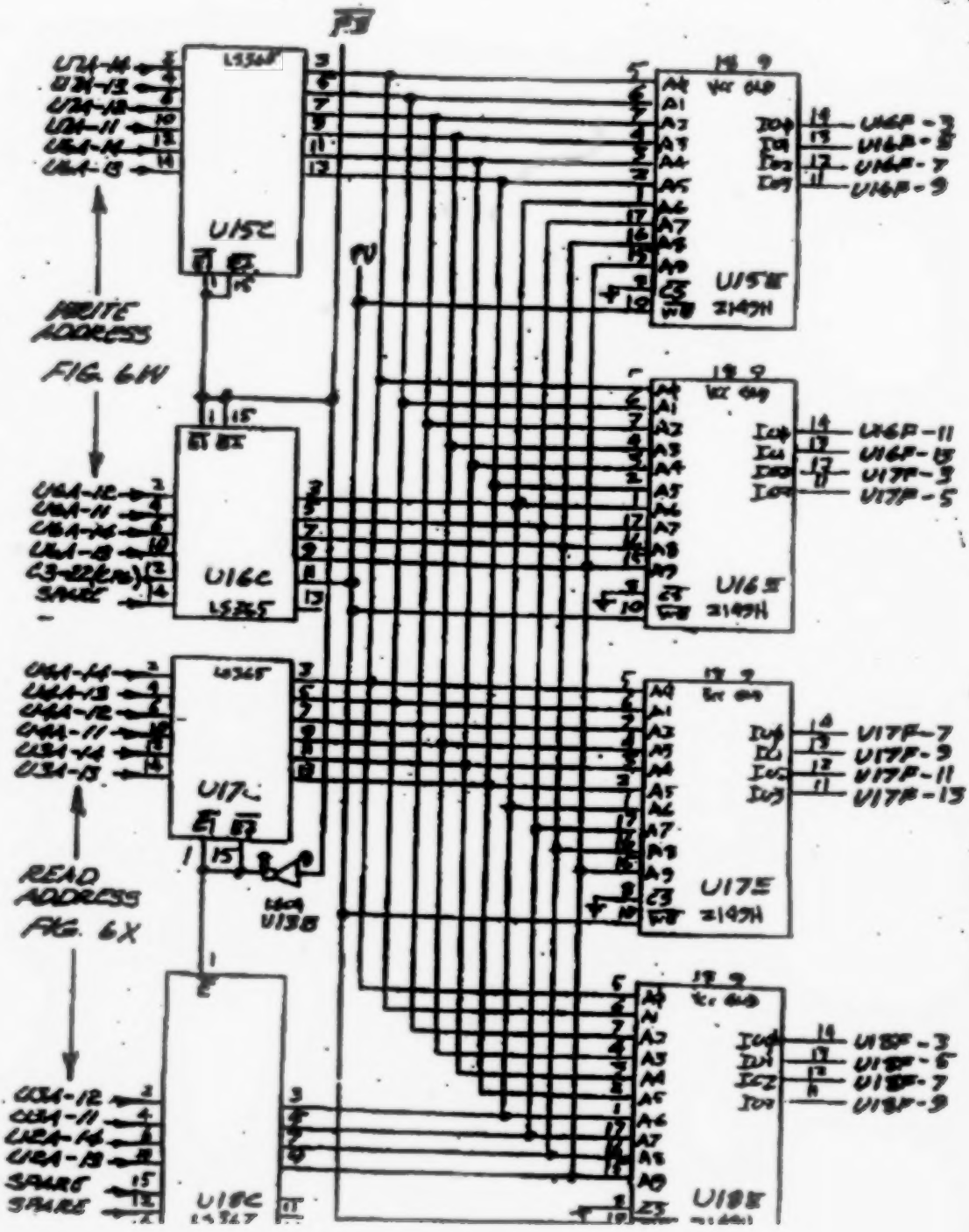
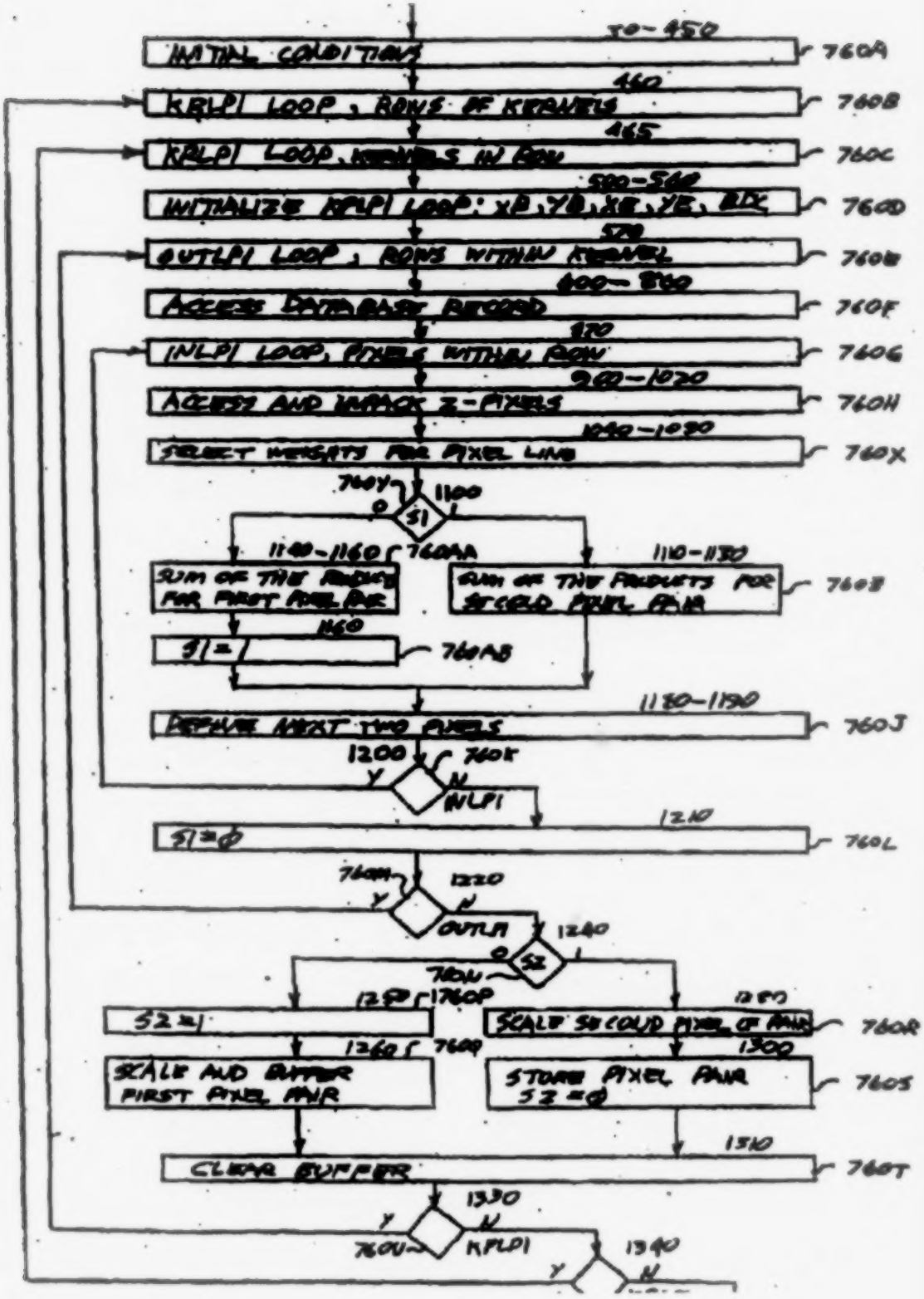

U15C
U16C
U17C
U18C
U15E
U16E
U17E
U18E
WRITE ADDRESS
FIG. 6W
READ ADDRESS
FIG. 6X
SPARE
SPARE

FIG 6AH

FIG6A G


INITIAL CONDITIONS
760A
KRLP1 LOOP, ROWS OF KERNELS
760B
KRLP1 LOOP, KERNELS IN ROW
760C
INITIALIZE KRLP1 LOOP: XB, YB, XE, YE, BIX
760D
OUTLP1 LOOP, ROWS WITHIN KERNEL
760E
ACCESS DATABASE RECORD
760F
INLP1 LOOP, PIXELS WITHIN ROW
760G
ACCESS AND UNPACK 2-PIXELS
760H
SELECT WEIGHTS FOR PIXEL LINE
760X
S1
760Y
1100
SUM OF THE PRODUCTS FOR FIRST PIXEL PAIR
1110-1130
SUM OF THE PRODUCTS FOR SECOND PIXEL PAIR
760Z
S1 =
760AB
PREPARE NEXT TWO PIXELS
760J
1180-1190
1200
760K
INLP1
S1 = 0
760L
1210
760M
1220
OUTLP1
1240
S2
760N
760P
S2 =
760Q
SCALE SECOND PIXEL OF PAIR
760R
1280
SCALE AND BUFFER FIRST PIXEL PAIR
760S
1260
STORE PIXEL PAIR S2 = 0
760S
1300
CLEAR BUFFER
760T
1310
1330
760U
KRLP1
1340

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	
GILBERT P. HYATT	Group Art Unit: Not yet assigned
Serial No. Not yet assigned	Examiner: Not yet assigned
Docket No. 516	
Filed: Not yet assigned	
For: IMPROVED MEMORY ARCHITECTURE HAVING A MULTIPLE BUFFER OUTPUT ARRANGEMENT	

LETTER TO THE OFFICIAL DRAFTSMAN

Hon. Assistant Commissioner For Patents
Washington, D.C. 20231

Sir:

Please amend the drawings as discussed below and as marked in red on the attached copy of the drawings.

In Fig 7A, at the top right side of the drawing; change "FIG 7A" to read --FIG 7--.

CERTIFICATION OF MAILING BY EXPRESS MAIL: I hereby certify that this correspondence is being deposited with the United States Postal Service with Express Mail post office to addressee service under 37 CFR 1.10, postage prepaid, in a package addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231 with the express mail label number [illegible] on the date set forth below.

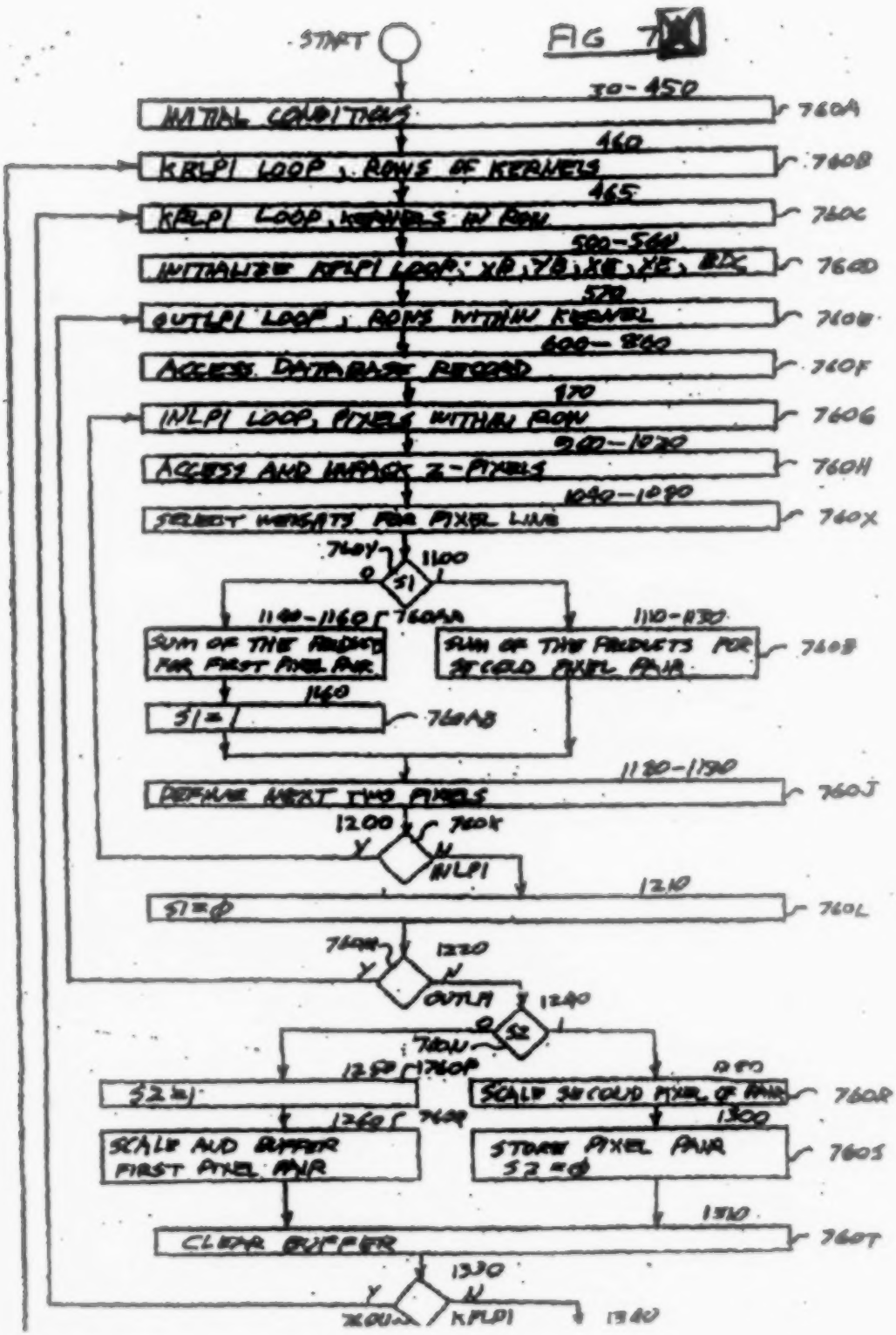
Dated: June 6, 1995

Respectfully submitted,

Gilbert P. Hyatt

Gilbert P. Hyatt
Registration No. 27,647
P.O. Box 81230
Las Vegas, NV 89180
Phone (702) 871-9899

FIG 7


START
30-450
INITIAL CONDITIONS
760A
460
KRLP1 LOOP, ROWS OF KERNELS
760B
465
KRLP1 LOOP, KERNELS IN ROW
760C
500-560
INITIALIZE KFLP1 LOOP: XB, YB, XE, YE, BDC
760D
570
OUTLP1 LOOP, ROWS WITHIN KERNEL
760E
600-860
ACCESS DATABASE RECORD
760F
870
INLP1 LOOP, PIXELS WITHIN ROW
760G
900-1020
ACCESS AND UNPACK 2-PIXELS
760H
1040-1080
SELECT WEIGHTS FOR PIXEL LINE
760X
760Y
1100
S1
1140-1160
760AA
SUM OF THE PRODUCTS FOR FIRST PIXEL PAIR
1110-1130
SUM OF THE PRODUCTS FOR SECOND PIXEL PAIR
760B
1160
S1=1
760AB
1180-1190
DEFINE NEXT TWO PIXELS
760J
1200
760K
INLP1
1210
S1=0
760L
760M
1220
OUTLP1
1240
S2
760N
1280
760P
S2=1
1280
SCALE SECOND PIXEL OF PAIR
760R
1260
760Q
SCALE AND BUFFER FIRST PIXEL PAIR
1300
STORE PIXEL PAIR S2=0
760S
1310
CLEAR BUFFER
760T
1330
KFLP1
1340

No. 10-1219

In the Supreme Court of the United States

DAVID J. KAPPOS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR, UNITED STATES PATENT AND TRADEMARK OFFICE, PETITIONER

v.

GILBERT P. HYATT

ON WRIT OF CERTIORARI TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

VOLUME 3
JOINT APPENDIX

DONALD B. VERRILLI, JR.
Solicitor General
Department of Justice
Washington, D.C. 20530-0001
SupremeCtBriefs@usdoj.gov
(202) 514-2217

Counsel of Record for Petitioner

AARON M. PANNER*
Kellogg, Huber, Hansen, Todd, Evans & Figel, P.L.L.C.
1615 M Street, N.W.
Suite 400
Washington, D.C. 20036
apanner@khhte.com
(202) 723-6871

GREGORY L. ROTH
5712 Parkwest Circle
La Palma, CA 90623
(714) 723-6871

* *Counsel of Record for Respondent*

PETITION FOR A WRIT OF CERTIORARI FILED: APR. 7, 2011
CERTIORARI GRANTED: JUNE 27, 2011

TABLE OF CONTENTS

Page

VOLUME 1

Court of appeals docket entries 1
District court docket entries 4
In re Application of Gilbert P. Hyatt:
Specification (June 6, 1995) 9

VOLUME 2

Specification Diagrams (June 6, 1995) 146

VOLUME 3

Amendment Under 37 C.F.R. § 1.111 (Oct. 15, 1996) 263
Final Office Action (July 30, 1997) 365
Appeal Brief (Sept. 2, 1998) 393

VOLUME 4

Examiner's Answer (Aug. 13, 1999) 541
Reply Brief Under 37 C.F.R. § 1.193(b) (July 31, 2000) 588
Request for Rehearing (Sept. 30, 2002) 670

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Docket No. 516
Serial No. 08/471,702
Group Art Unit: 2415
Examiner: Jeffery Brier

IN RE APPLICATION OF GILBERT P. HYATT

Filed: June 6, 1995
[Received: Oct. 30, 1996]

AMENDMENT UNDER 37 CFR 1.111

For: IMPROVED MEMORY ARCHITECTURE HAVING A MULTIPLE BUFFER OUTPUT ARRANGEMENT

Hon. Assistant Commissioner For Patents
Washington, D.C. 20231

Sir:

In response to the Action dated June 26, 1916 (Paper No. 12); please amend the present application as set forth in Section II hereinafter as provided for under 37 CFR 1.111. Further, the Applicant requests reconsideration for the reasons set forth in Section I hereinafter pursuant to 37 CFR 1.111.

I REMARKS

1.1 ALLEGED ABANDONMENT OF THE INVENTION

The Claims stand rejected for an alleged abandonment of the invention under 35 U.S.C. 102(c). The Applicant respectfully traverses this rejection.

At the outset, it is noted for the record that the rejection does not question the chain of copending [ILLEGIBLE] the ancestor applications for a proper claim of priority under 35 U.S.C. 120. It is also noted that nowhere in the rejection has there been any showing or other evidentiary finding that Applicant intended to abandon the invention which is the subject of the above identified application. It is made clear from MPEP 2134 that intent to abandon the invention will not be imputed, and every reasonable doubt should be resolved in favor of the inventor. Ex parte Dunne, 20 USPQ2d 1479 (Bd. Pat. App. & Inter. 1991). Delay in filing, as stated by the Board in the Dunne decision, is not a sufficient basis from which to infer the requisite intent to abandon under 35 U.S.C. 102(c). Moore v. United States, 194 USPQ 423 (Ct. Cl. Tr. Div. 1977).

Abandonment under 35 U.S.C. 102(c) requires a deliberate, though not necessarily express, surrender of any rights to a patent. To abandon the invention, the inventor must intend a dedication to the public. Such dedication may be either express or implied, by actions or inactions of the inventor. Delay alone is insufficient. The Applicant has not taken any such deliberate step to surrender any rights to a patent and the rejection does not present contrary evidence.

The MPEP makes clear that any inference of abandonment of subject matter disclosed but not claimed in a previously issued patent is rebuttable by an application filed at any time before a statutory bar arises. Thus, a rejection of a claim of a patent application under 35 U.S.C. 102(c) that is predicated solely on the issuance of a patent which discloses the subject matter of the claim in the application without claiming it would be improper, regardless of whether there is copendency between the application at issue and the application which issued as the patent. In re Gibbs, 437 P.2d 486, 168 USPQ 578 (CCPA 1971).

It is axiomatic that the mere lapse of time will not bar a patent. Cf. In re Henriksen, 399 F.2d 253, 158 USPQ 224 where the court stated that it was their view, as the judiciary, that it is for the Congress to decide, with the usual opportunity for public hearing and debate, whether a restriction should be placed on the number of applications which may be filed claiming continuous benefit under 39 U.S.C. 120 to several prior filed applications. There can be little doubt from Henriksen that the Applicant has a legal right to file multiple applications claiming benefit under 35 U.S.C. 120 to earlier filed applications without fear that doing so is legally detrimental to the Applicant.

The cases cited in the rejection have been reviewed in great detail and none of the cited cases deals with abandonment under 35 U.S.C. 102(c). MPEP 2134 (Rev. I, Sept. 1995) cautions against rejections based upon abandonment of the invention as such rejections require intent and, unless intent can be shown, any doubt is to be resolved in favor of the inventor. Thus, the rejection under 35 U.S.C. 102(c) is clearly improper and without

legal merit, in view of the Examiner's own Manual guidance as well as the Board decision in Ex parte Dunne, supra as well as Moore v. United States, supra.

Accordingly, the 35 USC 102(c) rejection is untenable in light of the foregoing comments and withdrawal of the rejection is respectfully requested.

1.2 DOUBLE PATENTING REJECTIONS

1.2.1 General Discussion

Claims 1-15 were provisionally rejected under 35 U.S.C. 101 for double patenting over copending applications; claims 1-8 were provisionally rejected for obviousness type, double patenting over the '816 patent in view of Preiss; and claims 1-15 were provisionally rejected for same type double patenting over the '951 patent (Paper No. 2). The Applicant respectfully traverses the double patenting rejections for the reasons set forth below.

Claims 1-15 of the instant application have been significantly amended and hence distinguish over the claims of the copending applications. Further, the claims of the copending applications have been (or are being) significantly amended and hence distinguish over the claims of the instant applications. Hence, the double patenting rejections are not relevant.

1.2.2 Traverse Of The Obviousness-Type Double Patenting Rejection Over Patent No. 4,551,816

Claims 1-8 stand rejected for obviousness-type double patenting over claims 6, 8, 10, and 16 of Patent. No. 4,551,816 in view of Preiss (Paper No. 2). However, the rejection fails to make a prima facie rejection, such as by reading the claims of the application and the claims of

the patent there between. Further, the Action establishes that Preiss is an improper reference. See Section 1.4 below.

1.2.3 Traverse Of The Disclosure-Type Double Patenting Rejection Over Patent No. 4,954,951

Claims 1-15 stand rejected for disclosure-type double patenting over claims 7 and 12 of Patent No. 4,954,951 (Paper No. 2). The Applicant respectfully traverses this rejection for the reasons discussed below.

The rejection improperly relies on the disclosure in the patent to meet the limitations in the application claims. The rejection erroneously asserts that use of the phrase "comprising" permits such importing of limitations from the disclosure. The rejection relies on In re Schneller, but In re Schneller does not support this remarkable theory. In fact In re Schneller expressly prohibits such a rejection. See Section 1.2.4 below. Further, the law of the Federal Circuit specifically requires that the application claims be compared with the patent claims, not with the patent disclosure. The patent disclosure may not be used as prior art, In re Vogel, 422 F.2d 438, 16USPQ 619, 622 (CCPA, 1970).

1.2.4 Reliance On The Disclosure for Double Patenting Violates The Law Of The Federal Circuit And Violates In Re Schneller

The law of the Federal Circuit requires comparison of the claims for double patenting. It is error to rely on the disclosure for unclaimed features. In re Schneller also agrees that it is the claims, not the disclosure, that must be compared.

> "By reason of the copendency, only the claims of the patent can be considered as support for the rejection, its disclosure being looked to only to determine the meaning of the claims, which are to be read in the light of the specification. [emphasis added] In re Schneller, 158 USPQ 210, at 213

paragraph 7 of the Action purports to reject the instant claims on a nonstatutory theory of double patenting based upon In re Schneller, 397 F.2d 350 (CCPA, 1968). This rejection cannot stand for three reasons. First, the rejection violates MPEP 804. Second, this supposed ground of rejection violates the law of the Court of Appeals for the Federal Circuit. Third, the Schneller case requires a very specific fact situation that does not apply to the present claims.

MPEP 804 states:

> "In making an analysis of this type (In re Schneller) of nonstatutory double patenting, the first question is: Is the subject matter recited in the claims of the application fully disclosed in the patent and covered by a claim in the patent? If the answer is no, double patenting does not exist. [emphasis added]

Because not one of the claims of the instant application is "covered by a claim in the patent", double patenting does not exist. Patent claims 7 and 12 have limitations that are not found in any of the claims of the instant application. Hence, In re Schneller does not apply to the claims of the instant application. The Examiner is respectfully requested to identify any claims in the patent. If any limitation that is recited in a claim of the patent is not recited in the instant application, the claim of the

instant application is not "covered" and hence In re Schneller type double patenting does not exist. The disclosure in the patent is irrelevant to this type of double patenting.

The Schneller case was in conflict with previous CCPA cases, such as In re Sutherland, 347 F.2d 1009, 146 USPQ 485 (CCPA 1965). The Schneller case apparently cast the law on double patenting into a state of confusion because, shortly thereafter, the CCPA found it necessary to restate the law of double patenting. A unanimous five judge panel stated:

> The proceedings below in this case indicate the advisability of restatement of the law of double patenting as enunciated by this court. In re Vogel, 422 F.2d 438, 164 USPQ 619, 621 (CCPA, 1970).

Vogel then proceeded to restate the law of double patenting as including (1) the 35 U.S.C. para. 101 "same invention", i.e., "identical subject matter" double patenting and (2) obviousness double patenting. The court stated:

> As we have said many times, "invention" here means what is defined by the claims, whether new or old, obvious or unobvious; it must not be used in the ancient sense of "patentable invention," or hopeless confusion will ensue. 164 USPQ at 621.
>
> The second analysis question is: Does any claim in the application define merely an obvious variation of an invention disclosed and claimed in the patent? In considering the question, the patent disclosure may not be used as prior art. [emphasis added] 164 USPQ at 622.

The restatement of the law by Vogel has been consistently followed in subsequent decisions. See, e.g., In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010, 2016 (CAFC, 1993); In re Braat, 937 F.2d 589, 19 USPQ2d 1289, 1292 (CAFC, 1991); In re Kaplan, 789 F.2d 1574, 229 USPQ 678 CAFC, 1986); In re Longi, 759 F.2d 887, 225 USPQ 645 (CAFC, 1985). Applicant has found no case subsequent to Vogel where either the CCPA or the CAFC has deviated from the restatement of the law of double patenting found in Vogel. Not only have the courts consistently followed Vogel, the CAFC has specifically denounced the "domination" type of analysis found in Schneller, stating:

> In possibly simpler terms, one patent dominates another if a claim of the first patent reads on a device built or process practiced according to the second patent disclosure. This commonplace situation is not, per se, double patenting as the board seemed to think. In re Kaplan, 789 F.24 1574, 229 USPQ678, 681 (CAFC, 1986).

Clearly, the Schneller type of analysis is not valid law.

Even if Schneller represented valid law, the claims of the present application do not comply with the criteria that was present in the Schneller case. That case involved claims directed to a unitary device, a single unitary wire having selected bends, not a combination of elements as recited in the instant claims. 158 USPQ at 216. Furthermore, in the present case the patent claims do not cover the present application claims. The instant application claims are directed to a completely different, independent and distinct invention. A system can be made in accordance with the instant claims that is not

covered by the other claims. In re Schneller is completely inapplicable.

1.3 37 CFR 1.78(B) OBJECTION

Claims 1-15 stand objected to as conflicting with the claims of copending applications (Paper No. 2). However, claims 1-15 of the instant application have been significantly amended and hence distinguish over the claims of the copending applications. Further, the claims of the copending applications have been (or are being) significantly amended and hence distinguish over the claims of the instant application.

1.4 35 USC 103 REJECTIONS

Claims 1-3 and 5-7 stand rejected under 35 USC 103 over Preiss (Paper No. 2). The Applicant respectfully traverses this rejection for the following representative reason. The rejection acknowledges that Preiss does not meet the buffer memory limitation.

Claim 4 stands rejected under 35 USC 103 over Preiss and Swanson (Paper No. 2). The Applicant respectfully traverses this rejection for the following representative reasons. As with claims 1-3 and 5-7, claim 4 is limited to the novel buffer memory that is not taught by Preiss. Such a defect is not cured by Swanson. Further, Swanson does not teach the claimed multiple line double buffer set forth in claim 4 and certainly not the recitation "with less then a double buffer memory."

Claim 8 stands rejected under 35 USC 103 over Preiss and an allegation of well known prior art (Paper No. 2). The Applicant respectfully traverses this rejection for the following representative reasons. As with claims 1-3 and 5-7, 8 is limited to the novel ROM based

image memory, which is not taught by Preiss. The rejection is based upon ROMs being well known. However, Preiss has no use for ROMs in his frame buffer. If Preiss used ROMs in his frame buffer. he could not be able to store the vectors being generated by his vector generator because the information in an ROM cannot be changed in such a manner.

Claims 9-14 stand rejected under 35 USC 103 over Widergren (Paper No. 2) and over Cease or Forquer (Paper No. 2). The Applicant respectfully traverses this rejection for the following representative reason. The Board in the '211 application interpreted claim 9 as "in parallel" modifing "words", not "plurality", in "a sequence of a plurality of words in parallel". However, interpreting claim 9 in view of the specification clearly establishes that "in parallel" modifies "plurality", not "words". The disclosure teaches "a sequence of a (parallel) plurality of words". [parenthetical expression added] Hence, claims 9-14 clearly distinguish over the references.

Claim 15 stands rejected under as 35 USC 103 over Goldberg (Paper No. 2). The Applicant respectfully traverses this rejection for the following representative reason. The rejection admits that Goldberg does not disclose "means for generating information." It would not be obvious to provide such an element with Goldberg because Goldberg has no use for such an element. Goldberg teaches a gray scale correction arrangement, not an information generating arrangement.

II AMENDMENTS

2.1 AMENDMENTS TO THE CLAIMS

Please amend claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, and 81-85 as rewritten in Appendix A attached hereto. Please cancel claims 15, 16; 21, 31-33, 38-41, 46-48, 53-80, and 86-94 and add new claims 95-172 as set ferth in Appendix A attached hereto.

III CONCLUSION

The Applicant has demonstrated that each of the rejected claims patentably distinguishes over the applied references. The Applicant has further demonstrated that the application has not been abandoned. The Applicant has further demonstrated that there is no double patenting. It is therefore respectfully requested that the rejections be withdrawn.

CERTIFICATION OF MAILING: I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231 on October 15, 1996.

Respectfully submitted,

Dated: Oct. 15, 1996

/s/ GILBERT P. HYATT
Gilbert P. Hyatt
Registration No. 27,647
[address and phone number omitted]

APPENDIX A

1. A [display] memory system comprising:

a data decompressed video image input circuit generating data decompressed video image information;

[an] a two dimensional pixel block image memory [for] storing a two dimensional array of blocks of video pixel image information, the two dimensional array of blocks of video pixel image information arranged in a two dimensional array of rows and columns of blocks of video pixel image information;

an address generator generating write addresses and generating read addresses;

a memory writing circuit coupled to the data decompressed video image input circuit, coupled to the two dimensional pixel lock image memory, and coupled to the address generator, the memory writing circuit writing the two dimensional array of blocks of video pixel image information into the two dimensional pixel block image memory in response to the data decompressed video image information generated by the data decompressed video image input circuit and in response to the write addresses generated by the address generator;

an accessing [means for accessing a plurality of lines of] circuit coupled to the two dimensional pixel block image memory and coupled to the address generator, the accessing circuit generating accessed blocks of video pixel image information by accessing the two dimensional array of blocks of video pixel image information from said two dimensional pixel block image memory in response to the read addresses generated by the address generator;

a vector generator generating two dimensional vector information;

a two dimensional vector processor coupled to the accessing circuit and coupled to the vector generator, the two dimensional vector processor generating two dimensional vector processed image information in response to the accessed blocks of video pixel image information accessed by the accessing circuit and in response to the two dimensional vector information generated by the vector generator;

a buffer memory coupled to the accessing circuit and coupled to the two dimensional vector processor, the buffer memory [for] storing [a plurality of lines of] buffered blocks of video pixel image information in response to the [accessing of a plurality of lines of] accessed blocks of video pixel image information [with] accessed by said accessing circuit [means] and storing buffered two dimensional vector processed image information in response to the two dimensional vector processed image information generated by the two dimensional vector processor; [*and*]

[a plurality of registers for storing image information accessed from said buffer memory;]

a two dimensional spatial [filter for] processor coupled to the buffer memory and generating data compressed video [filtered] image information in response to the buffered blocks of video pixel image information stored in said buffer memory and in response to the buffered two dimensional vector processed image information stored in said buffer memory [plurality of said registers; and

means for displaying the filtered image information].

2. [The] A memory system [as set forth in claim 1 above,] comprising:

a data decompressed video image input circuit generating data decompressed video image information;

a two dimensional pixel block image memory [wherein said plurality of registers include means for] storing a two dimensional array of blocks of video pixel image information, [kernel of pixels.] the two dimensional array of blocks of video pixel image information arranged in a two dimensional array of rows and columns of blocks of video pixel image information;

an address generator generating write addresses and generating read addresses;

a memory writing circuit coupled to the data decompressed video image input circuit, coupled to the two dimensional pixel block image memory, and coupled to the address generator, the memory writing circuit writing the two dimensional array of blocks of video pixel image information into the two dimensional pixel block image memory in response to the data decompressed video image information generated by the data decompressed video image input circuit and in response to the write addresses generated by the address generator;

an accessing circuit coupled to the two dimensional pixel block image memory and coupled to the address generator, the accessing circuit generating accessed blocks of video pixel image information by accessing the two dimensional array of blocks of video pixel image information from said two dimensional pixel

block image memory in response to the read addresses generated by the address generator;

a vector generator generating two dimensional vector information;

a two dimensional vector processor coupled to the accessing circuit and coupled to the vector generator, the two dimensional vector processor generating data compressed video image information in response to the accessed blocks of video pixel image information accessed by the accessing circuit and in response to the two dimensional vector information generated by the vector generator; and

a buffer memory coupled to the two dimensional vector processor and storing buffered data compressed video image information in response to the data compressed video image information in response to the data compressed video image information generated by the two dimensional vector processor.

3. [The] A memory system [as set forth in claim 1 above,] comprising:

a data decompressed video image input circuit generating data decompressed video image information;

a two dimensional pixel block image memory storing a two dimensional array of blocks of video pixel image information, the two dimensional array of blocks of video pixel information arranged in a two dimensional array of rows and columns of blocks of video pixel image information;

an address generator generating write addresses and generating read addresses;

a memory writing circuit coupled to the data decompressed video image input circuit, coupled to the two dimensional pixel block image memory, and coupled to the address generator, the memory writing circuit writing the two dimensional array of blocks of video pixel image information into the two dimensional pixel block image memory in response to the data decompressed video image information generated by the data decompressed video image input circuit and in response to the write addresses generated by the address generator;

an accessing circuit coupled to the two dimensional pixel block image memory and coupled to the address generator, the accessing circuit generating accessed blocks of video pixel image information by accessing the two dimensional array of blocks of video pixel image information from said two dimensional pixel block memory in response to the read addresses generated by the address generator;

a processor coupled to the accessing circuit and generating data compressed video image information in response to the accessed blocks of video pixel information generated by the accessing circuit; and

[wherein said] a buffer memory coupled to the processor and [includes means for precessing between the plurality of lines to provide changes in the] storing buffered data compressed video image information in response to the data compressed video image information generated by said processor [plurality of registers].

4. [The] A memory system [as set forth in claim 1 above,] comprising:

a data decompressed video image input circuit generating data decompressed video image information;

a two dimensional pixel block image memory coupled to the data decompressed video image input circuit and storing a two dimensional array of blocks of video pixel image information in response to the data decompressed video image information generated by the data decompressed video image input circuit, the two dimensional array of blocks of video pixel image input circuit, the two dimensional array of blocks of video pixel image information arranged in a two dimensional array of rows and columns of blocks of video pixel image information;

an address generator generating read addresses;

an accessing circuit coupled to the two dimensional pixel block image memory and coupled to the address generator, the accessing circuit generating accessed blocks of video pixel image information by accessing the two dimensional array of blocks of video pixel image memory in response to the read addresses generated by the address generator;

a processor coupled to the accessing circuit and generating data compressed video image information in response to the accessed blocks of video pixel information generated by the accessing circuit; and

[wherein said] a buffer memory coupled to the processor and [includes means for providing double] storing buffered [capability with less than a double buffer of memory] data compressed video image information in response to the data compressed video image information generated by the processor.

5. [The] A memory system [as set forth in claim 1 above,] comprising:

a data decompressed video image input circuit generating data decompressed video image information;

a two dimensional pixel block image memory storing a two dimensional array of blocks of video pixel image information, the two dimensional array of blocks of video pixel image information arranged in a two dimensional array of rows and columns of blocks of video pixel image information;

a memory writing circuit coupled to the data decompressed video image input circuit and coupled to the two dimensional pixel block image memory, the memory writing circuit writing the two dimensional array of blocks of video pixel image information into the two dimensional pixel block image memory in response to the data decompressed video image information generated by the data decompressed video image input circuit;

an accessing circuit coupled to the two dimensional pixel block image memory and generating accessed blocks of video pixel image information by accessing the two dimensional array of blocks of video pixel image information from said two dimensional pixel block image memory;

a vector generator generating two dimensional vector information;

a two dimensional vector processor coupled to the accessing circuit and coupled to the vector generator, the two dimensional vector processor generating data compressed video image information in response to the accessed blocks of video pixel image information accessed by the accessing circuit and in response to the two dimensional vector information generated by the vector generator, and

[wherein said] a buffer memory coupled to the two dimensional vector processor and storing [includes a double] buffered data compressed video image information in response to the data compressed video information generated by the two dimensional vector processor [implemented with a plurality of RAMs].

6. [The] A memory system [as set forth in claim 1 above,] comprising:

a data decompressed video image input circuit generating input data decompressed video frequency domain image information;

a two dimensional frequency domain block image memory storing a two dimensional array of blocks of video frequency domain image information, the two dimensional array of blocks of video frequency domain image information arranged in a two dimensional array of rows and columns of blocks of video frequency domain image information;

an address generator generating write addresses and generating read addresses;

a memory writing circuit coupled to the data decompressed video image input circuit, coupled to the two dimensional frequency domain block image memory, and coupled to the address generator, the memory writing circuit writing to the two dimensional array of blocks of video frequency domain information into the two dimensional frequency domain block image memory in response to the input data decompressed video frequency domain image information generated by the data decompressed video image input circuit and in response to the write addresses generated by the address generator;

an accessing circuit coupled to the two dimensional frequency domain block image memory and coupled to the address generator, the accessing circuit generating accessed blocks of video frequency domain image information by accessing the two dimensional array of blocks of video frequency domain image information from said two dimensional frequency domain image information from said two dimensional frequency domain block image memory in response to the read addresses generated by the address generator;

a two dimensional frequency domain transform processor coupled to the accessing circuit and generating data compressed video image information in response to the accessed blocks of video frequency domain image information accessed by the accessing circuit; and

[wherein said] a buffer memory coupled to the two dimensional frequency domain transform processor and storing buffered data compressed video image information [includes a first] in response to the data compressed video image information generated by the two dimensional frequency domain transform processor [first out memory implemented with a plurality of RAMs].

7. [The] A memory system [as set forth in claim 1 above,] comprising:

a data compressed video image input circuit generating data decompressed video frequency domain image information;

a two dimensional frequency domain block image memory coupled to the data decompressed video image input circuit and storing a two dimensional array of blocks of video frequency domain image information in

response to the data decompressed video frequency domain image information generated by the data decompressed video image input circuit, the two dimensional array of blocks of video frequency domain image information arranged in a two dimensional array of rows and columns of blocks of video frequency domain image information, wherein said two dimensional frequency domain block image memory includes a plurality of random access memories; [RAMs.]

an address generator generating read addresses;

an accessing circuit coupled to the two dimensional frequency domain block image memory and coupled to the address generator, the accessing circuit generating accessed blocks of video frequency domain image information by accessing the two dimensional array of blocks of video frequency domain image information from said two dimensional frequency domain block image memory in response to the read addresses generated by the address generator;

a two dimensional frequency domain transform processor coupled to the accessing circuit and generating data compressed video image information in response to the accessed blocks of video frequency domain image information accessed by the accessing circuit; and

a buffer memory coupled to the two dimensional frequency domain transform processor and storing buffered data compressed video image information in response to the data compressed video image information generated by the two dimensional frequency domain transfer processor.

8. [The] A memory system [as set forth in claim 1 above,] comprising:

a data decompressed video image input circuit generating input data decompressed video frequency domain image information;

a two dimensional frequency domain block [wherein said] image memory [includes a plurality of ROMs.] storing a two dimensional array of blocks of video frequency domain image information, the two dimensional array of blocks of video frequency domain image information arranged in a two dimensional array of rows and columns of blocks of video frequency domain image information;

a memory writing circuit coupled to the data decompressed video image input circuit and coupled to the two dimensional frequency domain block image memory, the memory writing circuit writing the two dimensional array of blocks of video frequency domain image information into the two dimensional frequency domain block image memory in response to the input data decompressed video frequency domain image information generated by the data decompressed video image input circuit;

an accessing circuit coupled to the two dimensional frequency domain block image memory and generating accessed blocks of video frequency domain image information by accessing the two dimensional array of blocks of video frequency domain image information from said two dimensional frequency domain block image memory;

a two dimensional frequency domain transform processor coupled to the accessing circuit and generat-

ing data compressed video image information in response to the accessed blocks of video frequency domain image information accessed by the accessing circuit; and

a buffer memory coupled to the two dimensional frequency domain transform processor and storing buffered data compressed video image information in response to the data compressed video image information generated by the two dimensional frequency domain transform processor.

9. A buffer memory system comprising:

a data decompressed video image input circuit generating [means for receiving] input data decompressed video frequency domain image information at a first word rate;

a two dimensional frequency domain block memory [means for] storing [the received] a two dimensional array of blocks of video frequency domain image information, the two dimensional array of blocks of video frequency domain image information arranged in a two dimensional array of rows and columns of blocks of video frequency domain image information; [and]

an address generator generating write addresses and generating read addresses;

a memory writing circuit coupled to the data decompressed video image input circuit, coupled to the two dimensional frequency domain block memory, and coupled to the address generator, the memory writing circuit writing the two dimensional array of blocks of video frequency domain image information into the two dimensional frequency domain block image memory in response to the input data decompressed video frequency domain image information generated by the data decom-

pressed video image input circuit and in response to the write address generated by the addresses generator;

a memory reading circuit coupled to the two dimensional frequency domain block memory and coupled to the address generator, the memory reading circuit accessing block of video frequency domain image information in response to the two dimensional array of blocks of video frequency domain image information stored in the two dimensional frequency domain block memory and in response to the read addresses generated by the address generator;

a vector generator generating two dimensional vector information;

a two dimensional vector processor coupled to the memory reading circuit and coupled to the vector generator, the two dimensional vector processor generating two dimensional vector processed image information in response to the blocks of video frequency domain image information accessed by the memory reading circuit and in response to the two dimensional vector information generated by the vector generator;

a two dimensional frequency domain transform processor coupled to the two dimensional vector processor and generating data compressed video image information in response to the two dimensional vector processed image information generated by the two dimensional vector processors; [*and*]

an output circuit coupled to the two dimensional frequency domain transform processor and [means for] outputting the data compressed video image information [stored in said storing means in parallel firm] at a second word rate that is greater than the first word rate.

10. [The] A buffer memory system [as set forth in claim 9 above,] comprising:

a data decompressed video image input circuit generating data decompressed video image [where the] information at a first word rate;

a two dimension pixel block memory storing a two dimensional array of blocks of video pixel image [received with said receiving means is a serial sequence of words and where the] information, the two dimensional array of blocks of video pixel image information arranged in a two dimensional array of rows and columns of blocks of video pixel image information;

an address generator generating write addresses and generating read addresses;

a memory writing circuit coupled to the data decompressed video image input circuit, coupled to the two dimensional pixel block memory, and coupled to the address generator, the memory writing circuit writing the two dimensional array of blocks of video pixel image information into the two dimensional pixel block image memory in response to the data decompressed video image information generated by the data decompressed video image input circuit and in response to the write addresses generated by the address generator;

a pixel block memory reading circuit coupled to the two dimensional pixel block memory and coupled to the address generator, the pixel block memory reading circuit accessing blocks of video pixel image information in response to the two dimensional array of blocks of video pixel image information stored in the two dimensional pixel block memory and in response to the read addresses generated by the address generator;

a vector generator generating two dimensional vector information;

a two dimensional vector processor coupled to the pixel block memory reading circuit and coupled to the vector generator, the two dimensional vector processor generating data compressed video image information in response to the blocks of video pixel image information accessed by the pixel block memory reading circuit and in response to the two dimensional vector information generated by the vector generator; and

an output circuit coupled to the two dimensional vector processor and [with said] outputting [means is a parallel sequence of words, where] the data compressed video image information at a second word rate [of the parallel words] that is greater than the first word [of the serial words].

11. [The] A buffer memory system [as set forth in claim 9 above,] comprising:

a data compressed video image input circuit generating data decompressed video image [where the] information at a first word rate;

a two dimensional pixel block memory storing a two dimensional array of blocks of video pixel image [received with said receiving means is a serial sequence of words and where the] information, the two dimensional array of blocks of video pixel image information arranged in a two dimensional array of rows and columns of blocks of video pixel image information;

an address generator generating write addresses and generating read addresses;

a memory writing circuit coupled to the data decompressed video image input circuit, coupled to the two dimensional pixel block memory, and coupled to the address generator, the memory writing circuit writing the information the two dimensional array of blocks of video pixel image information into the two dimensional pixel block image memory in response to the data decompressed video information generated by the data decompressed video image input circuit and in response to the write addresses generated by the address generator;

a pixel block memory reading circuit coupled to the two dimensional pixel block memory and coupled to the address generator, the pixel block memory reading circuit accessing blocks of video pixel image information in response to the two dimensional array of blocks of video pixel image information stored in the two dimensional pixel block memory and in response to the read addresses generated by the address generator;

a processor coupled to the pixel block memory reading circuit and generating data compressed video image information in response to the blocks of video pixel image information accessed by the pixel block memory reading circuit; and

an output circuit coupled to the processor and [with said] outputting [meams is a parallel sequence of words, where] the data compressed video image information at a second word rate [of the parallel words] that is greater than the first word rate [of the serial words].

12. [The] A buffer of memory system [as set forth in claim 9 above,] comprising:

a data decompressed video image input circuit generating data decompressed video image [where said receiving means include means for receiving the] information in response to a first clock signal;

a two dimensional pixel block memory storing a two dimensional array of blocks of video pixel image information, the two dimensional array of blocks of video pixel image information arranged in a two dimensional array of rows and columns of blocks of video pixel image information;

a memory writing circuit coupled to the data decompressed video image input circuit and coupled to the two dimensional pixel block memory, the memory writing circuit writing the two dimensional array of blocks of video pixel image information into the two dimensional pixel block image memory in response to the data decompressed video image information generated by the data decompressed video image input circuit;

a pixel block memory reading circuit coupled to the two dimensional pixel block memory, the pixel block memory reading circuit accessing blocks of video pixel image information in response to the two dimensional array of blocks of video pixel image Information stored in the two dimensional pixel block memory;

a vector generator generating two dimensional vector information;

a two dimensional vector processor coupled to the pixel block memory reading circuit and coupled to the vector generator, the two dimensional vector processor generating data compressed video image information in response to the blocks of video pixel image information accessed by the pixel block memory reading circuit and

in response to the two dimensional vector information generated by the vector generator; and

an output circuit coupled to the two dimensional vector processor and [where said] outputting [meams outputs] the data compressed video image [stored] information in response to a second clock signal,[;] wherein said first clock signal is asynchronous relative to said second clock signal.

13. [The] A buffer memory system [as set forth in claim 9 above,] comprising:

a data decompressed video image input circuit generating data decompressed video frequency domain image [where said receiving means includes means for receiving the] information in response to a first clock signal [having changing clock pulse periods];

a two dimensional frequency domain block memory storing a two dimensional array of blocks of video frequency domain image information, the two dimensional array of blocks of video frequency domain image information arranged in a two dimensional array of rows and columns of blocks of video frequency domain image information;

an address generator generating write addresses and generating read addresses;

a memory writing circuit coupled to the data decompressed video image input circuit, coupled to the two dimensional frequency domain block memory, and coupled to the address generator, the memory writing circuit writing the two dimensional array of blocks of video frequency domain image information into the two dimensional frequency domain block image memory in response to the input data decompressed video frequency

domain image information generated by the data decompressed video image input circuit and in response to the write addresses generated by the address generator;

a block memory reading circuit coupled to the two dimensional frequency domain block memory and coupled to the address generator, the block memory reading circuit accessing blocks of video frequency domain image information in response to the two dimensional array of blocks of video frequency domain image information stored in the two dimensional frequency domain block memory and in response to the read addresses generated by the address generator;

a two dimensional frequency domain transform processor coupled to the block memory reading circuit and generating data compressed video image information in response to the blocks of video frequency domain image information accessed by the block memory reading circuit; and

an output circuit coupled to the two dimensional frequency domain transform processor and [where said] outputting [meams outputs] the data compressed video image [stored] information generated by the two dimensional frequency domain transform processor in response to a second clock signal [having non-changing clock pulse periods].

14. [The] A buffer memory system [as set forth in claim 9 above,] comprising:

a data decompressed video image input circuit generating data decompressed video frequency domain image [where said receiving means includes means for receiving the] information;

a two dimensional frequency domain block memory coupled to the data decompressed video image input circuit and storing a two dimensional array of blocks of video frequency domain image [as a single line of] information in response to the data decompressed video frequency domain image information generated by the data decompressed video image input circuit, the two dimensional array of blocks of video frequency domain image information arranged in a two dimensional array of rows and columns of blocks of video frequency domain image information;

an address generator generating read addresses;

a block memory reading circuit coupled to the two dimensional frequency domain block memory and coupled to the address generator, the block memory reading circuit accessing blocks of video frequency domain image information in response to the two dimensional array of blocks of video frequency domain image information stored in the two dimensional frequency domain block memory and in response to the read addresses generated by the address generator;

a two dimensional frequency domain transform processor coupled to the block memory reading circuit and generating data compressed video image information in response to the blocks of video frequency domain image information in response to the blocks of video frequency domain image information accessed by the frequency domain block memory reading circuit; and

an output circuit coupled to the two dimensional frequency domain transform processor and [where said] outputting [meams includes means for outputting] the data compressed video image [stored] information generated by the two dimensional frequency domain trans-

form processor [as a plurality of lines of information in parallel].

17. A memory system [as set forth in claim 16, further] comprising:

an image input circuit generating input image information;

a two dimensional frame buffer storing a frame of [display] image information, the frame of image information arranged in a two dimensional array of rows and columns of blocks of pixel image information; [and]

an address generator generating write addresses and generating read addresses;

a frame buffer writing circuit coupled to the image input circuit, coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer writing circuit writing the frame of image information into the two dimensional frame buffer in response to the input image information generated by the image input circuit and in response to the write addresses generated by the address generator;

a first clock circuit generating a first clock signal having a first clock rate;

[an] a frame buffer accessing circuit coupled to the two dimensional frame buffer, coupled to the first clock circuit and coupled to the address generator, the frame buffer accessing circuit accessing [a line] blocks of [frame buffered display] pixel image information in response to the read addresses generated by the address generator, wherein the accessing blocks of pixel image information from the two dimensional frame buffer by the frame buffer accessing circuit is at a first

information rate in response to the first clock signal; [, wherein the input circuit is]

a vector generator generating two dimensional vector information;

a two dimensional block processor coupled to the frame buffer accessing circuit and coupled to the vector generator, the two dimensional block processor generating two dimensional processed image information [generates the sequence of input words into the first memory] in response to the [line] blocks of [frame buffered display] pixel image information accessed by the frame buffer accessing circuit and in response to the two dimensional vector information generated by the vector generator;

a two dimensional spatial processor coupled to the two dimensional block processor and generating two dimensional spatially processed image information in response to the two dimensional processed image information generated by the two dimensional block processor;

a second clock circuit generating a second clock signal having a second clock rate that is different than the first clock rate that is different than the first clock rate of the first clock signal; and

an output circuit coupled to the two dimensional spatial processor and coupled to the second clock circuit, the output circuit generating output image information in response to the two dimensional spatially processed image information generated by the two dimensional spatial processor, wherein the generation of the output image information by the output circuit is at a different

information rate than the first information rate in response to the second clock signal.

18. A memory system [as set forth in claim 16, further] comprising:

an image input circuit generating input image information;

[*a*] two dimensional frame buffer storing a frame of image information, the frame of image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

an address generator generating write addresses and generating read addresses;

a frame buffer writing circuit [kernel memory] coupled to the [first output] image input circuit, coupled to the two dimensional frame buffer and coupled to the [second output circuit] address generator and [storing a kernel] writing the frame of image information into the two dimensional frame buffer [output words] in response to the input image information [first sequence of output words] generated by the [first output] image input circuit and in response to the [second sequence of output words] write addresses generated by the [second output circuit] address generator; [and]

a frame buffer accessing circuit coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer accessing circuit accessing blocks of pixel image information in response to the read addresses generated by the address generator;

a vector generator generating two dimensional vector information;

a two dimensional block processor coupled to the frame buffer accessing circuit and coupled to the vector generator, the two dimensional block processor generating two dimensional processed image information in response to the blocks of pixel image information accessed by the frame buffer accessing circuit and in response to the two dimensional vector information generated by the vector generator;

a [kernel] two dimensional spatial processor coupled to the [kernel memory] two dimensional block processor and generating [a sequence of] two dimensional spatially processed image information [filtered output words] in response to the [kernel of display] two dimensional processed image information [stored] generated by the [kernel memory] two dimensional block processor; and

an output circuit coupled to the two dimensional spatial processor and generating output image information in response to the two dimensional spatially processed image information generated by the two dimensional spatial processor;

19. A memory system [as set forth in claim 18, further] comprising:

an image input circuit generating input image information;

[a] two dimensional frame buffer storing a frame of image information, the frame of image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

an address generator generating write addresses and generating read addresses;

a frame buffer writing circuit coupled to the image input circuit, coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer writing circuit writing the frame of image information into the two dimensional frame buffer in response to the input image information generated by the image input circuit and in response to the write addresses generated by the address generator;

a frame buffer accessing circuit coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer accessing circuit accessing blocks of pixel image information in response to the read addresses generated by the address generator;

a two dimensional spatial processor coupled to the frame buffer accessing circuit and generating two dimensional spatially processed image information in response to the blocks of pixel image information accessed by the frame buffer accessing circuit; and

an output circuit [display monitor] coupled to the [kernel] two dimensional spatial processor and generating [a spatially filtered display] output image information in response to the two dimensional spatially [filtered output words] processed image information generated by the two dimensional spatial processor.

20. A memory system [as set forth in claim 16, further] comprising:

an image input circuit generating input image information;

a two dimensional pixel block memory storing a two dimensional array of blocks of pixel image information, the two dimensional array of blocks of pixel image

information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

an address generator generating write addresses and generating read addresses;

a pixel block memory writing circuit coupled to the image input circuit, coupled to the two dimensional pixel block memory and coupled to the address generator, the pixel block memory writing circuit writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory in response to the input image information generated by the image input circuit and in response to the write addresses generated by the addresses generator;

a first clock circuit [coupled to the input circuit and] generating a first clock signal having a first clock rate;

a pixel block memory accessing circuit coupled to the two dimensional pixel block memory, coupled to the first clock circuit and coupled to the address generator, the pixel block memory accessing circuit accessing blocks of pixel image information in response to the read addresses generated by the address generator, wherein the [writing of the sequence of input words into the first memory] accessing of blocks of pixel image information from the two dimensional pixel block memory by the [input] pixel block memory accessing circuit is at a first [word] information rate in response to the first clock signal; [and]

a vector generator generating two dimensional vector information;

a two dimensional block processor coupled to the pixel block memory accessing circuit and coupled to the

vector generator, the two dimensional block processor generating two dimensional processed image information in response to the blocks of pixel image information accessed by the pixel block memory accessing circuit and in response to the two dimensional vector information generated by the vector generator;

a two dimensional spatial processor coupled to the two dimensional block processor and generating two dimensional spatially processed image information generated by the two dimensional block processor;

a second clock circuit [coupled to the output circuit and] generating a second clock signal having a second clock rate that is [higher] different than the first rate of the first clock signal; and

an output circuit coupled to the two dimensional spatial processor and coupled to the second clock circuit, the output circuit generating output image information in response to the two dimensional spatially processed image information generated by the two dimensional spatial processor, wherein the [outputting] generation of the [first sequence of] output image information [words from the second memory by the output circuit is at a higher word rate than the first word rate in response to the second clock signal and wherein the outputting of the second sequence of output words from the third memory] by the output circuit is at a [higher word] different information rate than the first [word] information rate in response to the second clock signal.

22. A memory system [as set forth in claim 21, further] comprising:

an image input circuit generating input image information;

a two dimensional frame buffer storing a frame of [display] image information, the frame of image information arranged in a two dimensional array of rows and columns of blocks of pixel image information; [and]

an address generator generating write addresses and generating read addresses;

a frame buffer writing circuit coupled to the image input circuit, coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer writing circuit writing the frame of image information into the two dimensional frame buffer in response to the input image information generated by the image input circuit and in response to the write addresses generated by the address generator;

[an] a frame buffer accessing circuit coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer accessing circuit accessing [a line] blocks of [frame buffered display] pixel image information in response to the read addresses generated by the address generator; [, wherein the input circuit is]

a two dimensional processor coupled to the frame buffer accessing circuit and generating two dimensional output processed image information [generates the sequence of input words] in response the [line] blocks of [frame buffered display] pixel image information accessed by the frame buffer accessing circuit; and

an output circuit coupled to the two dimensional processor and generating output image information in response to the two dimensional output processed image information generated by the two dimensional processor.

23. A memory system [as set forth in claim 21, further] comprising:

an image input circuit generating input image information;

a two dimensional pixel block memory storing a two dimensional array of blocks of pixel image information, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

an address generator generating write addresses and generating read addresses;

a pixel block [kernel] memory writing circuit coupled to the image input [output] circuit, coupled to the two dimensional pixel block memory and [storing a kernel] coupled [*to the*] address generator, the pixel block memory writing circuit writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory [output words] in response to the [plurality of sequences of output words] input image information generated by the image input circuit and in response to the write addresses generated by the address generator; [and]

a pixel block memory accessing circuit coupled to the two dimensional pixel block memory and coupled to the address generator, the pixel block memory accessing circuit accessing blocks of pixel image information generated by the address generator;

a [kernel] two dimensional processor coupled to the [kernel] pixel block memory accessing circuit and generating [a sequence of spatially filtered] two dimensional output processed image information [words] in response to the [kernel of output words stored] blocks of

pixel image information accessed by the [kernel] pixel block memory accessing circuit; and

an output circuit coupled to the two dimensional processor and generating output image information in response to the two dimensional output processed image information generated by the two dimensional processor.

24. A memory system [as set forth in claim 23, further] comprising:

an image input circuit generating input image information;

a two dimensional pixel block memory storing a two dimensional array of blocks of pixel image information, the two dimensional array of blocks of pixel of image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

an address generator generating write addresses and generating read addresses;

a pixel block memory writing circuit coupled to the image input circuit, coupled to the two dimensional pixel block memory and coupled to the address generator, the pixel block memory writing circuit writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory in response to the input image information generated by the image input circuit and in response to the write addresses generated by the address generator;

a first clock circuit generating a first clock signal having a first clock rate;

a pixel block memory accessing circuit coupled to the two dimensional pixel block memory, coupled to the

first clock circuit and coupled to the address generator, the pixel block memory accessing circuit accessing blocks of pixel image information in response to the read addresses generated by the address generator, wherein the accessing of blocks of pixel image information from the two dimensional pixel block memory by the pixel block memory accessing circuit is at a first information rate in response to the first clock signal;

a frequency domain processor coupled to the pixel block memory accessing circuit and generating frequency domain image information in response to the blocks of pixel image information accessed by the pixel block memory accessing circuit;

a weight memory storing weight information;

a weight memory accessing circuit coupled to the weight memory and generating accessed weight information by accessing the weight information stored by the weight memory;

a weighting processor coupled to the frequency domain processor and coupled to the weight memory accessing circuit, the weighting processor generating weighted frequency domain image information by weighting the frequency domain image information generated by the frequency domain processor in response to the accessed weight information generated by the weight memory accessing circuit;

a second clock circuit generating a second clock signal having a second clock rate that is different than the first clock rate of the first clock signal; and

[a display monitor] an output circuit coupled to the [kernel] weighting processor and coupled to the second clock circuit, the output circuit generating [a spa-

tially filtered display] output weighted frequency domain image information in response to the [spatially filtered] weighted frequency domain image information generated by the weighting processor, wherein the generation of the output [words] weighted frequency domain image information by the output circuit is at a different information rate than the first information rate in response to the second clock signal.

25. A memory system [as set forth in claim 21, further] comprising:

an image input circuit generating input image information;

a two dimensional pixel block memory storing a two dimensional array of blocks of pixel image information, the two dimensional array of blocks of pixel of image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

an address generator generating write addresses and generating read addresses;

a pixel block memory writing circuit coupled to the image input circuit, coupled to the two dimensional pixel block memory and coupled to the address generator, the pixel block memory writing circuit writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory in response to the input image information generated by the image input circuit and in response to the write addresses generated by the address generator;

a first clock circuit [coupled to the input circuit and] generating a first clock signal having a first clock rate;

a pixel block memory accessing circuit coupled to the two dimensional pixel block memory, coupled to the first clock circuit and coupled to the address generator, the pixel block memory accessing circuit accessing blocks of pixel image information in response to the read addresses generated by the address generator, wherein the [generating of the sequence of input words] accessing of blocks of pixel image information from the two dimensional pixel block memory by the pixel block memory accessing circuit is at a first [word] information rate in response to the first clock signal; [and]

a two dimensional spatial processor coupled to the pixel block memory accessing circuit and generating two dimensional spatially processed image information in response to the blocks of pixel image information accessed by the pixel block memory accessing circuit;

a second clock circuit [coupled to the output circuit and] generating a second clock signal having a second clock rate that is [higher] different than the first rate of the first clock signal; and

an output circuit coupled to the two dimensional spatial processor and coupled to the second clock circuit, the output circuit generating output image information in response to the two dimensional spatially processed image information generated by the two dimensional spatial processor, wherein the [outputting] generation of the [plurality of sequences] of output image information by the output circuit [words] is at a [higher word] different information rate than the first [word] information rate in response to the second clock signal.

34. A memory system [as set forth in claim 32, further] comprising:

an image input circuit generating input image information;

a two dimensional frame buffer storing a frame of [display] image information, the frame of image information arranged in a two dimensional array of rows and columns of blocks of pixel image information, wherein the blocks of pixel image information have boundaries there between; [and]

an address generator generating write addresses and generating read addresses;

a frame buffer writing circuit coupled to the image input circuit, coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer writing circuit writing the frame of image information into the two dimensional frame buffer in response to the input image information generated by the image input circuit and in response to the write addresses generated by the address generator;

a first clock circuit generating a first clock signal having a first clock rate;

[an] a frame buffer accessing circuit coupled to the two dimensional frame buffer, coupled to the first clock circuit and coupled to the address generator, the frame buffer accessing circuit accessing [a line] blocks of [frame buffered display] pixel image information in response to the read addresses generated by the address generator, wherein the accessing of blocks of pixel image information from the two dimensional frame buffer by the frame buffer accessing circuit is at a first information rate in response to the first clock signal; [, wherein the input circuit is]

a frequency domain processor coupled to the frame buffer accessing circuit and generating frequency domain image information [storing the sequence of input words into the input memory] in response to the [line] blocks of [frame buffered display] pixel image information accessed by the frame buffer accessing circuit;

a block boundary smoothing processor generating block boundary smoothing information to smooth the pixel image information at boundaries between blocks of pixel image information;

a weight memory storing weight information;

a weight memory accessing circuit coupled to the weight memory and generating accessed weight information by accessing the weight information stored by the weight memory;

a weighting processor coupled to the frequency domain processor, coupled to the block boundary smoothing processor and coupled to the weight memory accessing circuit, the weighting processor generating smoothed weighted frequency domain image information by weighting the frequency domain image information generated by the frequency domain processor in response to the accessed weight information generated by the weight memory accessing circuit and in response to the block boundary smoothing information generated by the block boundary smoothing processor;

a second clock circuit generating a second clock signal having a second clock rate that is different than the first clock rate of the first clock signal; and

an output circuit coupled to the weighting processor and coupled to the second clock circuit, the output circuit generating output smoothed weighted frequency

domain image information in response to the smoothed weighted frequency domain image information generated by the weighted processor, wherein the generation of the output smoothed weighted frequency domain image information by the output circuit is at a different information rate than the first information rate in response to the second clock signal.

35. A memory system [as set forth in claim 32, further] comprising:

an image input circuit generating input image information;

a two dimensional block memory storing a two dimensional array of blocks of image information, the two dimensional array of blocks of image information arranged in a two dimensional array of rows and columns of blocks of image information;

an address generator generating write addresses and generating read addresses;

a [kernel] block memory writing circuit coupled to the [output] image input circuit, coupled to the two dimensional block memory and [storing a kernel] coupled to the address generator, the block memory writing circuit writing the two dimensional array of blocks of image information into the two dimensional block memory [output words] in response to the input image information generated by the image input circuit [first sequence of output words] and in response to the [second sequence of output words] write addresses generated by the address generator; ~~and~~

a block memory accessing circuit coupled to the two dimensional block memory and coupled to the address generator, the block memory accessing circuit

accessing blocks of image information in response to the read addresses generated by the address generator;

a weight memory storing weight information;

a weight memory accessing circuit coupled to the weight memory and generating accessed weight information by accessing the weight information stored by the weight memory;

a [kernel] weighting processor coupled to the [kernel memory] block memory accessing circuit and coupled to the weight memory accessing circuit, the weighting processor generating weighted image information by weighting the image information contained in the blocks of image information accessed by the block memory accessing circuit [a sequence of spatially filtered output words] in response to the [kernel of display] accessed weight information generated [stored] by the [kernel memory.] weight memory accessing circuit; and

an output circuit coupled to the weighting processor and generating output weighted image information in response to the weighted image information generated by the weighting processor.

36. A memory system [as set forth in claim 35, further] comprising:

an image input circuit generating input image information;

a two dimensional pixel block memory storing a two dimensional array of blocks of pixel image information, the two dimensional array of blocks of pixel of image information arranged in a two dimensional array of rows and columns of blocks of pixel image information,

wherein the blocks of pixel image information have boundaries there between;

an address generator generating write addresses and generating read addresses;

a pixel block memory writing circuit coupled to the image input circuit, coupled to the two dimensional pixel block memory and coupled to the address generator, the pixel block memory writing circuit writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory in response to the input image information generated by the image input circuit and in response to the write addresses generated by the address generator;

a first clock circuit generating a first clock signal having a first clock rate;

a pixel block memory accessing circuit coupled to the two dimensional pixel block memory, coupled to the first clock circuit and coupled to the address generator, the pixel block memory accessing circuit accessing blocks of pixel image information in response to the read addresses generated by the address generator, wherein the accessing of blocks of pixel image information from the two dimensional pixel block memory by the pixel block memory accessing circuit is at a first information rate in response to the first clock signal;

a frequency domain processor coupled to the pixel block memory accessing circuit and generating frequency domain image information in response to the blocks of pixel image information accessed by the pixel block memory accessing circuit;

a block boundary smoothing processor generating block boundary smoothing information to smooth the

pixel image information at boundaries between blocks of pixel image information;

a weight memory storing weight information;

a weight memory accessing circuit coupled to the weight memory and generating accessed weight information by accessing the weight information stored by the weight memory;

a weighting processor coupled to the frequency domain processor, coupled to the block boundary smoothing processor and coupled to the weight memory accessing circuit, the weighting processor generating smoothed weighted frequency domain image information by weighting the frequency domain image information generated by the frequency domain processor in response to the accessed weight information generated by the weight memory accessing circuit and in response to the block boundary smoothing information generated by the block boundary smoothing processor;

a second clock circuit generating a second clock signal having a second clock rate that is different than the first clock rate of the first clock signal; and

[a display monitor] an output circuit coupled to the [kernel] weighting processor and coupled to the second clock circuit, the output circuit generating [a spatially filtered display] output smoothed weighted frequency domain image information in response to the [spatially filtered] smoothed weighted frequency domain image information generated by the weighting processor, wherein the generation of the output [words] smoothed weighted frequency domain image information by the output circuit is at a different information rate

than the first information rate in response to the second clock signal.

37. A memory system [as set forth in claim 32, further] comprising:

an image input circuit generating input image information;

a two dimensional block memory storing a two dimensional array of blocks of image information, the two dimensional array of blocks of image information arranged in a two dimensional array of rows and columns of blocks of image information;

an address generator generating write addresses and generating read addresses;

a block memory writing circuit coupled to the image input circuit, coupled to the two dimensional block memory and coupled to the address generator, the block memory writing circuit writing the two dimensional array of blocks of image information into the two dimensional block memory in response to the input image information generated by the image input circuit and in response to the write addresses generated by the address generator;

a first clock circuit [coupled to the input circuit and] generating a first clock signal having a first clock rate;

a block memory accessing circuit coupled to the two dimensional block memory, coupled to the first clock circuit and coupled to the address generator, the block memory accessing circuit accessing blocks of image information in response to the read addresses generated by the address generator, wherein the [storing of the

sequence of input words into] accessing of blocks of image information from the [input] two dimensional block memory by the [input] block memory accessing circuit is at a first [word] information rate in response to the first clock signal; [and]

a weight memory storing weight information;

a weight memory accessing circuit coupled to the weight memory and generating accessed weight information by accessing the weight information stored by the weight memory;

a weighting processor coupled to the block memory accessing circuit and coupled to the weight memory accessing circuit, the weighting processor generating weighted image information by weighting the image information contained in the blocks accessed by the block memory accessing circuit in response to the accessed weight information generated by the weight memory accessing circuit;

a second clock circuit [coupled to the output circuit and] generating a second clock signal having a second clock rate that is [higher] different than the first clock rate of the first clock signal; and

an output circuit coupled to the weighting processor and coupled to the second clock circuit, the output circuit generating output weighted image information in response to the weighted image information generated by the weighting processor, wherein the [outputting of the first sequence of output words from the first output memory by the output circuit is at a higher word rate than the first word rate in response to the second clock signal and wherein the outputting] generation of the [second sequence of output words from the second] out-

put weighted image information [memory] by the output circuit is at a [higher word] different information rate than the first [word] information rate in response to the second clock signal.

42. A memory system [as set forth in claim 41, further] comprising:

an image input circuit generating input image information;

a two dimensional frame buffer storing a frame of [display] image information, the frame of image information arranged in a two dimensional array of rows and columns of blocks of pixel image information, wherein the blocks of pixel image information have boundaries therebetween; [and]

an address generator generating write addresses and generating read addresses;

a frame buffer writing circuit coupled to the image input circuit, coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer writing circuit writing the frame of image information into the two dimensional frame buffer in response to the input image information generated by the image input circuit and in response to the write addresses generated by the address generator;

[an] a frame buffer accessing circuit coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer accessing circuit accessing [a line] blocks of [frame buffered display] pixel image information in response to the read addresses generated by the address generator; [wherein the input circuit is]

a frequency domain processor coupled to the frame buffer accessing circuit and [generates the input line of display] generating frequency domain image information in response to the [line] blocks of [frame buffered display] pixel image information accessed by the frame buffer accessing circuit;

a block boundary smoothing processor generating block boundary smoothing information to smooth the pixel image information at boundaries between blocks of pixel image information;

a weight memory storing weight information;

a weight memory accessing circuit coupled to the weight memory and generating accessed weight information by accessing the weight information stored by the weight memory;

a weighting processor coupled to the frequency domain processor, coupled to the block boundary smoothing processor and coupled to the weight memory accessing circuit, the weighting processor generating smoothed weighted frequency domain image information by weighting the frequency domain image information generated by the frequency domain processor in response to the accessed weight information generated by the weight memory accessing circuit and in response to the block boundary smoothing information generated by the block boundary smoothing processor; and

an output circuit coupled to the weighting processor and generating output smoothed weighted frequency domain image information in response to the smoothed weighted frequency domain image information generated by the weighting processor.

43. A memory system [as set forth in claim 41, further] comprising:

an image input circuit generating input image information;

a two dimensional frame buffer storing a frame of image information, the frame of image information arranged in a two dimensional array of rows and columns of blocks of image information, wherein the blocks of image information have boundaries therebetween;

an address generator generating write addresses and generating read addresses;

a [kernel memory] frame buffer writing circuit coupled to the [output] image input circuit, coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer writing circuit writing the frame [storing a kernel[of [display] image information into the two dimensional frame buffer in response to the [three lines of display] input image information generated by the [output] image input circuit and in response to the write addresses generated by the address generator; [and]

a frame buffer accessing circuit coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer accessing circuit accessing blocks of image information in response to the read addresses generated by the address generator;

a block boundary smoothing processor generating block boundary smoothing information to smooth the image information at boundaries between blocks of image information;

a weight memory storing weight information;

a weight memory accessing circuit coupled to the weight memory and generating accessed weight information by accessing the weight information stored by the weight memory;

a [kernel] weighting processor coupled to the frame buffer accessing circuit, coupled to the block boundary smoothing processor and coupled to the [kernel] weight memory accessing circuit, [and] the weighting processor generating [a line of spatially filtered display] smoothed weighted image information by weighting the image information contained in the blocks of image information accessed by the frame buffer accessing circuit in response to the [kernel of display] accessed weight information [stored] generated by the [kernel] weight memory accessing circuit and in response to the block boundary smoothing information generated by the block boundary smoothing processor; and

an output circuit coupled to the weighting processor and generating output smoothed weighted image information in response to the smoothed weighted image information generated by the weighting processor.

44. A memory system [as set forth in claim 43, further] comprising:

an image input circuit generating input image information;

a two dimensional block memory storing a two dimensional array of blocks of image information, the two dimensional array of blocks of image information arranged in a two dimensional array of rows and columns of blocks of image information, wherein the blocks of image information have boundaries therebetween;

an address generator generating write addresses and generating read addresses;

a block memory writing circuit coupled to the image input circuit, coupled to the two dimensional block memory and coupled to the address generator, the block memory writing circuit writing the two dimensional array of blocks of image information into the two dimensional block memory in response to the input image information generated by the image input circuit and in response to the write addresses generated by the address generator;

a block memory accessing circuit coupled to the two dimensional block memory and coupled to the address generator, the block memory accessing circuit accessing blocks of image information in response to the read addresses generated by the address generator;

a block boundary smoothing processor generating block boundary smoothing information to smooth the image information at boundaries between blocks of image information;

a weight memory storing weight information;

a weight memory accessing circuit coupled to the weight memory and generating accessed weight information by accessing the weight information stored by the weight memory;

a weighting processor coupled to the frame buffer accessing circuit, coupled to the block boundary smoothing processor and coupled to the weight memory accessing circuit, the weighting processor generating smoothed weighted image information by weighting the image information contained in the blocks of image information accessed by the frame buffer accessing circuit

in response to the accessed weight information generated by the weight memory accessing circuit and in response to the block boundary smoothing information generated by the block boundary smoothing processor; and

an [display monitor] output circuit coupled to the [kernel] weighting processor and generating [a spatially filtered display] output smoothed weighted image information in response to the [line of spatially filtered display] smoothed weighted image information generated by the weighting processor.

45. A memory system [as set forth in claim 41, further] comprising:

an image input circuit generating input image information;

a two dimensional block memory storing a two dimensional array of blocks of image information, the two dimensional array of blocks of image information arranged in a two dimensional array of rows and columns of blocks of image information;

an address generator generating write addresses and generating read addresses;

a block memory writing circuit coupled to the image input circuit, coupled to the two dimensional block memory and coupled to the address generator, the block memory writing circuit writing the two dimensional array of blocks of image information into the two dimensional block memory in response to the input image information generated by the image input circuit and in response to the write addresses generated by the address generator;

a first clock circuit [coupled to the input circuit and] generating a first clock signal having a first clock rate;

a block memory accessing circuit coupled to the two dimensional block memory, coupled to the first clock circuit and coupled to the address generator, the block memory accessing circuit accessing blocks of image information in response to the read addresses generated by the address generator, wherein the [generating] accessing of blocks of image information from the two dimensional block memory [the input line of display information] by the [input] block memory accessing circuit is at a first information rate in response to the first clock signal; [and]

a block boundary smoothing processor generating block boundary smoothing information to smooth the image information at boundaries between blocks of image information;

a weight memory storing weight information;

a weight memory accessing circuit coupled to the weight memory and generating accessed weight information by accessing the weight information stored by the weight memory;

a weighting processor coupled to the block memory accessing circuit, coupled to the block boundary smoothing processor and coupled to the weight memory accessing circuit, the weighting processor generating smoothed weighted image information by weighting the image information contained in the blocks accessed by the block memory accessing circuit in response to the accessed weight information generated by the weight memory accessing circuit and in response to the block

boundary smoothing information generated by the block boundary smoothing processor;

a second clock circuit [coupled to the output circuit and] generating a second clock signal having a second clock rate that is [higher] different than the first clock rate of the first clock signal; and

an output circuit coupled to the weighting processor and coupled to the second clock circuit, the output circuit generating output smoothed weighted image information in response to the smoothed weighted image information generated by the weighting processor, wherein the generating of the [three lines of display] output smoothed weighted image information by the output circuit is at a [higher] different information rate than the first information rate in response to the second clock signal.

49. A memory system [as set forth in claim 47, further] comprising:

an image input circuit generating input image information;

a two dimensional frame buffer storing a frame of [display] image information, the frame of image information arranged in a two dimensional array of rows and columns of blocks of pixel image information; [and]

an address generator generating write addresses and generating read addresses;

a frame buffer writing circuit coupled to the image input circuit, coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer writing circuit writing the frame of image information into the two dimensional frame buffer in re-

sponse to the input image information generated by the image input circuit and in response to the write addresses generated by the address generator;

a first clock circuit generating a first clock signal having a first clock rate;

[an] a frame buffer accessing circuit coupled to the two dimensional frame buffer, coupled to the first clock circuit and coupled to the address generator, the frame buffer accessing circuit accessing [a line] blocks of [frame buffered display] pixel image information in response to the read addresses generated by the address generator, wherein the accessing of blocks of pixel image information from the two dimensional frame buffer by the frame buffer accessing circuit is at a first information rate in response to the first clock signal; [, wherein the input circuit is]

a frequent domain processor coupled to the frame buffer accessing circuit and [generates the input line of display] generating frequency domain image information in response to the [line] blocks of [frame buffered display] pixel image information accessed by the frame buffer accessing circuit;

a weight memory storing weight information;

a weight memory accessing circuit coupled to the weight memory and generating accessed weight information by accessing the weight information stored by the weight memory;

a weight processor coupled to the frequency domain processor and coupled to the weight memory accessing circuit, the weighting processor generating weighted frequency domain image information by weighting the frequency domain image information generated by the

frequency domain processor in response to the accessed weight information generated by the weight memory accessing circuit;

a second clock circuit generating a second clock signal having a second clock rate that is different than the first clock rate of the first clock signal; and

an output circuit coupled to the weighting processor and coupled to the second clock circuit, the output circuit generating output weighted frequency domain image information in response to the weighted frequency domain image information generated by the weighting processor, wherein the generation of the output weighted frequency domain image information by the output circuit is at a different information rate than the first information rate in response to the second clock signal.

50. A memory system [as set forth in claim 47, further] comprising:

an image input circuit generating input image information;

a two dimensional frame buffer storing a frame of image information, the frame of image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

an address generator generating write addresses and generating read addresses;

a frame buffer writing circuit [kernel memory] coupled to the image input [output] circuit, coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer writing circuit writing the frame [storing a kernel] of [display] image infor-

mation into the two dimensional frame buffer in response to the input image [three lines of display] information [simultaneously] generated by the [output] image input circuit and in response to the write addresses generated by the address generator; [and]

a frame buffer accessing circuit coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer accessing circuit accessing blocks of pixel image information in response to the read addresses generated by the address generator;

a [kernel] frequency domain processor coupled to the [kernel memory] frame buffer accessing circuit and generating [a line of spatially filtered display] frequency domain image information in response to the [kernel] blocks of pixel image [display] information accessed [stored] by the [kernel memory.] frame buffer accessing circuit;

a weight memory storing weight information;

a weight memory accessing circuit coupled to the weight memory and generating accessed weight information by accessing the weight information stored by the weight memory;

a weighting processor coupled to the frequency domain processor and coupled to the weight memory accessing circuit, the weighting processor generating weighted frequency domain image information by weighting the frequency domain image information generated by the frequency domain processor in response to the accessed weight information generated by the weight memory accessing circuit; [*and*]

an output circuit coupled to the weighting processor and generating output weighted frequency domain

image information in response to the weighted frequency domain image information generated by the weighting processor.

51. A memory system [as set forth in claim 47, further] comprising:

an image input circuit generating input image information;

a two dimensional frame buffer storing a frame of image information, the frame of image information arranged in a two dimensional array of rows and columns of blocks of image information;

an address generator generating write addresses and generating read addresses;

a frame buffer writing circuit coupled to the image input circuit, coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer writing circuit writing the frame of image information into the two dimensional frame buffer in response to the input image information generated by the image input circuit and in response to the write addresses generated by the address generator;

a frame buffer accessing circuit coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer accessing circuit accessing blocks of image information in response to the read addresses generated by the address generator;

a weight memory storing weight coefficient information;

a weight memory accessing circuit coupled to the weight memory and generating accessed weight coeffi-

cient information by accessing the weight coefficient information stored by the weight memory;

a weighting processor coupled to the frame buffer accessing circuit and coupled to the weight memory accessing circuit, the weighting processor generating weighted image information by weighting the image information contained in the blocks of image information accessed by the frame buffer accessing circuit in response to the accessed weight coefficient information generated by the weight memory accessing circuit; [and]

an [display monitor] output circuit coupled to the [kernel] weighting processor and generating [a spatially filtered display] output weighted image information in response to the [spatially filtered display] weighted image information generated by the weighting processor.

52. A memory system [as set forth in claim 16, further] comprising:

an image input circuit generating input image information;

a two dimensional pixel block memory storing a two dimensional array of blocks of pixel image information, the two dimensional array of blocks of pixel of image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

an address generator generating write addresses and generating read addresses;

a pixel block memory writing circuit coupled to the image input circuit, coupled to the two dimensional pixel block memory and coupled to the address generator, the pixel block memory writing circuit writing the two dimensional array of blocks of pixel image informa-

tion into the two dimensional pixel block memory in response to the input image information generated by the image input circuit and in response to the write addresses generated by the address generator;

a first clock circuit [coupled to the input circuit and] generating a first clock signal having a first clock rate;

a pixel block memory accessing circuit coupled to the two dimensional pixel block memory, coupled to the first clock circuit and coupled to the address generator, the pixel block memory accessing circuit accessing blocks of pixel image information in response to the read addresses generated by the address generator, wherein the [generating of the input line of display] accessing of blocks of pixel image information from the two dimensional pixel block memory by the [input] pixel block memory accessing circuit is at a first information fate in response to the first clock signal; [and]

a two dimensional processor coupled to the pixel block memory accessing circuit and generating two dimensional processed image information in response to the blocks of pixel image information accessed by the pixel block memory accessing circuit;

a second clock circuit [coupled to the output circuit and] generating a second clock signal having a second clock rate that is [higher] different than the first rate of the first clock signal; and

an output circuit coupled to the two dimensional processor and coupled to the second clock circuit, the output circuit generating output image information in response to the two dimensional processed image information generated by the two dimensional processor,

wherein the generating of the [three lines of display] output image information by the output circuit is at a [higher] different information rate than the first information rate in response to the second clock signal.

81. [In a memory system, a] A process of operating a memory system comprising the acts of;

generating [an] input [line of display] image information;

storing [three lines] a frame of [display] image information by a two dimensional frame buffer, the frame of image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

generating write addresses and generating read addresses;

writing the frame of image information into the two dimensional frame buffer in response to the input image [lines of display] information and in response to the write addresses; [and]

generating a first clock signal having a first clock rate;

accessing blocks of pixel image information from the two dimensional frame buffer in response to the read addresses, wherein the accessing of blocks of pixel image information from the two dimensional frame buffer is at a first information rate in response to the first clock signal;

[simultaneously] generating two dimensional processed image [three lines of display] information in response to the [three lines] accessed blocks of [double

buffered display] pixel image information and in response to the two dimensional vector information;

generating two dimensional spatially processed image information in response to the two dimensional processed image information;

generating a second clock signal having a second clock rate that is different than the first clock rate of the first clock signal; and

generating output image information in response to the two dimensional spatially ~~by~~ processed image information, wherein the generation of the output image information is at a different information rate than the first information rate in response to the second clock signal.

82. [In a memory system, a] A process of operating a memory system comprising the acts of:

generating [an] input [line of display] image information;

storing [three lines of double buffered display] a two dimensional array of blocks of pixel image information by a two dimensional pixel block memory, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

generating write addresses and generating read addresses;

writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory in response to the input image [line of display] information and in response to the wrote addresses; [and]

generating a first clock signal having a first clock rate;

accessing blocks of pixel image information from the two dimensional frame buffer in response to the read addresses; wherein the accessing of blocks of pixel image information from the two dimensional frame buffer is at a first information rate in response to the first clock signal;

[simultaneously] generating two dimensional processed image [three lines of display] information in response to the [three lines] accessed blocks of [double buffered display] pixel image information;

generating a second clock signal having a second clock rate that is different than the first clock rate of the first clock signal; and

generating output image information in response to the two dimensional processed image information, wherein the generation of the output image information ~~by~~ is at a different information rate than the first information rate in response to the second clock signal.

83. [In a memory system, a] A process of operating a memory system comprising the acts of:

generating [an] input [line of display] image information;

storing [three lines] a frame of [double buffered display] image information by a two dimensional frame buffer, the frame of image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

generating write addresses and generating read addresses;

writing the frame of image information into the two dimensional frame buffer in response to the input image [line of display] information and in response to the write addresses; [and]

accessing blocks of pixel image information from the two dimensional frame buffer in response to the read addresses;

[simultaneously] generating two dimensional processed image [three lines of display] information in response to the [three lines] accessed blocks of [double buffered display] pixel image information; [*and*]

generating output image information in response to the two dimensional processed image information.

84. [In a memory system, a] A process of operating a memory system comprising the acts of:

generating [an] input [line of display] image information;

storing a [first line] two dimensional array of blocks of [display] pixel image information by a two dimensional pixel block memory, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

generating write addresses and generating read addresses;

writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory in response to the input image [line of display] information and in response to the write addresses; [and]

accessing [the first line] blocks of [display] pixel image information from the two dimensional pixel block memory in response to the read addresses;

generating two dimensional processed image [storing a second line of display] information in response to the accessed blocks [*of*] [first line of display] pixel image information; and

generating output image information [accessing the second line of display] in response to the two dimensional processed image information.

85. [In a memory system, a] A process of operating a memory system comprising the acts of:

generating [an] input [line of display] image information;

storing a [first line] two dimensional array of blocks of [display] pixel image information by a two dimensional pixel block image memory, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

generating write addresses and generating read addresses;

writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block image memory in response to the input [line of display] image information and in response to the write addresses;

accessing [the first line] blocks of [display] pixel image information from the two dimensional pixel block image memory in response to the read addresses;

generating two dimensional vector image information;

generating two dimensional vector processed image information in response to the accessed blocks of pixel image information and in response to the two dimensional vector information;

storing [a second line] buffered blocks of [display] pixel image information by a buffer memory in response to the accessed [first line] blocks of [display] pixel image information;

[accessing the second line of display information;]

storing [a third line of display] buffered two dimensional vector processed image information in response to the [accessed second line of display] two dimensional vector processed image information; and

generating two dimensional spatially processed image [accessing the third line of display] information in response to the buffered blocks of pixel image information stored in the buffer memory and in response to the buffered two dimensional vector processed image information stored in said buffer memory.

95. A process of operating a memory system comprising the acts of:

generating input image information;

storing a two dimensional array of blocks of pixel image information in a two dimensional pixel block image memory in response to the input image information, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

generating read addresses;

accessing blocks of pixel image information from the two dimensional pixel block image memory in response to the read addresses;

generating output image information in response to the accessed blocks of pixel image information; [*and*]

storing buffered output image information by a buffer memory in response to the output image information.

96. A process of operating a memory system comprising the acts of:

generating input image information;

storing a two dimensional array of blocks of pixel image information in a two dimensional pixel block image memory in response to the input image information, the two dimensional array of blocks of pixel image infuriation arranged in a two dimensional array of rows and columns of blocks of pixel image information;

generating read addresses;

accessing blocks of pixel image information from the two dimensional pixel block image memory in response to the read addresses;

generating two dimensional spatially processed image information in response to the accessed blocks of pixel image information; and

storing buffered two dimensional spatially processed image information in a buffer memory in response to the two dimensional spatially processed image information.

97. A process of operating a memory system comprising the acts of:

generating input image information;

storing a two dimensional array of blocks of pixel image information in a two dimensional pixel block image memory in response to the input image information, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

accessing blocks of pixel image information from the two dimensional pixel block image memory;

generating two dimensional spatially processed image information in response to the accessed block.s of pixel image information; and

storing buffered two dimensional spatially processed image information in a buffer memory in response to the two dimensional spatially processed image information.

98. A process of operating a memory system comprising the acts of:

generating input image information at a first information rate;

storing a two dimensional array of blocks of pixel image information by a two dimensional pixel block memory, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

generating write addresses and generating read addresses;

writing the two dimensional array of blocks of pixel image information into the two dimensional pixel

block image memory in response to the input image information and in response to the write addressees;

accessing blocks of pixel image information response to the read addresses;

generating two dimensional vector information;

generating two dimensional vector processed image information in response to the accessed blocks of pixel image information and in response to the two dimensional vector information;

generating two dimensional spatially processed image information in response to the two dimensional vector processed image information;

generating output image information in response to the two dimensional spatially processed image information; and

outputting the output image information at a second information rate that is greater than the first information rate.

99. A process of operating a memory system comprising the acts of:

generating input image information at a first information rate;

storing a two dimensional array of blocks of pixel image information in a two dimensional pixel block memory in response to the input image information, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

generating read addresses;

accessing blocks of pixel image information in response to the read addresses;

generating output processed image information in response to the accessed blocks of pixel image information;

generating output image information in response to the input processed image information; and

outputting the output image information at a second information rate that is greater than the first information rate.

100. A process of operating a memory system comprising the acts of:

generating input image information at a fast information rate;

storing a two dimensional array of blocks of pixel image information in a two dimensional pixel block memory in response to the input image information, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

generating read addresses;

accessing blocks of pixel image information in response to the read addresses;

generating two dimensional spatially processed image information in response to the accessed blocks of pixel image information;

generating output image information in response to the two dimensional spatially processed image information; and

outputting the output image information at a second information rate that is greater than the first information rate.

101. A process of operating a memory system comprising the acts of:

generating input image information at a first information rate;

storing a two dimensional array of blocks of pixel image information in a two dimensional pixel block memory in response to the input image information, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

accessing blocks of pixel image information;

generating two dimensional spatially processed image information in response to the accessed blocks of pixel image information;

generating output image information in response to the two dimensional spatially processed image information; and

outputting the output image information at a second information rate that is greater than the first information rate.

102. A process of operating a memory system comprising the acts of:

generating input image information;

storing a frame of image information by a two dimensional frame buffer, the frame of image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

generating write addresses and generating read addresses;

writing the frame of image information into the two dimensional frame buffer in response to the input image information and in response to the write addresses;

generating a first clock signal having a first clock rate;

accessing blocks of pixel image information from the two dimensional frame buffer in response to the read addresses, wherein the accessing of blocks of pixel image information from the two dimensional frame buffer is at a first information rate in response to the first clock signal;

generating frequency domain image information in response to the accessed blocks of pixel image information;

storing weight information by a weight memory;

generating accessed weight information by accessing the weight information stored by the weight memory;

generating weighted frequency domain image information by weighting the frequency domain image information in response to the accessed weight information;

generating a second clock signal having a second clock rate that is different than the first clock rate of the first clock signal; and

generating output weighted frequency domain image information in response to the weighted frequency domain image information, wherein the genera-

tion of the output weighted frequency domain image information is at a different information rate than the first information rate in response to the second clock signal.

103. A process of operating a memory system comprising the acts of:

generating input image information;

storing a two dimensional array of blocks of pixel image information by a two dimensional pixel block memory, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

generating write addresses and generating read addresses;

writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory in response to the input image information and in response to the write addresses;

generating a first clock signal having a first clock rate;

accessing blocks of pixel image information from the two dimensional pixel block memory in response to the read addresses, wherein the accessing of blocks of pixel image information from the two dimensional pixel block memory is at a first information rate in response to the first clock signal;

storing weight information by a weight memory;

generating accessed weight information by accessing the weight information stored by the weight memory;

generating weighted image information by weighting the pixel image information contained in the accessed blocks of pixel image information in response to the accessed weight information;

generating a second clock signal having a second clock rate that is different than the first clock rate of the first clock signal; and

generating output weighted image information in response to the weighted image information, wherein the generation of the output weighted image information is at a different information rate than the first information rate in response to the second clock signal.

104. A process of operating a memory system comprising the acts of:

generating input image information;

storing a frame of image information by a two dimensional frame buffer, the frame of image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

generating write addresses and generating read addresses;

writing the frame of image information into the two dimensional frame buffer in response to the input image information and in response to the write addresses;

accessing blocks of pixel image information from the two dimensional frame buffer in response to the read addresses;

storing weight information by a weight memory;

generating accessed weight information by accessing the weight information stored by the weight memory;

generating weighted image information by weighting the pixel image information contained in the accessed blocks of pixel image information in response to the accessed weight information; and

generating output weighted image information in response to the weighted image information.

105. A process of operating a memory system comprising the acts of:

generating input image information;

storing a two dimensional array of blocks of pixel image information by a two dimensional pixel block memory, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

generating write addresses and generating read addresses;

writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory in response to the input image information and in response to the write addresses;

accessing blocks of pixel image information from the two dimensional pixel block memory in response to the read addresses;

storing weight information by a weight memory;

generating accessed weight information by accessing the weight information stored by the weight memory;

generating weighted image information by weighting the pixel image information contained in the accessed blocks of pixel image information in response to the accessed weight information; and

generating output weighted image information in response to the weighted image information.

106. A process of operating a memory system comprising the acts of:

generating input image information;

storing a frame of image information by a two dimensional frame buffer, the frame of image information arranged in a two dimensional array of rows and columns of blocks of pixel image information, wherein the blocks of pixel image information have boundaries therebetween;

generating write addresses and generating read addresses;

writing the frame of image information into the two dimensional frame buffer in response to the input image information and in response to the write addresses;

generating a first clock signal having a first clock rate;

accessing blocks of pixel image information in response to the read addresses, wherein the accessing of blocks of pixel image information from the two dimensional frame buffer is at a first information rate in response to the first clock signal;

generating frequency domain image information in response to the accessed blocks of pixel image information;

generating block boundary smoothing information to smooth the pixel image information at boundaries between blocks of pixel image information;

storing weight information by a weight memory;

generating accessed weight information by accessing the weight information stored by the weight memory;

generating smoothed weighted frequency domain image information by weighting the frequency domain image information in response to the accessed weight information and in response to the block boundary smoothing information;

generating a second clock signal having a second clock rate that is different than the first clock rate of the first clock signal; and

generating output smoothed weighted frequency domain image information in response to the smoothed weighted frequency domain image information, wherein the generation of the output smoothed weighted frequency domain image information is at a different information rate than the first information rate in response to the second clock signal.

107. A process of operating a memory system comprising the acts of:

generating input image information;

storing a two dimensional array of blocks of pixel image information by a two dimensional pixel block memory, the two dimensional array of blocks of pixel

image information arranged in a two dimensional array of rows and columns of blocks of pixel image information, wherein the blocks of pixel image information have boundaries therebetween;

generating write addresses and generating read addresses;

writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory in response to the input image information and in response to the write addresses;

generating a first clock signal having a first clock rate;

accessing blocks of pixel image information in response to the read addresses, wherein the accessing of blocks of pixel image information from the two dimensional pixel block memory is at a first information rate in response to the first clock signal;

generating block boundary smoothing information to smooth the pixel image information at boundaries between blocks of pixel image information;

storing weight information by a weight memory;

generating accessed weight information by accessing the weight information stored by the weight memory;

generating smoothed weighted image information by weighting the pixel image information contained in the accessed blocks of pixel image information in response to the accessed weight information and in response to the block boundary smoothing information;

generating a second clock signal having a second clock rate that is different than the first clock rate of the first clock signal; and

generating output smoothed weighted image information in response to the smoothed weighted image information, wherein the generation of the output smoothed weighted image information is at a different information rate than the first information rate in response to the second clock signal.

108. A process of operating a memory system comprising the acts of:

generating input image information;

storing a frame of image information by a two dimensional frame buffer, the frame of image information arranged in a two dimensional array of rows and columns of blocks of pixel image information, wherein the blocks of pixel image information have boundaries therebetween;

generating write addresses and generating read addresses;

writing the frame of image information into the two dimensional frame buffer in response to the input image information and in response to the write addresses;

accessing blocks of pixel image information in response to the read addresses;

generating block boundary smoothing information to smooth the pixel image information at boundaries between blocks of pixel image information;

storing weight coefficient information by a weight memory;

generating accessed weight coefficient information by accessing the weight coefficient information stored by the weight memory;

generating smoothed weighted image information by weighting the pixel image information contained in the accessed blocks of pixel image information in response to the accessed weight information and in response to the block boundary smoothing information; and

generating output smoothed weighted image information in response to the smoothed weighted image information.

109. A process of operating a memory system comprising the acts of:

generating input image information;

storing a two dimensional array of blocks of pixel image information by a two dimensional pixel block memory, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information, wherein the blocks of pixel image information have boundaries therebetween;

generating write addresses and generating read addresses;

writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory in response to the input image information and in response to the write addresses;

accessing blocks of pixel image information in response to the read addresses;

generating block boundary smoothing information to smooth the pixel image information at boundaries between blocks of pixel image information;

storing weight information by a weight memory;

generating accessed weight information by accessing the weight information stored by the weight memory;

generating smoothed weighted image information by weighting the pixel image information contained in the accessed blocks of pixel image information in response to the accessed weight information and in response to the block boundary smoothing information; and

generating output smoothed weighted image information in response to the smoothed weighted image information.

110. A memory system as set forth in claim 1,

wherein the two dimensional pixel block image memory is a static random access memory storing the array of blocks of pixel image information as a frame of 512 rows and 512 pixels per row of pixel image information;

wherein the image input circuit is a graphic stored program computer image input circuit generating the input image information as graphic input image information; and

wherein the accessing circuit is a two dimensional eight pixel by eight pixel accessing circuit simultaneously accessing the 64 pixels arranged as eight rows and eight columns of pixel image information.

111. A memory system as set forth in claim 1, further comprising:

a graphics processor generating graphics image information; and

a graphics writing circuit coupled to the two dimensional pixel block memory and coupled to the graphics processor, the graphics writing circuit writing the graphics image information generated by the graphics processor into the two dimensional array of blocks of pixel image information stored in the two dimensional pixel block memory.

112. A memory system as set forth in claim 1,

wherein the memory system is a video image data compression system;

wherein the two dimensional pixel block image memory is a two dimensional pixel block frame buffer memory storing the two dimensional array of blocks of pixel image information; and

wherein the accessing circuit is a sequential block memory accessing circuit sequentially generating pixel information included in accessed blocks of pixel image information by sequentially accessing pixel information included in blocks of pixel image information stored in the two dimensional pixel block frame the buffer memory.

113. A memory system as set forth in claim 2, wherein the buffer memory is an output single buffer memory storing the buffered output image information as double buffered output image information.

114. A memory system as set forth in claim 2, wherein the buffer memory is a double buffer memory storing the buffered output image information.

115. A memory system as set forth in claim 24,

wherein the frequency domain processor is a two dimensional fast Fourier transform frequency domain processor generating the frequency domain image information as two dimensional fast Fourier transformed frequency domain image information in response to the blocks of pixel image information accessed by the pixel block memory accessing circuit;

wherein the weight memory is a static random access memory kernel weight memory storing the weight information as a three row by three column kernel array of weight information; and

wherein the weighting processor is a kernel weighting processor generating the weighted frequency domain image information as kernel processed weighted frequency domain image information by weighting the frequency domain image information in response to the accessed weight information generated by the weight memory accessing circuit;

the memory system further comprising:

a three color digital to analog converter display circuit generating a three color display signal in response to the output weighted frequency domain image information generated by the output circuit; and

a CRT display monitor displaying an image in response to the three color display signal generated by the three color digital to analog converter display circuit;

116. A memory system as set forth in claim 24,

wherein the frequency domain processor is a frequency domain transform processor generating the frequency domain image information in response to the blocks of pixel image information accessed by the pixel block memory accessing circuit;

wherein the weight memory is a dynamic random access memory weight memory storing the weight information as quantization coefficient weight information; and

wherein the weighting processor is a quantization weighting processor generating the weighted frequency domain image information as quantized weighted frequency domain image information by weighting the frequency domain image information generated by the frequency domain processor in response to the accessed weight information generated by the weight memory accessing circuit.

117. A memory system as set forth in claim 24,

wherein the image input circuit is a data decompressed database memory image input circuit generating the input image information as data decompressed input image information;

wherein the two dimensional pixel block memory is a static random access memory storing the two dimensional array of blocks of pixel image information;

wherein the pixel block memory accessing circuit is a simultaneous pixel block memory accessing circuit simultaneously accessing each block of pixel image information stored in the two dimensional pixel block memory; and

wherein the output circuit is a red, green, blue digital to analog converter image output circuit generating the output weighted frequency domain image information as red, green, and blue output image information in response to the weighted frequency domain image information generated by the weighting processor.

118. A memory system as set forth in claim 24,

wherein the image input circuit is a data decompressed data link image input circuit generating the input image information as data decompressed input image information;

wherein the two dimensional pixel block memory is a dynamic random access memory storing the two dimensional array of blocks of pixel image information;

wherein the pixel block memory accessing circuit is a sequential pixel block memory accessing circuit sequentially accessing each block of pixel image information stored in the two dimensional pixel block memory; and

wherein the output circuit is a NTSC television digital to analog converter image output circuit generating the output weighted frequency domain image information as NTSC television output weighted frequency domain image information in response to the weighted frequency domain image information generated by the weighting processor.

119. A memory system as set forth in claim 1, further comprising:

an output circuit coupled to the two dimensional spatial processor and generating output data decompressed video image information in response to the data

compressed video image information generated by the two dimensional spatial processor; and

a display coupled to the output circuit and displaying an image in response to the output image data decompressed video information.

120. A memory system as set forth in claim 2, further comprising:

an output circuit coupled to the buffer memory and generating output data decompressed video image information in response to the buffered data compressed video image information stored by the buffer memory; and

a display coupled to the output circuit and displaying an image in response to the output data decompressed video image information.

121. A memory system as set forth in claim 3, further comprising:

an output circuit coupled to the buffer memory and generating output data decompressed video image information in response to the buffered data compressed video image information stored in the buffer memory; and

a display coupled to the output circuit and displaying an image in response to the output data decompressed image information.

122. A memory system as set forth in claim 4, further comprising:

an output circuit coupled to the buffer memory and generating output data decompressed video image information in response to the buffered data compressed

video image information stored by the buffer memory; and

a display coupled to the output circuit and displaying an image in response to the output data decompressed image information.

123. A memory system as set forth in claim 5, further comprising:

an output circuit coupled to the buffer memory and generating output data decompressed video image information in response to the buffered data compressed video image information stored by the buffer memory; and

a display coupled to the output circuit and displaying an image in response to the output data decompressed image information.

124. A memory system as set forth in Claim 6, further comprising:

an output circuit coupled to the buffer memory and generating output data decompressed video image information in response to the buffered data compressed video image information stored by the buffer memory; and

a display coupled to the output circuit and displaying an image in response to the output data decompressed image information.

125. A memory system as set forth in claim 7, further comprising:

an output circuit coupled to the buffer memory and generating output data decompressed video image information in response to the buffered data compressed

video image information stored by the buffer memory; and

a display coupled to the output circuit and displaying an image in response to the output data decompressed image information.

126. A memory system as set forth in claim 8, further comprising:

an output circuit coupled to the buffer memory and generating output data decompressed video image information in response to the buffered data compressed video image information stored by the buffer memory; and

a display coupled to the output circuit and displaying an image response to the output data decompressed image information.

127. A memory system as set forth in claim 9, wherein the output circuit further outputs data decompressed video image information, the memory system farther comprising:

a display coupled to the output circuit and displaying an image in response to the output data decompressed video image information output by the output circuit.

128. A memory system as set forth in claim 10, wherein the output circuit further outputs data decompressed video image information, the memory system further comprising:

a display coupled to the output circuit and displaying an image in response to the output data decompressed video image information output by the output circuit.

129. A memory system as set forth in claim 11, wherein the output circuit further outputs data decompressed video image information, the memory system further comprising:

a display coupled to the output circuit and displaying an image in response to the output data decompressed video image information output by the output circuit.

130. A memory system as set forth in claim 12, wherein the output circuit further outputs data decompressed video image information, the memory system further comprising:

a display coupled to the output circuit and displaying an image in response to the output data decompressed video image information output by the output circuit.

131. A memory system as set forth in claim 13, wherein the output circuit further outputs data decompressed video image information, the memory system further comprising:

a display coupled to the output circuit and displaying an image in response to the output data decompressed video image information output by the output circuit.

132. A memory system as set forth in claim 14, wherein the output circuit further outputs data decompressed video image information, the memory system further comprising:

a display coupled to the output circuit and displaying an image in response to the output data decom-

pressed video image information output by the output circuit.

133. A memory system as set forth in claim 17, further comprising:

a display coupled to the output circuit and displaying an image in response to the output image information generated by the output circuit.

134. A memory system as set forth in claim 18, further comprising:

a display coupled to the output circuit and displaying an image in response to the output image information generated by the output circuit.

135. A memory system as set forth in claim 19, further comprising:

a display coupled to the output circuit and displaying an image in response to the output image information generated by the output circuit.

136. A memory system as set forth in claim 20, further comprising:

a display coupled to the output circuit and displaying an image in response to the output image information generated by the output circuit.

137. A memory system as set forth in claim 22, further comprising:

a display coupled to the output circuit and displaying an image in response to the output image information generated by the output circuit.

138. A memory system as set forth in claim 23, further comprising:

a display coupled to the output circuit and displaying an image in response to the output image information generated by the output circuit.

139. A memory system as set forth in claim 24, further comprising:

a display coupled to the output circuit and displaying an image in response to the output weighted frequency domain image information generated by the output circuit.

140. A memory system as set forth in claim 25, further comprising:

a display coupled to the output circuit and displaying an image in response to the output image information generated by the output circuit.

141. A memory system as set forth in claim 34, further comprising:

a display coupled to the output circuit and displaying an image in response to the output smoothed weighted frequency domain image information generated hy the output circuit.

142. A memory system as set forth in claim 35, further comprising:

a display coupled to the output circuit and displaying an image in response to the output weighted image information generated by the output circuit.

143. A memory system as set forth in claim 36, further comprising:

a display coupled to the output circuit and displaying an image in response to the output smoothed

weighted frequency domain image information generated by the output circuit.

144. A memory system as set forth in claim 37, further comprising:

a display coupled to the output circuit and displaying an image in response to the output weighted image information generated by the output circuit.

145. A memory system as set forth in claim 42, further comprising:

a display coupled to the output circuit and displaying an image in response to the output smoothed weighted frequency domain image information generated by the output circuit.

146. A memory system as set forth in claim 43, further comprising:

a display coupled to the output circuit and displaying an image in response to the output smoothed weighted image information generated by the output circuit.

147. A memory system as set forth in claim 44, further comprising:

a display coupled to the output circuit and displaying an image in response to the output smoothed weighted image information generated by the output circuit.

148. A memory system as set forth in claim 45, further comprising:

a display coupled to the output circuit and displaying an image in response to the output smoothed

weighted image information generated by the output circuit.

149. A memory system as set forth in claim 49, further comprising:

a display coupled to the output circuit and displaying an image in response to the output weighted frequency domain image information generated by the output circuit.

150. A memory system as set forth in claim 50, further comprising:

a display coupled to the output circuit and displaying an image in response to the output weighted frequency domain image information generated by the output circuit.

151. A memory system as set forth in claim 51, further comprising:

a display coupled to the output circuit and displaying an image in response to the output weighted image information generated by the output circuit.

152. A memory system as set forth in claim 52, further comprising:

a display coupled to the output circuit and displaying an image in response to the output image information generated by the output circuit.

153. A process of operating a memory system as set forth in claim 81, further comprising the act of making a product in response to the output image information.

154. A process of operating a memory system as set forth in claim 82, further comprising the act of making a product in response to the output image information.

155. A process of operating a memory system as set forth in claim 83, further comprising the act of making a product in response to the output image information.

156. A process of operating a memory system as set forth in claim 84, further comprising the act of making a product in response to the output image information.

157. A process of operating a memory system as set forth in claim 85, further comprising the act of making a product in response to the two dimensional spatially processed image information.

158. A process of operating a memory system as set forth in claim 95, further comprising the act of making a product in response to the buffered output image information.

159. A process of operating a memory system as set forth in claim 96, further comprising the act of making a product in response to the buffered two dimensional spatially processed image information.

160. A process of operating a memory system as set forth in claim 97, further comprising the act of making a product in response to the buffered two dimensional spatially processed image information.

161. A process of operating a memory system as set forth in claim 98, further comprising the act of making a product in response to the output image information.

162. A process of operating a memory system as set forth in claim 99, further comprising the act of making a product in response to the output image information.

163. A process of operating a memory system as set forth in claim 100, further comprising the act of making a product in response to the output image information.

164. A process of operating a memory system as set forth in claim 101, further comprising the act of making a product in response to the output image information.

165. A process of operating a memory system as set forth in claim 102, further comprising the act of making a product in response to the output weighted frequency domain image information.

166. A process of operating a memory system as set forth in claim 103, further comprising the act of making a product in response to the output weighted image information.

167. A process of operating a memory system as set forth in claim 104, further comprising the act of making a product in response to the output weighted image information.

168. A process of operating a memory system as set forth in claim 105, further comprising the act of making a product in response to the output weighted image information.

169. A process of operating a memory system as set forth in claim 106, further comprising the act of making a product in response to the output smoothed weighted frequency domain image information.

170. A process of operating a memory system as set forth in claim 107, further comprising the act of making a product in response to the output smoothed weighted image information.

171. A process of operating a memory system as set forth in claim 108, further comprising the act of making a product in response to the output smoothed weighted image information.

172. A process of operating a memory system as set forth in claim 109, further comprising the act of making a product in response to the output smoothed weighted image information.

UNITED STATES DEPARTMENT OF COMMERCE

PATENT AND TRADEMARK OFFICE
Address: COMMISSIONER OF PATENTS
AND TRADEMARKS
Washington, D.C. 20231

* * * * *

Serial Number: 08/471,702

Art Unit: 2415

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed 4/18/97 fails to comply with 37 CFR 1.97(c) because it does not include either a certification as specified in 37 CFR 1.97(e) or the fee set forth in 37 CFR 1.17(p). This information disclosure statement also fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. The reference to related patent application serial no. 08/469,939 as containing the first page of the references cited in this information disclosure statement is noted but this application is not a parent application of this application. The reference to other patent applications is noted but this broad statement does not prove that the references cited on pages 2-5 are present in a parent application. Note 37 CFR 1.98(d) and MPEP 609 paragraph A(2). This information disclosure statement has been placed in the

application file, but the information referred to therein has not been considered

2. The information disclosure statement filed 8/28/95 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. The reference to related patent application serial no. 08/435,894 as containing all of the references cited in this information disclosure statement except for the textbooks is noted. However, this application is not at this time available to the examiner. Furthermore, submission of the references in a related application does not satisfy 37 CFR 1.98(d) and MPEP 609 both of which requires that the only time that references may not be submitted is when those references are present in a parent application. The reference to patent application serial no. 08/417,530 as containing the references cited on sheets 6/10 to 8/10 is noted but a review of that file reveals that those references are not present in that application. Furthermore, this application is not a parent application of this application. The reference to patent application serial no. 08/431,640 as containing the references cited on sheets 1/10 to 5/10 is noted but this application is not at this time available to the examiner. Furthermore, this application is not a parent application of this application. The reference to patent application serial no. 07/289,355 is noted but this application is not a parent application of this application. Thus, the information disclosure statement filed 8/28/95 fails to comply with 37 CFR 1.98(a)(2) and 1.98(d). This information disclosure statement has been placed in the application

file, but the information referred to therein has not been considered.

Response to Amendment

3. The amendments to the specification filed on 2/7/97 has been entered.

4. The amendment filed on 4/18/97 has been entered in part. All amendments have been entered except for the amendment to page 2 line 5 located at the bottom of page 3 of applicants response. The amendment to page 2 line 5 located at the bottom of page 3 of applicants response has not been entered because after the instructions on page 2 of applicants response have been entered "Hyatt." is not present.

Drawings

5. The proposed drawing correction, filed on 2/7/97 has not been approved because MPEP 608.02(v) does not allow for the omission of a sketch showing the proposed changes. MPEP 608.02(v) is reproduced below. 608.02(v)

Drawing Changes Which Require Sketches

When changes are to be made in the drawing itself, other than mere changes in reference characters, designations of figures, or inking over lines pale and rough, a print or pen-and-ink sketch must be filed showing such changes in red ink or with the changes otherwise highlighted. Ordinarily, broken lines may be changed to full without a sketch.

Sketches filed by an applicant and used for correction of the drawing will not be returned. All such sketches must be in ink or permanent prints.

Specification

6. The abstract of the disclosure is objected to because the originally filed abstract does not correspond to the invention defined by the claims. Correction is required. See MPEP § 608.01(b).

Claim Objections

7. Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 are objected to under 37§1.75(d)(1). The claim or claims do not conform to the invention as set forth in the remainder of the specification and the terms and phrases used in the claims do not find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description. The claims do not conform to the specification for the reasons given below in the rejections under 35 U.S.C. 112, first paragraph.

Oath/Declaration

7. This application presents a claim for subject matter not originally claimed or embraced in the statement of the invention. The originally filed claims in this application did not claim the kernel processor of the currently pending claims. A supplemental oath or declaration is required under 37 CFR 1.67. The new oath or declaration must properly identify the application of which it is to form a part, preferably by application number and filing date in the body of the oath or declaration. See MPEP §§ 602.01 and 602.02.

Claim Rejections - 35 USC § 112

8. The claims of this application are directed to the portions of the specification which describe a vector mem-

ory storing vectors, reading the vectors from the vector memory, sending the read vectors to the address generators, strobing (writing) color values into image memory at the locations defined by the address generators, reading the image memory during display system readout, storing the readout values in a buffer memory, applying in parallel 9 pixels of information from the buffer memory to a spatial filter, applying the spatially filtered pixel information to a digital to analog convertor, and sending the analog signal to a monitor. It is clear from the following rejections based upon 35 U.S.C. 112, first paragraph, that the claims of this application are not supported and/or enabled by the specification.

9. Claims 1-14 and 119-132 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 1-14 and 119-132 claim "a data decompressed video image input circuit generating data decompressed image information". The claimed feature of a circuit for compressing video image information was not described in the specification at the time of filing this application nor at the time of filing parent application serial no. 06/662,211. This specification briefly describes compressing database images and data compression but the specification is totally silent as to compressing video images or to compressing images. The specification at page 23 lines 1-18 states "Image processing can be performed on digitized images stored in the database. A stored image can be loaded from the database into image memory for image processing online with a hardware-implemented

image processor. A stored image can be preprocessed, such as offline in the database and such as online with a preprocessor. Offffine processing can be performed during database generation, such as filtering database images before storing the images in the database. Online preprocessing can be performed during system operation, such as by accessing database images and preprocessing the accessed database images with compression and filtering, prior to loading into image memory. Offline preprocessing can be performed for filtering of images, which is illustrative of other forms of offline preprocessing and is also illustrative of online preprocessing. For example, other forms of offline preprocessing includes data compression, image enhancement, and other forms of filtering. Also, other forms of online preprocessing includes data decompression, image expansion, image compression, and filtering.". Thus, applicants originally filed specification does not manifest that applicant had possession of the currently claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

10. Claims 1-14 and 119-132 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 1-14 and 119-132 claim "a data decompressed video image input circuit generating data decompressed graphic image information". The claimed feature of a circuit for or method of compressing video image information was not enabled in the specifi-

cation at the time of filing this application nor at the time of filing parent application serial no. 06/662,211. Thus, applicants specification fails to enable one of ordinary skill in the art at the time of filing the parent to practice applicants invention.

11. Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 1-14,17-20, 22-25, 34-37, 42-45, 49-52, 81-85, 95-112, 117, and 118 claim a writing circuit and an accessing circuit for writing and reading a block of video pixel image data into the block memory or the process of writing and reading a block of video pixel image data into the block memory. These claims cover simultaneous writing and reading of a block of graphic image data (note claims 110 and 117). Claims 112 or 118 solve the accessing problem but does not solve the writing. The specification does not describe this. This claimed feature was not described in the specification at the time of filing this application nor at the time of filing parent application serial no. 06/662,211. The specification describes a sequential write to and read from the block memory. Thus, applicants originally filed specification does not manifest that applicant had possession of the currently broadly claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

12. Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, 95-110, 112, 117, and 118 claim a writing circuit and an accessing circuit for writing and reading a block of video pixel image data into the block memory. These claims cover simultaneous writing and reading of a block of video pixel image data (note claims 110 and 117). Claims 112 or 118 solve the accessing problem but does not solve the writing. The specification does not describe this. The specification describes a sequential write to and read from the block memory. The specification fails to enable one of ordinary skill in the art at the time of filing this application and at the time of filing parent application serial no. 06/662,211 to build a circuit which simultaneously writes block of information into the block memory or to build a circuit which simultaneously reads a block of information out the block memory.

13. Claims 1, 2, 5, 9, 10, 12, 20, 81, 85, 98, 110-114, 119, 120, 123, 127, 128, 130, 136, 153, 157, and 161 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 1, 2, 5, 9, 10, 12, 20, 81, 85, and 98 claim a vector processor responsive to an accessed block of video pixel image information and to vec-

tor information. This feature of the claims is not supported by applicants originally filed specification nor by parent application serial no. 06/662,211. Thus, applicants originally filed specification does not manifest that applicant had possession of the currently claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

14. Claims 1, 2, 5, 9, 10, 12, 20, 81, 85, 98, 110-114, 119, 120, 123, 127, 128, 130, 136, 153, 157, and 161 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 1, 2, 5, 9, 10, 12, 20, 81, 85, and 98 claim a vector processor responsive to an accessed block of video pixel image information and to vector information. This feature of the claims is not enabled by applicants originally filed specification nor by parent application serial no. 06/662,211. Thus, applicants specification fails to enable one of ordinary skill in the art at the time of filing to practice applicants invention.

15. Claims 3, 4, 11, 121, 122, and 129 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 3, 4, and 11 claim a processor responsive to an accessed block of video pixel image information. This feature of the claims is not supported by applicants orig-

inally filed specification nor by parent application serial no. 06/662,211. Thus, applicants originally filed specification does not manifest that applicant had possession of the currently claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CAFC, 6/7/91).

16. Claims 3, 4, 11, 121, 122, and 129 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 3, 4, and 11 claim a processor responsive to an accessed block of video pixel image information. This feature of the claims is not enabled by applicants originally filed specification nor by parent application serial no. 06/662,211. Thus, applicants specification fails to enable one of ordinary skill in the art at the time of filing to practice applicants invention.

17. Claims 1, 85, 95, 110-112, 119, 157, and 158 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 1, 85, and 95 claim a spatial processor responsive to an accessed block of video pixel image information and to vector information and generating data compressed video. This feature of the claims is not supported by applicants originally filed specification nor by parent application serial no. 06/662,211.

Thus, applicants originally filed specification does not manifest that applicant had possession of the currently claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CAFC, 6/7/91).

18. Claims 1, 85, 95, 110-112, 119, 157, and 158 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 1, 85, and 95 claim a spatial processor responsive to an accessed block of video pixel image information and to vector information and generating data compressed video. This feature of the claims is not enabled by applicants originally filed specification nor by parent application serial no. 06/662,211. Thus, applicants specification fails to enable one of ordinary skill in the art at the time of filing to practice applicants invention.

19. Claims 6-9, 13, 14, 24, 34, 36, 42, 49, 50, 102, 106, 115-118, 124-127, 131, 132, 139, 141, 143, 145, 149, 150, 165, and 169 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 6-9, 13, 14, 24, 34, 36, 42, 49, 50, 102, 106, 115-118, 139, 141, 143, 145, 149, 150, 165, and 169 claim a frequency domain processor or generating frequency domain image information or frequency domain information. The specification does not describe frequency domain, frequency domain pro-

cessor, frequency domain image information or frequency domain information. This claimed feature was not described in the specification at the time of filing this application nor at the time of filing parent application serial no. 06/662,211. Thus, applicants originally filed specification does not manifest that applicant had possession of the currently claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CAFC, 6/7/91).

20. Claims 6-9, 13, 14, 24, 34, 36, 42, 49, 50, 102, 106, 115-118, 124-127, 131, 132, 139, 141, 143, 145, 150, 165, and 169 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 6-9, 13, 14, 24, 34, 36, 42, 49, 50, 102, 106, 115-118, 139, 141, 143, 145, 149, 150, 165, and 169 claim frequency a frequency domain processor or generating frequency domain image information or frequency domain information. The specification does not enable one of ordinary skill in the art at the time of filing this application nor at the time of filing the parent application to build a system using frequency domain, frequency domain processor, frequency domain image information, or frequency domain information. This claimed feature was not enabled by the specification at the time of filing thisapplication nor at the time of filing parent application serial no. 06/662,211. Thus, applicants specification fails to enable one of ordinary skill in

the art at the time of filing to practice applicants invention.

21. Claims 17, 18, 133, and 134 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 17 and 18 claim a block processor responsive to an accessed block of pixel image information and to vector information. This feature of the claims is not supported by applicants originally filed specification nor by parent application serial no. 06/662,211. Thus, applicants originally filed specification does not manifest that applicant had possession of the currently claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

22. Claims 17, 18, 133, and 134 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 17 and 18 claim a processor responsive to an accessed block of pixel image information and to vector information. This feature of the claims is not enabled by applicants originally filed specification nor by parent application serial no. 06/662,211. Thus, applicants specification fails to enable one of ordinary skill in the art at the time of filing to practice applicants invention.

23. Claims 24, 34-37, 42-45, 49-51, 102-109, 115-118, 139-151, and 165-172 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. No claims in this application directly claim an input weight circuit generating input weight information, however, claims 24, 34-37, 42-45, 49-51, 102-109, 115, and 116 claim other weight related elements. An input weight circuit generating input weight information is not supported by the specification. This implicitly claimed feature was not described in the specification at the time of filing this application nor at the time of filing parent application serial no. 06/662,211. The specification at page 147 lines 12-17 and figures 6Y and 6Z teach applying addresses through multiplexers U5C and U6C to the address inputs of RAMs U5E and U6E so these RAMs may store weight addresses supplied on input lines IO0 to IO3 from address generators. The same lines of page 147 describe the line buffers U4F to U6F as applying the intensity bits from image memory to RAMs U3E and U4E and applying the weight addresses from the address generators to RAMs U5E and U6E. Page 142 lines 13 to 29 and figure 6X describe an address counter for generating the addresses to be applied to the address lines of RAMs U3E, U4E, U5E, and U6E so these RAMS will be able to store the intensity and weight addresses at storage locations determined by the addresses. Page 149 lines 1-9 describes reading the weight addresses from RAMs U5E and U6E and applying those weight addresses on a weight bus. Page 162 lines 5-7 describes outputting the weight addresses stored in the line buff-

ers to the weight RAMs U21E to U23E for accessing of the weights associated therewith in order for those weights to be applied to the spatial filter (spatial filter shown in figure 5A). Page 12 lines 1-6 describes using address generators for performing a vector to raster conversion by using the address generators to step through addresses and by strobing a color value into each memory location represented by each address of the generated addresses. Pages 118 to 127 and figures 6O to 6R describes address generators for generating addresses. Applicant has failed to describe an address generator which will generate weight addresses and has failed to describe an address generator which will apply the weight addresses to the inputs of RAMS U5E and U6E at the same time the intensity bits are being applied to RAMS U3E and U4E. This portion of applicants specification is critical in supporting the claimed invention because each weight address associated with an intensity value for a pixel must select a weight value from the weight table which will perform the correct filtering of a matrix of pixels in the spatial filter in order for the desired filtered image to be generated. Applicant has thus failed to teach an address generator which will generate weight addresses for selecting weight values from the weight table to perform the desired weighting function at the spatial filter. Thus, applicants originally filed specification does not manifest that applicant had possession of the currently claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

24. Claims 24, 34-37, 42-45, 49-51, 102-109, 115-118, 139-151, and 165-172 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. No claims in this application directly claim an input weight circuit generating input weight information, however, claims 24, 34-37, 42-45, 49-51, 102-109, 115, and 116 claim other weight related elements. Claims 24, 34-37, 42-45, 49-51, 102-109, 115, and 116 rely upon the input weight circuit for supporting the weight functions performed by the other weight elements. The specification, at the time of filing this application and at the time of filing parent application serial no. 06/662,211, does not enable one of ordinary skill in the art to build an address generator which will generate weight addresses and to build an address generator which will apply the weight addresses to the inputs of RAMS U5E and U6E at the same time the intensity bits are being applied to RAMS U3E and U4E. This portion of applicants specification is critical in supporting the claimed invention because each weight address associated with an intensity value for a pixel must select a weight value from the weight table which will perform the correct filtering of a matrix of pixels in the spatial filter in order for the desired filtered image to be generated. Therefore, at the time of filing the oldest parent application, applicant has also failed to enable one of ordinary skill in the art with the knowledge to build an address generator which will generate weight addresses for selecting weight values from the weight table in order to perform the desired weighting function at the spatial filter. Thus, applicants specification fails to enable one of ordi-

nary skill in the art at the time of filing to practice applicants invention and to build a complete working kernel processor.

25. Claims 34, 36, 42-45, 106-109, 141-148, and 169-172 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 34, 36, 42-45, and 106-109 claim block boundary smoothing. This type of processing was not described in the specification. This claimed feature was not described in the specification at the time of filing this application nor at the time of filing parent application serial no. 06/662,211. Thus, applicants originally filed specification does not manifest that applicant had possession of the currently claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

26. Claims 34, 36, 42-45, 106-109, 141-148, and 169-172 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 34, 36, 42-45, and 106-109 claim block boundary smoothing. This type of processing was not described in the specification. The specification does not enable one of ordinary skill in the art at the time of filing the parent application to build a memory system using a block boundary processor or generating block boundary

smoothing information. Thus, applicants specification fails to enable one of ordinary skill in the art at the time of filing to practice applicants invention.

27. Claim 112 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. This claim claims that the memory system is a video image data compression system. This claimed feature was not described in the specification at the time of filing this application nor at the time of filing parent application serial no. 06/662,211. Thus, applicants originally filed specification does not manifest that applicant had possession of the currently claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

28. Claim 112 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. This claim claims that the memory system is a video image data compression system. This claimed feature was not enabled by the specification at the time of filing this application nor at the time of filing parent application serial no. 06/662,211. Thus, applicants specification fails to enable one of ordinary skill in the art at the time of filing to practice applicants invention.

29. Claim 116 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. This claim claims a quantization weighting processor. This processor was not described in the specification. This claimed feature was not described in the specification at the time of filing this application am at the time of filing parent application serial no. 06/662,211. Thus, applicants originally filed specification does not manifest that applicant had possession of the currently claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

30. Claim 116 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. This claim claims a quantization weighting processor. The specification does not enable one of ordinary skill in the art at the time of filing the parent application to build a memory system using a quantization weighting processor. Thus, applicants specification fails to enable one of ordinary skill in the art at the time of filing to practice applicants invention.

31. Claims 2-14, 113, 114, and 120-132 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the

relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 2-14 claim generating data compressed video image information. This type of image information was was not described in the specification let alone the processor needed to perform the generation. Thus, this claimed feature was not described in the specification at the time of filing this application nor at the time of filing parent application serial no. 06/662,211. Thus, applicants originally filed specification does not manifest that applicant had possession of the currently claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

32. Claims 2-14, 113, 114, and 120-132 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 2-14 claim generating data compressed video image information. This type of image information was was not enalbed in the specification let alone the processor needed to perform the generation. The specification does not enable one of ordinary skill in the art at the time of filing the parent application to build a memory system using a quantization weighting processor. Thus, applicants specification fails to enable one of ordinary skill in the art at the time of filing to practice applicants invention.

33. Claims 153-172 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to

reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. These claims claim the act of making a product in response to image information. The originally filed specification did not describe making a product in response to information. This claimed feature was not described in the specification at the time of filing this application nor at the time of filing parent application serial no. 06/662,211. Thus, applicants originally filed specification does not manifest that applicant had possession of the currently claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

34. Claims 153-172 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. These claims claim the act of making a product in response to image information. The originally filed specification did not describe making a product in response to information. This claimed feature was not enabled by the specification at the time of filing this application nor at the time of filing parent application serial no. 06/662,211. Thus, applicants specification fails to enable one of ordinary skill in the art at the time of filing to practice applicants invention.

Double Patenting

35. The non-statutory double patenting rejection, whether of the obviousness-type or non-obviousness-type, is based on a judicially created doctrine grounded

in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985) *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely flied terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a non-statutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal, disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

36. Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-162 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over:

claims 17-20, 22-25, 42-45, 49-52, 71-74, 81-85, and 110-162 of copending Application No. 08/472,062;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 96-173 of copending Application No. 08/479,088;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 of copending Application No. 08/471,925;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 of copending Application No. 08/479,086;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-/72 of copending Application No. 08/479,087;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 of copending Application No. 08/471,712;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 96-173 of copending Application No. 08/471,704; and

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 90-167 of copending Application No. 08/483,016. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims in these nine copending applications claim a memory system for storing image information and for processing the stored image information and for outputting the processed image information. The minor differences between the claims in these nine applications are obvious variations of the same claimed invention. A grant of a second patent from these nine patent applications would unjustly extend the right given in a first patent from these nine patent applications.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

37. Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-162 are provisionally rejected under the judicially created doctrine of double patenting over:

claims 17-20, 22-25, 42-45, 49-52, 71-74, 81-85, and 110-162 of copending Application No. 08/472,062;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 96-173 of copending Application No. 08/479,088;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 of copending Application No. 08/471,925;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 of copending Application No. 08/479,086;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 of copending Application No. 08/479,087;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 of copending Application No. 08/471,712;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 96-173 of copending Application No. 08/471,704; and

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 90-167 of copending Application No. 08/483,016. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows: the claims in these nine copending applications claim a memory system for storing image information and for processing the stored image information and for outputting the processed image information. The minor differences between the claims in these nine applications are obvious variations of the same claimed invention. A grant of a second patent from these nine patent applications would

unjustly extend the right given in a first patent from these nine patent applications.

Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Claim Rejections - 35 USC § 102

38. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless—
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

39. Claims 22, 23, 83, 84, 95, 137, and 138 are rejected under 35 U.S.C. 102(b) as being anticipated by Hill U.S. Patent No. 4,200,867. Hill describes a picture matrix memory which stores a block of video data. A processor (MPU 162) is connected to a memory accessing circuit and thus generates output video image information which is then stored in a buffer memory (shift registers 400A, 400B, 400C).

40. Claims 82 and 99 are rejected under 35 U.S.C. 102(b) as being anticipated by Hill U.S. Patent No. 4,200,867. The MPU generates the video image information at a first word rate and the shift registers output the video image information at a second word rate.

Claim Rejections - 35 USC § 103

41. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

42. Claims 19, 25, 96, 100, 101, 140, and 135 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lord et al U.S. Patent No. 4,322,750 and Hill U.S. Patent No. 4,200,867 and Lelke U.S. Patent No. 4,069,511. Lord et al describes a memory system for a display system were a spatial processor 21 is connected to an accessing circuit 20 for reading a block of image information. Lord does not describe the field store as being formed with blocks of storage locations and Lord does not describe a buffer connected to the output of the spatial processor. Lelke shows that it is old and well known to form a field memory with blocks of memory locations. Figures 6 and 13 show a field memory formed out of blocks of storage locations with figure 13 showing a block of memory locations. Hill shows that it is old and well known to use a buffer memory (shift registers 400A, 400B, 400C) to store the output of a processor. It would have been obvi-

ous to one of ordinary skill in the art at the time of applicants invention to use a block memory in Lord because the chips from which the memory is formed from lead one of ordinary skill in the art to forming a field memory with blocks of chips. It would have been obvious to one of ordinary skill in the art at the time of applicants invention to use a buffer memory to temporally store the output of the spatial processor in order to buffer the data prior to sending the spatially filtered image information to an output device.

Re claims 25, 100, 101, and 140:

These claims add the additional feature of a first clock and a second clock. The processor of Hill operates at one clock rate while the shift registers output the video image information at a second word rate. Thus, it would have been obvious to one of ordinary skill in the art at the time of applicants invention access the image memory at one clock rate while operating the buffers at a second clock rate.

43. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any exten-

sion fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

44. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffery A. Brier whose telephone number is (703) 305-4723. The examiner can normally be reached on Monday through Friday from 8:15am to 4:45pm eastern time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Powel, can be reached on (703) 305-3900. The fax phone number for this Art Unit is (703)-305-6606.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

July 30, 1997

JEFFERY BRIER
PRIMARY EXAMINER
GROUP 2600

UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

IN RE APPLICATION OF
GILBERT P. HYATT

SERIAL NO. 08/471,702
DOCKET NO. 516
GROUP ART UNIT: 2775
EXAMINER: JEFFERY BRIER

Filed: June 6, 1995
[Received:]

APPEAL BRIEF

For: A DATA COMPRESSION SYSTEM

Hon. Assistant Commissioner For Patents
Washington, D.C. 20231

ATTENTION: Board of Patent Appeals and Interferences

This is an Appeal from the action of the Primary Examiner finally rejecting all claims (claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172). An Ap-

peal Brief in compliance with 37 CFR 1.192 is provided hereinafter.

For efficiency, abbreviations are used herein.[1]

---

[1] "Board" => the PTO Board of Patent Appeals and Interferences
"MPEP" => the PTO Manual of Patent Examining Procedure
'102 => 35 USC 102
'103 => 35 USC 103
'112-1 => 35 USC 112, first paragraph
"instant claims" => the claims in the instant application
"copending claims" => the claims in the subject copending applications
"Spec. at 20" => a cite to the instant specification at page 20
"at 10" => a cite to page 10
"at 10:5-8" => a cite to page 10 at lines 5-8
"at 10:5-13:7" => a cite to pages 10 line 5 through page 13 line 7

TABLE OF CONTENTS[2]

I. THE REAL PARTY IN INTEREST 8

II. RELATED APPEALS AND INTERFERENCES 8

III. STATUS OF CLAIMS 8

IV. STATUS OF AMENDMENTS 8

V. SUMMARY OF THE INVENTION 9

VI. ISSUES 14

VII. GROUPING OF CLAIMS 15

VIII. ARGUMENT 16

8.1 ARGUMENTS COMMON TO THE 35 USC 112-1 ENABLEMENT AND WRITTEN DESCRIPTION REJECTIONS 16

8.1.1 The Instant Disclosure Being The Same As In Ancestor Patent 5,584,032 Is Legally Correct And Presumptively Valid 17

8.1.2 The Examiner Expressly Admits That The Instant Disclosure Is Adequate . 19

8.1.3 The '112-1 Rejections Fail To Consider The Disclosure As A Whole 20

8.1.4 The '112-1 Rejections Are Erroneously Based Upon Unclaimed Subject Matter 21

---

[2] The "Conclusion" section headings appearing in this Appeal Brief are not listed in this Appeal Brief's the Table of Contents.

TABLE OF CONTENTS (CONTINUED)

8.1.5 The Examiner Alleges Insufficient Disclosure While Ignoring Hundreds Of Relevant Recitations In The Disclosure 23

8.1.6 The '112-1 Rejections Regarding Product Terminology Are Improper In Light Of The Statute And The Law Of The Federal Circuit 29

8.1.7 The Product Terminology Objected To Based On '112-1 Has Ample Antecedent Basis In The Instant Disclosure 32

8.1.8 The 112-1 Rejections Do Not Establish A Prima Facie Case 34

8.2 35 USC 112-1 ENABLEMENT REJECTION 38

8.2.1 The Disclosure Is Enabling, Having Schematic Details Down To The Component Level 38

8.2.2 The Disclosure Makes Extensive Use Of Commercially Available Products And Integrated Circuit Components 40

8.2.3 The Enablement Rejection Improperly Ignores The Skill In The Art 44

8.2.4 The Enablement Rejection Does Not Establish A Prima Facie Case 47

8.3 35 USC 112-1 WRITTEN DESCRIPTION REJECTION REGARDING A LIST OF ALLEGED CLAIM LIMITATIONS 48

8.3.1 Claim Terminology Does Not Have To Be Stated Verbatim In The Disclosure To Satisfy The Written Description Requirement 48

8.3.2 The Written Description Rejection Does Not Establish A Prima Facie Case ... 51

(CONTINUED)

TABLE OF CONTENTS (CONTINUED)

8.4 ARGUMENTS COMMON TO THE OBVIOUSNESS-TYPE AND NONOBVIOUSNESS-TYPE DOUBLE PATENTING REJECTIONS 52

8.4.1 The Double Patenting Rejections Overlook Restriction Requirements 53

8.4.2 The Instant Claims Are Independent Or Distinct From The Claims Of The Copending Applications 57

8.4.3 There Are Many Novel Differences Between The Instant Claims And The Copending Claims 58

8.4.4 The Double Patenting Rejections Do Not Even Provide A Claim-By-Claim Analysis, Much Less The Limitation-By-Limitation Analysis Required By The Federal Circuit 61

8.4.5 Simultaneous Issuance Of The Instant And Copending Patent Applications Would Obviate The Double Patenting Rejections 64

8.4.6 The Double Patenting Rejections Do Not Establish A Prima Facie Case 66

8.5 OBVIOUSNESS-TYPE DOUBLE PATENTING REJECTION 70

8.6 NONOBVIOUSNESS-TYPE DOUBLE PATENTING REJECTION 72

8.6.1 The Controlling Two-Part Test For Double Patenting Has Been Established By In Re Vogel 72

8.6.2 The Board Should Not Ignore In Re Vogel By Creating A Third Test For Double Patenting 75

8.6.3 The Present Claims Satisfy The Overruled Schneller Inquiries For Double Patenting 76

(CONTINUED)

TABLE OF CONTENTS (CONTINUED)

8.6.4 Schneller Only Applies Where The Patent Claims And The Application Claims Are Directed To The Same Preferred Embodiment 76

8.6.5 The Facts In The Instant Application Are Significantly Different From The Facts Of Schneller 78

8.6.5.1 Introduction 78

8.6.5.2 Schneller's Invention Is A Unitary Device, A Single Piece Of Wire Having Five Bends 80

8.6.5.3 The Present Case Has Ample Justification For Multiple Applications .. 81

8.6.5.4 The Claims In The Instant Application Are Not "Covered" By The Copending Application Claims 83

8.6.5.5 It Is Contrary To Schneller To Reject The Instant Claims Over Copending Applications 84

8.6.6 Schneller Is Distinguished Pursuant To In re Heinle 84

8.6.7 The Examiner Improperly Attempts To Support The Rejection With Uninformative Schneller Cliches 85

8.6.8 The Nonobviousness-Type Double Patenting Rejection Does Not Establish A Prima Facie Case 86

(CONTINUED)

TABLE OF CONTENTS (CONTINUED)

8.7 ARGUMENTS COMMON TO BOTH THE 35 USC 102 ANTICIPATION REJECTION AND THE 35 USC 103 OBVIOUSNESS REJECTION 90

8.7.1 The Art Rejections Do Not Even Provide A Claim-By-Claim Analysis, Much Less The Limitation-By-Limitation Analysis Required By The Federal Circuit 91

8.7.2 The Present Examiner Was Previously Reversed By The Board For Similarly Improper Rejections 93

8.7.3 The Art Rejections Do Not Establish A Prima Facie Case 95

8.8 35 USC 102 ANTICIPATION REJECTION 100

8.8.1 The '102 Rejection Does Not Provide The Identity Required By The Federal Circuit 100

8.8.2 The '102 Rejection Overlooks The Many Novel Differences Between The Instant Claims And The References 102

8.8.3 The '102 Rejection Does Not Establish A Prima Facie Case 108

8.9 35 USC 103 OBVIOUSNESS REJECTION 110

8.9.1 The '103 Rejection Relies Upon Improper Hindsight 110

8.9.2 The '103 Rejection Does Not Perform The Required Graham Analysis 115

8.9.3 The Claims Distinguish Over The References 117

8.9.4 The '103 Rejection Does Not Establish A Prima Facie Case 121

(CONTINUED)

TABLE OF CONTENTS (CONTINUED)

8.10 THE 35 USC 112-1 AND THE DOUBLE PATENTING REJECTIONS ARE JUDICIALLY ESTOPPED 125

8.11 THE APPELLANT IS ENTITLED TO A PATENT 126

IX. CONCLUSION 128

EXHIBIT-1 ..... E1-1

TABLE OF CONTENTS (INSTANT DISCLOSURE)

EXHIBIT-2 ..... E2-1

CLAIM CHARTS

EXHIBIT-3 ..... E3-1

COMBINATIONS OF CONTESTED LIMITATIONS

EXHIBIT-4 ..... E4-1

EXCERPTS FROM BASIC COMPUTER PROGRAMMING DOCUMENTATION

I. THE REAL PARTY IN INTEREST

The real party in interest is the Appellant, Gilbert P. Hyatt.

II. RELATED APPEALS AND INTERFERENCES

Appeals are being filed substantially contemporaneously herewith in the instant application and in eight copending applications, all nine of which are listed below.

DKT. NO.	SERIAL NO.
510	08/479,088
511	08/471,712
513	08/479,086
516	08/471,702
517	08/479,087
518	08/471,925
524	08/472,062
546	08/483,016

III. STATUS OF CLAIMS

Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 are pending in the instant application.

No claims are allowed.

Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 stand finally rejected and are appealed herein.

IV. STATUS OF AMENDMENTS

All amendments have been considered by the Examiner.

V. SUMMARY OF THE INVENTION

The appealed claims are directed to a system having novel combinations of features (e.g., novel memory and processor combinations). The disclosure of these features is arranged in a "top-down"[3] form. Both the figures and the description related thereto are arranged in this "top-down" form. The disclosure ptovides both an end-to-end system-configuration and details down to the electronic component, pin, and wire level of detail. The application discloses an entire system (e.g., Fig. 1) from an input device to an output device (e.g., a display output device) and discloses highly detailed schematic diagrams down to the individual component and individual wire level of detail (e.g., Figs. 6B-6D).

A system block diagram is shown in Fig. 1 with various blocks that are shown in greater detail in other figures. For example, an input device 115A (Fig. 1) is shown in detailed schematic form in Figs. 6U and 6V, an address generator 115B (Fig. 1) is shown in detailed schematic form in Figs. 6O-6R, a memory 115C (Fig. 1) is shown in detailed schematic form in Figs. 6E-6N, a buffer 115D (Fig. 1) is shown in detailed schematic form in Figs. 6X-6AF, and an output device 115E (Fig. 1) is shown in detailed schematic form in Figs. 6S and 6T.

---

[3] The top-down disclosure includes a more general top level shown in block diagram form down to a very detailed level of schematic diagrams with actual commercially available integrated circuit components and actual wires shown between numbered pins on the integrated circuit components.

Furthermore, Fig. 6A illustrated another block diagram with various blocks that are shown in greater detail in other figures. For example, control logic 610B (Fig. 6A) is shown in detailed schematic form in Figs. 6B-6D, address generators 610C (Fig. 6A) are shown in detailed schematic form in Figs. 6O-6R, memory 610D (Fig. 6A) is shown in detailed schematic form in Figs. 6E-6N, and a buffer 610E (Fig. 6A) is shown in detailed schematic form in Figs. 6X-6AF.

Intermediate level figures are provided to further disclose the invention. For example, Fig. 2 provides intermediate level detail[4] to further illustrate the address generator block 115E (Figs. 1 and 2) and the memory block 115C (Figs. 1 and 2). Other figures (e.g., Fig. 5A, 5D; 6A, and 6E) also provide various intermediate levels of detail.

The figures are described in detail in the extensive specification comprising over 200 pages of description. The sections of the specification and the figures are functionally grouped together. For example, the section entitled Address Generators (Spec. at 118-27) discusses the detailed schematic diagrams related to the address generator figures (Figs. 6O-6R and Spec. at 6:7-13). The

---

[4] Fig. 2 is intermediate between the block diagram of an address generator 115B and a memory 115C in Fig. 1 and the detailed schematics of an address generator in Figs. 6O-6R and a memory in Figs. 6B-6N.

specification is outlined with the Table of Contents[5] which is attached hereto as Exhibit-1.

The level of detail is illustrated by the disclosure of an experimental system that was actually reduced to practice (e.g., Spec. at 84-236 and Figs. 6A-6AH); including highly detailed schematic diagrams down to the individual component and individual wire level of detail (e.g., Figs 6B-6D), detailed descriptions thereof down to the individual component and individual wire level of detail (e.g., Spec. at 84-236), cable wire lists (e.g., Spec. at 173-76 and 180-91), integrated circuit component (DIP) location on circuit boards (e.g., Spec. at 192- 211), and actual Basic[6] program listings with instructions and detailed annotations (e.g., Spec. at 214-36).

Representative antecedent basis limitations is discussed in Section 8.1.5 and summarized in Table-1 therein. The Table of Contents (Exhibit-1) provides a top-down road map (an indented outline) disclosure. Top-tier sections include:

GRAPHICS PROCESSOR[7]

SPATIAL FILTERING

MEMORY ARCHITECTURE

---

[5] The Table of Contents (without page numbers) was added to the specification by amendment in the Preliminary Amendment. A copy of the Table of Contents with page numbers, which was originally filed in ancestor application Serial No. 06/662,211 as Exhibit-A, was filed again in the instant application as Exhibit-A, to the Supplemental Amendment dated April 14, 1997.

[6] "Basic" is a higher level computer language, available in both a compiler and an interpreter.

[7] This is the first indented tier in the Table of Contents.

BUFFER MEMORY

EXPERIMENTAL SYSTEM

middle-tier sections for the top-tier EXPERIMENTAL SYSTEM section include:

EXPERIMENTAL SYSTEM ARCHITECTURE[8]

LOGIC BOARD

MEMORY BOARDS

BUFFER BOARD

REAR-END BOARD

CIRCUIT SPECIFICATIONS

and lower-tier sections for the middle-tier EXPERIMENTAL SYSTEM ARCHITECTURE section include:

General Description[9]

Supervisory Processor Interface

Image Loading

Software

Circuit Boards

Cable List

S-100 Bus System

Some of the contested limitations even have a whole section in the specification related thereto (Section 8.1.5).

---

[8] This is the second indented tier in the Table of Contents.

[9] This is the third indented tier in the Table of Contents.

The section entitled Brief Description of the Drawings (Spec. at 5-8) provides another type of top-down list of the disclosure. For example, Fig. 6A is identified as "a block diagram" and Fig. 6B is "a detailed schematic diagram".

In addition, extremely detailed tables of cabling and component placement (Spec. at 138-213) and computer source programs (Spec. at 214-36) are located near the back of the specification.

The experimental system is an actual reduction to practice system with many parts that operated together; including, for example, the computer, the computer programs, the computer interface, the address generators, the image memory, the buffer memory, the weight circuitry, the kernel circuitry, and the display monitor. For example, the instant application discloses a computer (e.g., Spec. at 85-89 and 237-38 and 610A in Fig. 6A) filtering an image with a disclosed filter program (e.g., Spec. at 15-24 and 23-1-36 and Fig. 7A), overlaying graphics vectors into image memory with a disclosed program (e.g., Spec. at 9-14 and 213-16), and initializing address generators and displaying an image with a disclosed program (e.g., Spec. at 214-30). The instant application also discloses an image memory (e.g., Spec. at 25-62 and 128-35, element 115C in Figs. 1 and 2, element 610D in Fig. 6A, and Figs. 6E-6N) storing the image information and being accessed by the address generators (e.g., Spec. at 118-127 and 115B in Figs. 1 and 2, Figs. 3 and 4, element 610C in Fig. 6A, and Figs. 6O-6R); a buffer memory (e.g., Spec. at 63-83 and 136-58 and element 115D in Fig. 1, element 610E in Fig 6A, and Figs. 6W-6AF, buffering the accessed image information; a weight circuit (e.g., Spec. at 15-24 and 165-170

and Figs. 5A, 5D, and 6AH) generating kernel weights (e.g., Spec. at 232), a kernel circuit (e.g., Spec. at 15-24 and 162-64 and Figs, 5A-5D and 6AG) generating a kernel of image information (e.g., Spec. at 231-36); a display interface (e.g., Spec. at 165-170 and element 520 in Fig. 5A and Figs. 6S-6T) generating display information; and a display monitor (e.g., Spec. at 165-170, element 115E in Fig. 1., output-from element 610E in Fig. 6A, and Figs. 6S-6T) displaying an image. All of these disclosures and more are compatible and are combined in the experimental system.

The experimental system further implements an input arrangement (e.g., joysticks, Spec. at 165-170, element 115A in Fig. 1, and Figs. 6U-6V).

The experimental system further implements an output arrangement (e.g., display monitor with a video interface, Spec. at 165-170, element 115E in Fig. 1, output from element 610E in Fig.6A, and Figs. 6B-6T).

The experimental system further implements a block memory with a detailed disclosure of a block having eight rows, eight columns, and 64 bytes or pixels; an accessing or reading circuit; and a writing circuit (e.g., Spec. at 25-62 and 128-35, element 115C in Figs. 1 and 2, element 610D in Fig. 6A, and Figs. 6E-6N).

The experimental system further implements memory address generators (e.g., Spec. at 118-127 and 115B in Figs. 1 and 2, Figs. 3 and 4, element 610C in Fig. 6A, and Figs. 6O-6R).

The experimental system further implements a computer or data processor with detailed disclosures of computer programs (e.g., Spec. at 9-24, 85-89, 213-38, 610A in Fig. 6A, and Fig. 7A).

The experimental system further implements a spatial processor and a filter processor (e.g., Spec. at 15-24 and 231-36 and Fig. 7A).

The experimental system further implements a graphic processor generating vector information (e.g., Spec. at 9-14 and 213-16).

The experimental system further implements a kernel circuit including a kernel memory and a kernel processor (e.g., Spec. at 15-24, 162-64, and 231-36; and Figs. 5A-5D and 6AG).

The experimental system further implements a weight arrangement (e.g., Spec. at 15-24, 165-170, and 232 and Figs. 5A, 5D, and 6AH).

VI. ISSUES

The issues presented for review are as follows.

a) Whether all claims are unpatentable under 35 USC 112 first paragraph for enablement?

b) Whether all claims are unpatentable under 35 USC 112 first paragraph for written description?

c) Whether there is obviousness-type double patenting of claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-162 and claims of each of the eight copending applications?

d) Whether there is nonobviousness-type-double patenting of claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-162 and claims of each of the eight copending applications?

e) Whether claims 22, 23, 82-84, 95, 99, 137, and 138 are unpatentable over Patent No. 4,200,867 to Hill ("Hill") under 35 USC 102 for anticipation?

g) Whether claims 19, 25, 96, 100, 101, 140, and 135 are unpatentable over Patent No. 4,200,867 to Hill ("Hill"); Patent No. 4,069,511 to Lelke ("Lelke"); and Patent No. 4,322,750 to Lord ("Lord") under 35 USC 103 for obviousness?

VII. GROUPING OF CLAIMS

The claims do not stand or fall together. This is because the claims are separately patentable and because each of the claims is separately argued (Section VIII). For example, the different limitations in each claim are separately argued (e.g., Sections 8.4.3, 8.8.2, and 8.9.3), the different combinations of limitations in each claim are separately argued (e.g., Sections 8.4.3., 8.8.2, and 8.9.3), the distinctions of each claim over the references are separately argued (e.g., Sections 8.8.2 and 8.9.3), the antecedent basis for each contested limitation regarding the '112 rejections is separately argued (e.g., Sections V, 8.1.5, and 8.2.1), and claims that do not recite the contested features are separately argued (e.g., Section 8.1.4).

The Supreme Court requires a Graham[10] analysis of each individual claim for '103 rejections and for obviousness-type double-patenting rejections related thereto (Sections 8.5 and 8.9). The Federal Circuit decisions in Nielson and Beaver[11] require that rejections address the claims individually where the Appellant has reasonably argued the claims separately. The Federal

---

[10] Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966).

[11] In re Nielson, 816 F.2d 1567, 2 USPQ2d 1525 (Fed. Cir. 1987); In re Beaver, 893 F.2d 329, 13 USPQ2d 1409 (Fed. Cir. 1989).

Circuit also requires a Gechter[12] analysis on a limitation-by- limitation basis with specific fact findings for each contested limitation, with satisfactory explanations for such findings, and with explicit claim construction (Sections 8.4.4 and 8.7.1).

In view of the above, the claims do not stand or fall together.

VIII. ARGUMENT

8.1 ARGUMENTS COMMON TO THE 35 USC 112-1 ENABLEMENT AND WRITTEN DESCRIPTION REJECTIONS

All claims stand rejected under 35 USC 112, first paragraph ("'112-1") regarding enablement and written description. The arguments common to both the enablement and the written description '112-1 rejections. are set forth in this Section 8.1. The arguments primarily related to the enablement rejection are set forth in Section 8.2 to supplement the arguments set forth in this Section 8.1. The arguments primarily related to the written description rejection are set forth in Section 8.3 to supplement the arguments set forth in this Section 8.1.

---

[12] Gechter v. Davidson, 116 F.3d 1454, 43 USPQ2d 1030 (Fed. Cir. 1997).

MPEP 706.03[13] establishes that the instant application should not have "undue emphasis" given to "technical" issues (e.g., disclosure issues). Effort should be minimized or eliminated as to technical rejections unless they are critical. Hence, the non-critical '112-1 "technical" (disclosure) rejections are clearly improper. MPEP 706.03 further requires that such '112-1 (disclosure) rejections "should be stated with a full development of the reasons rather than by a mere conclusion coupled with some stereotyped expression." In violation thereof, the rejections are based upon unsupported conclusionary statements that object to selected parts of the disclosure (Section 8.1.5), that are not related to the claimed invention (Section 8.1.4), and that ignore the disclosure as a whole (Section 8.1.3).

The '112-1 rejections do not, and in fact cannot,[14] establish a prima facie case of lack of enablement or lack of written description.

---

[13] '706.03 Rejections Not Based on Prior Art

The primary objective of the examination of an application is to determine whether or not the claims define a patentable advance over the prior art. This consideration should not be relegated to a secondary position while undue emphasis is given to nonprior art or "technical" rejections. Effort in examining should be concentrated on truly essential matters, minimizing or eliminating effort on technical rejections which are not really critical. Where a major technical rejection is proper (e.g., lack of proper disclosure . . .) such rejection should be stated with a full development of the reasons rather than by a mere conclusion coupled with some sterotyped expression.' (emphasis added).

[14] The Examiner cannot establish a prima facie case of lack of enablement or lack of written description because the claims find ample antecedent basis in the extensive and detailed disclosure.

The Appellant respectfully traverses the 35 USC 112-1 rejections for the reasons discussed in Sections 8.1.1 et seq, 8.2, and 8.3.

8.1.1 The Instant Disclosure Being The Same As In Ancestor Patent 5,584,032 Is Legally Correct And Presumptively Valid

The '112-1 rejections are prima facie erroneous because the disclosure is presumptively valid and correct. Since the disclosure in the instant application is the same in pertinent part as the disclosure in ancestor patent No. 5,584,032 (the '032 patent) and the disclosure of an issued patent is already established as being legally correct and presumptively valid, the disclosure in the instant application must also be presumed to be correct. Nevertheless, the Examiner did not consider the presumptive validity of the disclosure in the ancestor '032 patent, just as he did not consider the extensive disclosure in the instant application. Hence, the '112-1 rejections should be reversed.

Notwithstanding the above, MPEP 2164.04 states that an applicant's disclosure is presumptively correct and that an examiner is required to provide sufficient objective reasons to challenge this presumption. However, in the instant application, the Examiner has not provided the required objective reasons to overcome the presumption of correctness. This is not surprising since the instant disclosure is extensive and certainly sufficient (Sections V, 8.1.5, 8.1.7, 8.2.1, and 8.2.2). Hence, the '112-1 rejections should be reversed.

Court decisions confirm this presumption—that the disclosure is presumed to be correct and that the Exam-

iner is required to provide acceptable evidence or reasoning regarding any challenge to the disclosure.

> As a matter of Patent Office practice then, a specification disclosure which contains a teaching of the manner and process of making and using the invention in terms which correspond in scope to those used in describing and defining the subject matter sought to be patented must be taken as in compliance with the enabling requirement of the first paragraph of Section 112 unless there is reason to doubt the objective truth of the statements contained therein which must be relied on for enabling support . . . .
>
> In any event, it is incumbent upon the Patent Office, whenever a rejection on this basis is made, to explain why it doubts the truth or accuracy of any statement in a supporting disclosure and to back up assertions of its own with acceptable evidence or reasoning which is inconsistent with the contested statement. Otherwise, there would be no need for the applicant to go to the trouble and expense of supporting his presumptively accurate disclosure.

Marzocchi.[15]

> There is no requirement in 35 USC 112 or anywhere else in the patent law that a specification convince persons skilled in the art that the assertions in the specification are correct.
>
> In examining a patent application, the PTO is required to assume that the specification complies with the enablement provision of Section 112 unless it has

---

[15] In re Marzocchi, 439 F.2d 220, 223-24, 169 USPQ 367, 369-70 (CCPA 1967). (emphasis added).

> 'acceptable evidence or reasoning' to suggest otherwise . . . . The PTO thus must provide reasons supported by the record as a whole why the specification is not enabling . . . . Then and only then does the burden shift to the applicant to show that one of ordinary skill in the art could have practiced the claimed invention without undue experimentation.

Gould.[16] The failure of the Examiner to provide any objective reasons is not surprising since the instant application has extensive relevant disclosure and the Examiner would not have been to support the '112-1 rejections. Hence, the '112-1 rejections should be reversed.

In view of the above, the disclosure is presumptively and legally correct. Hence, the '112 rejections should be reversed.

8.1.2 The Examiner Expressly Admits That The Instant Disclosure Is Adequate

The Examiner expressly admits in the Final Action that the disclosure is adequate:

> "The subject matter claimed in the instant application is fully disclosed in the referenced copending application . . . . "

(pages 26-27) (emphasis added). Because the instant disclosure is the same in pertinent part as the disclosures in "the referenced copending applications", this admission by the Examiner that "[t]he subject matter claimed in the instant application is fully disclosed" ap-

---

[16] Gould v. Mossinghoff, 229 U.S.P.Q. 1, 13-14 (D.D.C. 1985), aff'd in part, vacated in part, and remanded sub nom. See also Gould v. Quigg, 822 F.2d 1074, 3 U.S.P.Q.2d 1302 (Fed. Cir. 1987).

plies equally to the instant application. This admission alone is sufficient to merit reversing the '112-1 rejections.

In view of the above, the Examiner admits that the disclosure is adequate. Hence, the '112-1 rejections should be reversed.

8.1.3 The '112-1 Rejections Fail To Consider The Disclosure As A Whole

The instant disclosure is significant (e.g., Sections V, 8.2.1, and 8.2.2), comprising over 200 hundred pages of description with detailed schematic diagrams showing actual commercially available electrical components in well known schematic symbol form and even showing component pin designations and wire connections (Sections 6.2.1 and 8.2.2). However, the Examiner has not considered the disclosure as a whole as required by the Appeals Court.[17] For example, the subject terminology (Table-1) finds extensive basis in the disclosure (e.g., Sections V, 8.2.1, and 8.2.2). Nevertheless, despite the large number of occurrences of the subject terminology in the specification (Table-1), the Examiner has never acknowledged any basis at all in the disclosure and has not even attempted to reconcile the '112-1 rejections in view of the large number of recitations of the subject terminology in the specification (Table-1). Hence, the Examiner has not considered the disclosure as a whole nor established a prima facie case.

The '112-1 rejections are based upon subject matter that is adequately disclosed but ignored (Sections 8.1.3, 8.1.5, 8.2.1, and 8.2.2). The Examiner does not cite any

---

[17] In re Moore, 439 F.2d 1232, 169 USPQ 236 (CCPA 1971); In re Hogan, 559 F.2d 595, 194 USPQ 527 (CCPA 1977).

law to support this novel position. Taken to its limit, such a rejection would render all claims unpatentable (e.g., claims enabled by adequately disclosing the claimed subject matter would be rendered unpatentable by an examiner refusing to consider the relevant disclosure). This is similar to what has occurred in the instant application, as discussed below.

Instead of considering the disclosure as a whole, the Examiner improperly criticizes brief excerpts from the claims (Table-1) for being inadequate while disregarding the extensive detailed disclosure related thereto. It is improper for the Examiner to object to brief excerpts from the claims as not being enabling and to ignore the detailed disclosures related thereto. If the Examiner had considered the disclosure as a whole, he would have found extensive relevant disclosure (e.g., Table-1) and would have had to withdraw the '112-1 rejections.

In view of the above, the disclosure is extensive and, when considered as a whole, is certainly sufficient. Hence, the '112-1 rejections should be reversed.

8.1.4 The '112-1 Rejections Are Erroneously Based Upon Unclaimed Subject Matter

Various claims stand rejected under '112-1 based upon unclaimed subject matter. However, the Examiner does not cite any law to support this novel position. Taken to its limit, such a doctrine poses a "catch 22" situation that would render all applications unpatentable (e.g., an application disclosing and claiming an electronic device would be unpatentable for insufficient disclosure of an unclaimed nuclear reactor). Notwithstanding the fact that it is not necessary to provide antecedent basis for unclaimed subject matter, the unclaimed subject

matter objected to by the Examiner is in fact adequately enabled (Sections 8.1.4 and 8.1.5 and Table-1).

The law is well-established, that disclosure of unclaimed subject matter is irrelevant to rejections.

OPINION * * *

> Nor will we sustain the rejection of selected claims 1, 4, 5, 7, 11 through 13, 16, 24 and 29 under 35 U.S.C. 112 as being based upon an insufficient disclosure . . . . And second, we agree with the appellant that the examiner's criticisms of the disclosure of the present application at pages 2-5 of the answer are irrelevant because they do not pertain to claimed subject matter. Cf. In re Brown, 477 F.2d 946, 177 USPQ 691 (CCPA 1973); In re Ghiron, 442 F.2d 985, 169 USPQ 723 (CCPA 1971). * * *
>
> Accordingly, all grounds of rejection advanced by the examiner are reversed.

Hyatt-'277[18]. See also Uniroyal.[19] Hence, rejections under '112-1 must be evaluated based upon the claimed invention. Matter that is not claimed is not relevant to a 112-1 rejection. It is for the invention as claimed that enablement and written description must exist, and not

---

[18] Ex parte Hyatt, Appeal No. 88-0854, Paper No. 24 at 3-5 in patent application Serial No. 06/520,277 which issued as U.S. Patent No. 4,910,706 on March 20, 1990 (Bd. Pat. App. & Int. April 14, 1989) (herein Hyatt-'277] (unpublished PTO decision). (footnote omitted).

[19] Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1998), cert. denied, 488 U.S. 825 (1988).

some other.[20] Since the instant '112-1 rejections include objections to subject matter that is not claimed, the '112-1 rejections thereof should be reversed.

In view of the above, the '112-1 rejections rely on unclaimed subject matter. Hence, the '112-1 rejections should be reversed.

8.1.5 The Examiner Alleges Insufficient Disclosure While Ignoring Hundreds Of Relevant Recitations In The Disclosure

The Examiner erroneously bases the '112-1 rejections on a position that the subject terminology has no basis in the disclosure. However, this terminology has extensive basis in the disclosure. Remarkably, the extensive basis for the terminology has been ignored by the Examiner. The Examiner cannot possibly establish a prima facie case for the '112-1 rejections until he evaluates the numerous occurrences of this terminology. The quantities of such occurrences of representative terminology and representative antecedent basis are listed in Table-1.[21]

---

[20] In re Wright, 999 F.2d 1557, 27 USPQ2d 1510 (Fed. Cir. 1993); Christianson v. Colt Indus.Corp., 822 F.2d 1544, 3 USPQ2d 1241 (Fed. Cir. 1987), vacated on jurisdictional grounds and remanded, 486 U.S. 800, 7 USPQ2d 1109 (1988).

[21] Terminology that is objected to by the Examiner is listed in alphabetical order in the "TERMINOLOGY" column in Table-1. The number of occurrences in the specification for the term is identified in the "OCCURRENCES" column in Table-1. The symbol ">" means "greater than". For example "memory" terminology is listed as ">400", which means that it has more than 400 occurrences in the disclosure. Representative examples of the pages and figures that provide basis for the term in the disclosure are listed in the "REPRESENTATIVE PAGE(S)" column and the "REPRESENTATIVE FIGURE(S)" column in Table-1, respectively.

The experimental system embodiment described in the specification and shown in the figures represents a detailed disclosure of an actual reduced to practice system. Hence, the subject terminology that is described (Table-1) is also fully enabled by the disclosure. Further, features which operate together in the experimental system are certainly disclosed as being coupled together in the claimed combinations. Still further, the Basic computer programs have Basic computer statements that operate together in the programs and that operate with the computer and the disclosed circuitry and hence are certainly disclosed as being coupled together in the claimed combinations.

The Examiner has not indicated how many occurrences of a term he requires before the term is considered to be adequately disclosed. However, the law of the Federal Circuit does not even require a single verbatim recitation or literal recitation in order to satisfy '112-1 (Section 8.3.1). Hence, the numerous verbatim recitations and literal recitations are certainly adequate.

The experimental system was developed as an operating demonstration system. The interconnections disclosed in the experimental system establish coupling and responsiveness as recited in the claims. See, for example, the discussion of interconnection between integrated circuit components in Sections 8.2.1 and 8.2.2. Also, the Basic program listings disclosed for the experimental system further establish coupling and responsiveness as recited in the claims.

The Table of Contents illustrates the extensive disclosure. For example, the section entitled "EXPERIMENTAL SYSTEM" (Spec. at 84 et seq.) is followed by a list of 20 sub-sections of description and tables disclos-

ing an experimental system that was actually reduced to practice in over 100 pages of specification illustrated with Figs. 6A to 6AH and 7A.

The application discloses the experimental system in great detail. With the extensive memory disclosure (e.g., Spec. at 99-135) and processor disclosure (e.g., Spec. at 87-98, 214-36) in the instant application, it is unbelievable that the Examiner would object to the disclosure of memory and processor features. Clearly, the Examiner did not consider the disclosure as a whole as required by the Federal Circuit.

In view of this extensive antecedent basis for the subject terminology, the Examiner's position that there are no such recitations nor that there is a lack of written description or slack of enablement is clearly erroneous.

TABLE-1

REPRESENTATIVE TERMINOLOGY	NOTES [22]	OCCURRENCES	REPRESENTATIVE CITES PAGE(S)
access	A	>100	25-83, 128-164
address	A	>500	25-83, 128-164
block	A	>80	25-83, 128-164
boundary		=3	14, 41
compress		=4	23
data compressed		=1	23
decompressed		=1	23
frequency (FFT)	C	=7	33-34
graphic	D	>20	9-14, 214-230
image		>50	50-55
information		>100	THROUGHOUT

[22] Each note is discussed below.

input		>200	THROUGHOUT
memory	A	>400	25-83, 128-164
pixel		>300	THROUGHOUT
processor		>50	85-98
quantization	E	>100	231-236
read	A	>50	25-83, 128-164
simultaneous		>8	36, 45, 46, 50
smoothing		=1	232
spatial	B	>20	15-24, 231-236
vector	D	>50	9-14, 214-230
video		=8	77, 166, 168-171
weight	F	>100	162-164
write	A	>100	25-83, 128-164

In addition to the features which are objected to by the Examiner that have hundreds of relevant recitations in the disclosure (Table-1), various features objected to under '112-1 have whole sections directed thereto in the disclosure. However, the Examiner did not properly address these sections. See the Table-1 notes discussed below. These sections are clearly identified in the Table of Contents (Exhibit-1). Hence, it is apparent that the Examiner did not consider the disclosure as a whole (even with the Table of Contents at his disposal) and that the Examiner did not establish a prima facie case. See, for example, the discussion of the notes following Table-1 below.

NOTE-A: Memory terminology; including memory access, memory read, memory write, and memory block terminology; is disclosed, for example, in two whole sections entitled "MEMORY ARCHITECTURE" and "MEMORY BOARDS" (Spec. at 25-62 and 128-35 and Figs. 6E-6N) and in two additional whole sections enti-

tled "BUFFER MEMORY" and "BUFFER BOARD" (Spec. at 63-83 and 136-58 and Figs. 6W-6AF).

NOTE-B: Filter terminology and spatial terminology is disclosed, for example, in a whole section entitled "SPATIAL FILTERING" (Spec. at 15-24), in a computer program entitled "FTR.ASC" (Spec. at 231-36), and in Figs. 5A-5D and 7A directed thereto.

NOTE-C: An FFT (Spec. at 33-34) is a well known frequency domain transform.[23] The term "frequency-domain" is described in Appellant's prior Patent No. 4,209,843.[24]

NOTE-D: Graphics terminology as disclosed, for example, in a whole section entitled "GRAPHICS PROCESSOR" (Spec. at 9-14) and in computer programs entitled "GRAPH.ASC" and "LD.ASC" (Spec. at 214-30).

---

[23] "2. Description of the Prior Art

The prior art provides digital filtering arrangements with whole number digital data processors which require complex computational hardware to implement whole-number computations. Prior art correlators are implemented as frequency-domain correlators by first performing a Fast Fourier Transform (FFT) to convert time-domain input information to frequency-domain information, then by performing a correlation operation in the frequency-domain, and then by performing an inverse FFT for converting the frequency-domain correlated information to time-domain information for interpretation by an operator. The large quantity of whole-number computational operations such as multiplication operations for an FFT computation, complex hardware, and extensive computations result in expensive correlation processors which are not able to operate in real-time." Hyatt Patent No. 4,209,843 at col. 1.

[24] Patent No. 4,209,843 issued on June 24, 1980; which is prior to the October 1984 filing dates of ancestor applications Serial No. 06/661,649 and Serial No. 06/662,211.

NOTE-E: The Basic computer programs (Spec. at 214-36) use, for example, the "%" integer declaration character, the "FIX" truncated integer arithmetic function, and the "INT" integer arithmetic function. These Basic computer instructions round, truncate, and otherwise quantize the operands. (See Exhibit-4). The "%""declaration character occurs more than 100 times, the "FIX" arithmetic" function occurs more than 10 times in the Basic computer programs, and the "INT" arithmetic function occurs more than 100 times in the Basic computer programs (Spec. at 214-36).

NOTE-F: Weight terminology is disclosed, for example, in a whole section entitled "Weight Logic" (Spec. at 162-64 and Fig. 6AH) directed thereto, in the filter computer program section entitled "Description of Fig 7A and the FTR.ASC Listing" (Spec. at 18-22), and in the filter computer program entitled "FTR.ASC" (Spec. at 231-36 and Fig. 7A).

The Examiner criticizes selected excerpts from the claims as being inadequately disclosed. However, the Examiner ignores the extensive details provided in the disclosure. Criticizing selected excerpts from the claims while ignoring the extensive details provided in the disclosure in support thereof is improper. Because the Examiner has ignored the relevant parts of the disclosure, the '112-1 rejections do not establish a prima facie case and hence are fatally defective.

The Examiner discusses the disclosure of weighting including identifying several disclosed integrated circuit components (Final Action at 16-18), thus illustrating the very detailed nature of the disclosure. However, the Examiner questions the showing of weight addresses applied to the RAMs. The Examiner is referred to Fig.

6AH where weight read addresses are loaded into U22A and U22B registers to access the weight RAMs U21E, U22E, and U23E and where weight write addresses are multiplexed with multiplexer circuits U22C and U22D to write into the weight RAMS U21E, U22E, and U23E. See the address pins AO-A9 on each of the RAM components coupled to the multiplexer circuits U22C and U22D. See also the specification at 162-64 entitled "Weight Logic".

In view of the above, the disclosure has numerous recitations that establish written description and the disclosure has extensive details of an experimental system that establishes enablement. Hence, the '112 rejections should be reversed.

8.1.6 The '112-1 Rejections Regarding Product Terminology Are Improper In Light Of The Statute And The Law Of The Federal Circuit

The '112-1 rejections of process claims for reciting "making a product" terminology are improper because "making a product" terminology is statutory language and is explicitly permitted by PTO Examination Guidelines. Furthermore, the '112-1 rejections of such process claims are in violation of the law of the Federal Circuit. Finally, notwithstanding the legal impropriety of the '112-1 rejection of product terminology, the disclosure provides extensive support for "product" terminology (Section 8.1.7).

The '112-1 rejections are in conflict with the statutory language of 35 USC 271(g). This statute expressly provides for protection of a "product" made by a claimed process. The process claims at issue recite the act of

making such a "product" in full compliance with the statute.

The law in 35 USC 271(g) also protects "products" made with the claimed process even without the process reciting "product" terminology. Hence, it goes against the intent of the statute to reject claims under 35 USC 112 for expressly reciting such statutory "product" terminology.

Furthermore, because the "product" terminology is statutory language (35 USC 271(g)), it is improper to require the disclosure to recite this "product" terminology verbatim. Generally, statutory language is above challenge by the PTO.

In addition to being improper because of 35 USC 271(g), the '112 rejections are also contradicted by the PTO Examination Guidelines regarding "product" terminology.

> "Products may be either machines, manufactures or compositions of matter.
>
> A machine is:
>
> a concrete thing, consisting of parts or of certain devices and combinations of devices. Burr v. Duryee, 68 US (1 Wall.) 531, 570 (1863).
>
> A manufacture is:
>
> the production of articles for use from raw or prepared materials by giving to these material new forms, qualities, properties or combinations, whether by hand-labor or by machinery.

> Diamond v. Chakrabarty, 447 US at 308, 206 USPQ at 196-197 (quoting American Fruit Growers, Inc. v. Brogdex Co., 283 US 1, 1 (1931)."

Examination Guidelines.[25] See also Harmon[26]:

> The eligible products identified in paragraph 101 are machines, manufactures, and compositions of matter.

Clearly, the disclosed apparatuses (e.g., circuits) constitute "machines" and "manufactures" and hence "products". Also, the disclosed signals constitute "manufactures" (and hence "products") because the signals are physical things[27] that are made, for example, by the disclosed circuits.

Because statutory categories of patentable subject matter include both processes and products and since products include machines, manufactures, and compositions of matter; there can be no question that claims directed to the acts of a process and further directed to the act of making a product fully comply with 35 USC 112. Hence, the disclosed apparatuses (e.g., circuits and devices) and the disclosed signals, for example, all constitute products.

---

[25] Examination Guidelines For Computer-Related Inventions, 1184 OG 87 at 96, FN 35.

[26] Robert L. Harmon, Patents and the Federal Circuit at 27, Second Edition, BNA (1991) (emphasis added).

[27] Signals are "necessarily physical." Arrhythmia Research Technology Inc. Corazonix Corp., 22 USPQ2d 1033, 1038 (Fed. Cir. 1992). See also In re Taner et al., 214 USPQ 678, (CCPA 1982); In re Sherwood, 613 F.2d 809, 204 USPQ 537, 545 FN 8 (CCPA 1980); and In re Johnson, 589 F.2d 1070, 200 USPQ 199 (CCPA 1978).

The '112 rejections regarding "product" terminology are in conflict with the law of the CCPA and thus the '112 rejections are in conflict with the law of the Federal Circuit.[28]

The CCPA in Best[29] established that an invention can be claimed both with a "process" claim and with a "product" claim. Similarly, in the instant application, it is clearly permitted to claim both the process and the further act of making a product in response to or as a step in the process. Hence, it is permissible to recite together both a process claim and a process claim which comprises the further act of making a product even when both recite similar characteristics of the product.

Notwithstanding the fact that the '112-1 rejections regarding "making a product" violate the law of the Federal Circuit and the rules of the PTO, this issue has already been resolved for the instant application. However, the Examiner has overlooked this resolution. In particular, (a) claims reciting "making a product" have already been issued in ancestor patent No. 5,584,032[30] (the '032 patent); (b) the disclosure in the instant appli-

---

[28] The Federal Circuit has adopted the law of the CCPA. See South Corp. v. United States, 690 F.2d 1368, 215 USPQ 657 (Fed. Cir. 1982). Because the CCPA always sat in banc, its decisions will not be overturned by a panel decision of the Federal Circuit. Rather, CCPA decisions can be overturned only by an in banc decision of the Federal Circuit.

[29] In re Best, Bolton, and Shaw, 562 F.2d 1252, 195 USPQ 430 (CCPA 1977).

[30] See "making a product" claim terminology in claims 32, 34, 40, and 42 of ancestor patent No. 5,584,032. See also "making a product" claim terminology in claims 38, 40, 42, 44, 46, 48, 50, 52, 54., 56, 58, 60, 62, and 64 of Hyatt patent No. 5,615,142.

cation is the same in pertinent part as the disclosure in the '032 patent; and (c) the claims in the '032 patent have a presumption of correctness because it is an issued patent. Hence, there is a presumption that the instant disclosure satisfies '112-1 regarding "making a product" claim terminology. The Examiner has not even attempted to explain the basis of the objection to "making a product" terminology. Hence, the '112-1 rejections regarding "making a product" claim terminology should be reversed.

In view of the above, the product terminology in the claims is consistent with the statutes, case law, and PTO guidelines. Hence, the '112-1 rejections regarding product terminology should be reversed.

8.1.7 The Product Terminology Objected To Based On '112-1Has Ample Antecedent Basis In The Instant Disclosure

Notwithstanding the impropriety of the '112-1 rejections regarding the "product" terminology (Section 8.1.6), the instant disclosure recites ample product related terminology. Terms related to implement, manufacture, construct, configure, insert, interconnect, plug-in, and practice are recited in the disclosure, as discussed below. Further, terms related to displays, signals, information, etc. are also recited in the disclosure.

The term "implement" and terms related thereto are used more than 100 times in the disclosure.

Various commercial products are cited in the disclosure (Section 8.2.2) and are identified as being "manufactured" or terminology related thereto. (See, e.g., Spec. at 17, 92, 93, 95, 96, 168, and 169).

Representative excerpts from the disclosure are quoted below.

> An experimental system has been constructed to demonstrate operation of the graphics display capability.

(Spec. at 10:18-19) (emphasis added).

> The experimental configuration has been constructed having a 512-pixel by 512-pixel memory map. For convenience of experimentation, static 16K-RAM chips are used for memory map implementation. Typical circuits are the TMS-4016 RAM from Texas Instruments Inc. and the M58725P static RAM from Mitsubishi Electric. These circuits are configured in the form of a 2K-word by 8-bit static RAM having an 11-bit address, a tristate chip select, and a tristate output enable. Conventionally, the chip select and output enable are used to provide output bussing and to reduce the need for an output register. In the present configuration, the chip select and output enable signals are used to provide 2-additional dimensions of memory addressing.

(Spec. at 46:13-24). (emphasis added).

> Each board is constructed with a Vector board, manufactured by Vector Electronic Company of Sylmar CA, having 1/10th inch hole spacings on a 17-inch by 8 1/2-inch board. Wire wrap DIP sockets and cable connectors are inserted into the Vector board and interconnected with wire wrap Interconnections. Information on the DIPs plugged-in to the DIP sockets is provided for selected boards in the printout of the table of dip layout on boards included herewith. Information on the cable connectors is provided for

each cable in the printout of the cable connection table included herewith.

(Spec. at 92:5-1.4) (emphasis added).

A discussion will now be provided relative to Figs 6G to 6N to illustrate the logical design of the memory. Figs 6G to 6K each show 16-RAMs organized in 2-logical columns and constructed on one row on a memory board, where each memory board has 4-groups of 16-RAMs each shown in one of Figs 6G to 6J.

(Spec. at 130:21-25) (emphasis added).

In view of the above, the disclosure has numerous recitations of product-related terminology that establishes written description for products and the disclosure has extensive details that constitutes enablement of products. Hence, the '112 rejections regarding product terminology should be reversed.

8.1.8 The '112-1 Rejections Do Not Establish A Prima Facie Case

The 35 USC 112-1 rejections do not establish a prima facie case[31], as discussed below.

a. The most relevant parts of the disclosure are ignored (e.g., Sections V, 8.1.5, 8.2.1, and 8.2.2).

b. The rejections improperly group claims together and reject them together in groups.

---

[31] See 37 CFR 1.106(b); Chester v. Miller, 906 F.2d 1574, 1578, 15 USPQ2d 1333, 1337 (Fed. Cir. 1990) ("Section 132 is violated when a rejection is so uninformative that it prevents the applicant from recognizing and seeking to counter the grounds for rejection."). See also In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992).

c. The rejections do not provide the required "acceptable evidence or reasoning" (Section 8.1.1).

d. The Examiner even admits in the Final Action that the instant application fully discloses the claimed subject matter (Section 8.1.2).

e. The rejections fail to consider the disclosure as a whole (Section 8.1.3).

f. The rejections fail to consider the skill in the art (Section 8.2.3).

g. The rejections are improperly based upon unclaimed subject matter (Section 8.1.4).

h. The rejections merely identify claim terminology (Table-1) without any support (Section 8.1.5).

i. The Appellant properly traversed the Examiner's unsupported statements, but the Examiner did not provide the required reference or affidavit in accordance with MPEP 2144.03.

j. The rejections are grossly inconsistent (Section 8.10), alleging complete lack of disclosure in support of '112-1 rejections and then alleging full disclosure in support of the double patenting rejections.

The burden of establishing a prima facie case rests with the examiner and is not satisfied by a mere list of terminology (Table-1).[32]

---

[32] In re Edwards, 568 F.2d 1349, 1354, 196 USPQ 465, 469 (CCPA 1978); In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992).

Judge Lindquist in Hyatt '444[33], in reversing the rejection under '112-1, stated:

OPINION

35 U.S.C. 112 Rejection

> With respect to the rejection under the first paragraph of section 112, it is clear that the examiner is concerned with the enablement (make and use) requirement. We are not convinced, however, that the examiner has discharged his initial burden of establishing that the disclosure does not describe the claimed invention sufficiently to enable the artisan to practice it without undue experimentation. Cf. In re Strahilevitz, 668 F.2d 1229, 212 USPQ 561 (CCPA 1982); In re Ancistadt, 537 F.2d 498, 190 USPQ 214 (CCPA 1976); In re Armbruster, 512 F.2d 676, 185 USPQ 152 (CCPA 1975) . . . . According, the examiner did not have a reasonable basis for questioning the sufficiency of the disclosure.

The Examiner completely ignores the most relevant parts of the disclosure (e.g., Sections V, 8.1.5, 8.2.1, and 8.2.2) and simply contends that the disclosure does not provide any written description or enablement of the subject terminology (Table-1). The rejection does not acknowledge any of the extensive verbatim and literal basis in the disclosure (e.g., Sections V, 8.1.5, and 8.2.1).

The claims are all rejected together as groups of claims. This is improper. In order to establish a prima facie case, each claim must be evaluated individually to

---

[33] Ex parte Hyatt, Appeal No. 636-62, Paper No. 48 at 3-4 in patent application Serial No. 07/874,444 (Bd. Pat. App. & Int. October 30, 1986) [herein Hyatt-'444] (unpublished PTO decision).

determine whether the individual claim meets the '112-1 requirement. Since the Examiner did not evaluate the claims individually, the rejection is improper for failing to establish a prima facie case. See Van Geuns, and Wright.[34] See also Nielson and Beaver.[35]

The Examiner must support disclosure rejections with a proper explanation of why the disclosure is not adequate and must provide "acceptable evidence or reasoning" to support a finding of lack of adequate disclosure (Section 8.1.1). See also Piasecki.[36] However, the '112-1 rejections do not provide a proper explanation or "acceptable evidence or reasoning" regarding the adequacy of the instant disclosure.

The Appellant developed his position with reasoning and evidence and traversed the Examiner's unsupported statements even though the Examiner did not provide a reference or affidavit in support of his position in violation of MPEP 2144.03. Further, the Examiner's unsupported statements are "in areas of esoteric technology" and hence should have been supported by a citation of a reference (MPEP 2144.03), but were not thusly supported.

---

[34] In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993); In re Wright, 999 F.2d 1557, 27 USPQ2d 1510 (Fed. Cir. 1993).

[35] In re Nielson, 816 F.2d 1567, 2 USPQ2d 1525 (Fed. Cir. 1987); In re Beaver, 893 F.2d 329, 13 USPQ2d 1409 (Fed. Cir. 1989).

[36] In re Piasecki, 745 F.2d 1468, 223 USPQ 785 (Fed. Cir. 1984).

It is the content and not the form or style of the disclosure that is important. See Sherwood.[37] Just because the disclosure was drafted by a pro se applicant (who is a self-taught patent agent) and thus may not follow as formal a style as the Examiner might desire, this does not in itself provide a basis for a 35 USC 112-1 rejection.

It is improper to reject a claim for lack of written description or enablement over terminology that is not recited in the particular claim. However, the Examiner in fact rejected claims over terminology that is not recited in the particular claim.

In view of the above, the '112-1 rejections do not establish a prima facie case. Hence, the '112-1 rejections should be reversed.[38]

8.1.9 Conclusion[39]

The 35 USC 112-1 rejections should be reversed for the reasons set forth above; the instant disclosure being the same as in ancestor patent 5,584,032 is legally correct and presumptively valid; the Examiner expressly admits that the instant disclosure is adequate; the '112-1 rejections fail to consider the disclosure as a whole; the '112 rejections are erroneously based upon unclaimed subject matter; the Examiner alleges insufficient disclosure while ignoring hundreds of relevant recitations in the disclosure; the product terminology has ample basis; there is antecedent basis for product terminology; and

---

[37] In re Sherwood, 613 F.2d 809, 816, 204 USPQ 537, 545 FN 8 (CCPA 1980) cert. denied, 450 U.S. 994 (1981).

[38] In re Oetiker, 977 F.2d 1443, 24 U.S.P.Q.2d 1443 (Fed. Cir. 1992).

[39] The "Conclusion" section headings appearing in this Appeal Brief are not listed in this Appeal Brief's Table of Contents.

the 35 USC 112-1 rejections do not establish a prima facie case.

8.2 35 USC 112-1 ENABLEMENT REJECTION

All claims stand rejected under 35 USC 112-1 for lack of enablement. The Appellant respectfully traverses the 35 USC 112-1 enablement rejection for the reasons discussed in Sections 8.1 and 8.2.1 et seq.

8.2.1 The Disclosure is Enabling, Having Schematic Details Down To The Component Level

The disclosure is enabling, including extensive design details. For example, actual "off the shelf" electrical components are shown interconnected in detailed schematic diagrams. The specification has extensive discussions of the schematic components, interconnections, and signals. The disclosure even provides well known component schematic symbols with pin[40] designations and with many individual wire connections between circuit components (e.g., Figs. 613-6D). For example, the Schottky TTL Data book is expressly incorporated by reference into the instant disclosure and many of the integrated circuit (IC) components that are shown in the schematic diagrams (e.g., Figs. 6B-6D) and discussed in the specification (e.g., Spec. at 99 et seq) are specified therein.

Many individual wire connections are shown connected to the logic gate, inverter, and flip-flop components. For example, near the lower right hand part of

---

[40] Electronic components are usually interconnected with discrete wires or printed wires between pins (terminals) on the components. The pins on integrated circuit components are often assigned schematic notations. These same schematic pin notations' are shown with the integrated circuit components, for example, in Figs. 6B-6AH.

Fig. 6B; a wire CXRM is shown connected from output pin-3 of OR-gate U18C (schematically referred to as signal U18C-3) and is shown connected to input pin-1 of inverter U8A (schematically referred to as signal U8A-1). The Specification includes extensive detailed discussions of the circuitry and the interconnection thereof, as illustrated with the following representative quotation regarding Fig. 6B.[41]

> R-register gating logic will now be discussed with reference to Fig 6B.
>
> Gate U19C-1[42] steers the load strobe U22B-3 to clock the register with the computer generated strobe to load the computer generated parameter into the related register. Steering signal U19C-3 steers the computer pulse U19C-2 to the input of gate U18C-1. Gate U18C-3 combines the two mutually exclusive clock signals, the computer strobe and the line sync strobe to clock the XR-register CXRM with signal U18C-3 for the computer strobe and on the rising edge of the line sync pulse.
>
> Gate U19C-10 steers the load strobe U22B-3 to clock the register with the computer generated

---

[41] The circuits, signals, and interconnections quoted below are labeled consistent with the circuits, signals, and interconnections shown in Fig. 6B. This quoted material can be better understood if reference is made to Fig. 6B.

[42] "U19C-1", for example, means the signal or connection at pin 1 of circuit "U19C". Fig. 6B at the middle right side shows U19C-1 as being the output pin "1" of the circuit "U19C", which is labeled as an LS02 (74LS02) type integrated circuit. A 74LS02 integrated circuit is identified as a NOR circuit in the referenced integrated circuit data books and U19C in Fig. 6B is shown with a well known NOR gate symbol.

> strobe to load the computer generated parameter into the related register. Steering signal U19C-9 steers the computer pulse U19C-8 to the input of gate U18C-9. Gate U18C-8 combines the two mutually exclusive clock signals, the computer strobe and the line sync strobe to clock the XR-register CXRL with signal U18C-8 for the computer strobe and on the rising edge of the line sync pulse.
>
> Gate U19D-1 steers the load strobe U22B-3 to clock the register with the computer generated strobe to load the computer generated parameter into the related register. Steering signal U19D-3 steers the computer pulse U19D-2 to the input of gate U18C-4. Gate U18C-6 combines the two mutually exclusive clock signals, the computer strobe and the line sync strobe to clock the YR-register CYRM with signal U18C-6 for the computer strobe and on the rising edge of the line sync pulse.
>
> Gate U19D-13 steers the load strobe U22B-3 to clock the register with the computer generated strobe to load the computer generated parameter into the related register. Steering signal U19D-12 steers the computer pulse U19D-11 to the input of gate U18C-12. Gate U18C-11 combines the two mutually exclusive clock signals, the computer strobe and the line sync strobe to clock the YR-register CYRL with signal U18C-11 for the computer strobe and on the rising edge of the line sync pulse.

(Spec. at 113-14) (emphasis and footnote added).

In view of the above, the application has extensive enabling disclosure. Hence, the enablement rejection should be reversed.

8.2.2 The Disclosure Makes Extensive Use Of Commercially Available Products And Integrated Circuit Components

The description and the figures include extensive disclosure of commercially available products and components, such as commercially available integrated circuit components. The disclosure provides extensive details, including schematic diagrams down to the individual component and individual wire level of detail (Sections V and 8.2.1).

The disclosure includes the widely used series 7400 line of commercially available integrated circuits. The disclosure identifies components by serial number and by schematic symbols. The disclosure expressly incorporates by reference various integrated circuit design books, including the Motorola Schottky TTL Data book.

> The circuits used in the experimental system are generally commercially available circuits and are well known . . . . For example, the 74LS00, 74ALS00, and 74AS00 specifications are set forth in the referenced Texas Instrument and Motorola catalogs . . . ; which are herein incorporated by reference. . . .
>
> 6. Motorola, Schottky TTL Databook, 1981.

(Spec. at 171). The disclosure identifies integrated circuit components by serial numbers and schematic symbols including the pin numbers for the components.

The Motorola Schottky TTL Data book is a detailed data book on integrated circuit components. "TTL" is a well known acronym for Transistor Transistor Logic. (TTL) integrated circuit components.

The Motorola Schottky TTL Data book includes extensive design detail; including schematic diagrams of the integrated circuit components, operating parameters, parametric design charts, pin designations, design details, descriptions of the circuits, and significant other design details.

The use and disclosure of commercial integrated circuits mounted and interconnected on circuit boards is clearly described in the specification, as discussed below, even to the level of cable lists, circuit placement, and software listings, as discussed below.

CIRCUIT SPECIFICATIONS

The circuits used in the experimental system are generally commercially available circuits that are well known and that are described in widely distributed specification sheets and component catalogs. A list of these specification sheets and catalogs is provided hereinafter and the materials referenced therein are incorporated herein by reference. For example, the 74LS00, 74ALS00, and 74AS00 specifications are set forth in the referenced Texas Instruments and Motorola catalogs and the Intel 8216 bus interface and the Intel 2149 RAM specifications are set forth in the referenced Intel catalogs; which are herein incorporated by reference.

1. Texas Instruments, ALS/AS Logic Circuits Data Book, 1983.

2. Texas Instruments, The TTL Data Book, Volume 3, 1984.

3. Texas Instruments, The TTL Pocket Data Book, 1983.

4. Intel, Component Data Catalog, 1981.

5. Intel, Memory Components Handbook, 1984.

6. Motorola, Schottky TTL Databook, 1981.

Various circuits used in the experimental system are described in the following list of component specifications, which are herein incorporated by reference.

1. TRW, LSI D/A Converters, TDC1016J-8/9/10.

2. TRW, Monolithic Video D/A Converters; TDC1016J-8, TDC0106J-9, TDC1016J-10; 1979

3. Texas Instruments, TMS-4016, 2048-Word By 8-Bit Static RAM.

4. National Semiconductor, ADC0800 8-Bit A/D Converter.

5. National Semiconductor, MM5321 TV Camera Sync. Generator.

6. Signetics, Hex Buffers/Inverters; 8T95, 96, 97, 98.

7. Mitsubishi; M58725P, S; P-15, S-15; 16384-BIT (2048-word by 8-bit static RAM.

(Spec. at 171-72).

Circuit Boards

The experimental system is implemented with wire wrap circuit boards consisting of 2-Memory Boards (BM1 and BM2), 1-Logic Board (BL1), 1-Buffer Board (BB1), and 1-Rear End Board (BR1). Each board is constructed with a Vector board, manufactured by Vector Electronic Company of Sylmar CA, having 1/10th inch hole spacings on a 17-inch by 8 1/2-inch board. Wire wrap DIP sockets and cable

connectors are inserted into the Vector board and interconnected with wire wrap interconnections. Information on the DIPS plugged-in to the DIP sockets is provided for selected boards in the printout of the TABLE OF DIP LAYOUT ON BOARDS included herewith. Information on the cable connectors is provided for each cable in the printout of the CABLE CONNECTION TABLE included herewith.

DIP assignments are provided for selected boards in the TABLE OF DIP LAYOUT ON BOARDS included herewith, for each board. DIPs are arranged on the boards as rows identified with alphabetical symbols; i.e., A to E; and as columns identified with numerical symbols; i.e., 1 to 23. Each DIP position on a board is identified with a symbol followed by the column and row symbols (i.e., U3A).

Logical schematic diagrams showing implementation of the experimental system are provided herewith, such as shown in Fig 6. These logical diagrams show standard commercially available integrated circuits; such as TTL series 7400 ICs, Mitsubishi M58725 RAMs, and 8216 bi-directional bus drivers, and Sygnetics 8T97 buffers. Specifications for these integrated circuits are available in catalogs and specification sheets from the abovementioned manufacturers and are well known in the art.

The schematic diagrams show the logical function in symbolic form, identify the type of IC, identify the DIP numbers and pin numbers, and show wiring interconnections between DIP and pin numbers. Device types are often shortened, such as shortening the name 74LS02 to LSQ2. DIP assignments are identified with U numbers, such as U20C represent-

> ing the DIP at row-20 column-C on the subject circuit board. For example, a NOR-gate is shown at the top portion of Fig 6B identified with the designation LSO2 as being a 74LS02 quad NOR-gate integrated circuit, identified with the designation U21C as being located on the BL1 circuit board at row-C column-21, and having 2-input signals on pin-11 and pin-12 of the DIP and-one output signal on pin-13 of the DIP. The input to pin-11 is shown connected to the output of DIP U22B pin-3, the input to-pin-12 is shown connected to the output of DIP U20B pin-12, and the output from pin-13 is shown connected to DIP U7D pin-9. For convenience of documentation, interconnections may be designated by the DIP identification number and pin number separated by a dash; i.e., U21C-13 representing pin-13 of DIP U21C. For convenience of discussion, logical circuits may be designated by the DIP identification number and the output pin number separated by a dash; i.e., U21C-13 representing pin-13 of DIP U21C.

(Spec. at 92-93).

The use and disclosure of commercial products is clearly described in the specification, the commercial design documentation is incorporated by reference into the instant disclosure, and the commercial design documentation was filed in the PTO as a disclosure document so that the public would have access to this documentation after a patent issued.

DISCLOSURE DOCUMENT

> A disclosure document has been filed in the U.S. Patent and Trademark Office on or about October 18, 1984 No. [131,747]; which is herein incorporated by

reference. This disclosure document has copies of many of the documents and specification sheets referenced herein as follows.

1. National Semiconductor specification sheet for the MM5321 synchronization generator.

2. Signetics specification sheet for the 8T95, 96, 97, 98 hex buffers/inverters.

3. National Semiconductor specification sheet for the ADC 0800 A/D converter.

4. Texas Instruments specification sheet for the TNS4016 RAM.

5. TRW specification sheet for the TDC1016J-8, TDC1016J-9, TDC1016J-10 video D/A converters.

6. Mitsubishi Electric specification sheet for the M58725P, S; P-15, S-15, RAMs.

7. Computer Compatible Joystick Instruction sheet.

8. CompuPro CPU 8085/88 Technical Manual.

9. Viewpoint/3A Plus User's Manual.

10. CompuPro RAM 17 Technical Manual.

11. CompuPro RAM 16 Technical Manual.

12. CompuPro 8080 Multi-User Monitor program listing.

13. CompuPro System Support 1 User Manual.

14. International Instrumentation Incorporated Universal Disk Enclosures manual.

15. Siemens OEM Floppy Disk Drive FDD 100-8 manual.

16. CompuPro Disk 1 User Manual.

(Spec. at 237-38). (bracketed term added).

In view of the above, the application has extensive enabling disclosure. Hence, the enablement rejection should be reversed.

8.2.3 The Enablement Rejection Improperly Ignores The Skill In The Art

The '112-1 enablement rejection improperly ignores the skill in the art. However, it is necessary for the '112-1 enablement rejection to address skill in the art notwithstanding the fact that the instant disclosure provides adequate antecedent basis to satisfy enablement for the instant claims.

The courts permit and actually prefer a disclosure to rely on what is known in the art and not to repeat that which is already known.

> If these bridge-gapping tools (the input and the output) are disclosed, there would seem to be no cogent reason to require disclosure of the menial tools known to all who practice this art.

Sherwood.[43]

> However, paragraph 112-1 does not require that the specification contain what is well known to those skilled in the art. Id.; Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co., 730 F.2d 1452, 1463, 221 U.S.P.Q. 481, 489 (Fed. Cir. 1984).

---

[43] In re Sherwood, 613 F.2d 809, 816, 204 USPQ 537, 544 FN 8 (CCPA 1980), cert. denied, 450 U.S. 994 (1981) (parenthetical expression added).

Hyatt-'253.[44]

> Obviously, it is not necessary that an applicant be more specific than is required by section 112, portion [A] [para.1]. Not every last detail is to be described, else patent specifications would turn into production specifications, which they were never intended to be. United States specifications have often been criticized as too cluttered with details to give an easy understanding of what the invention really is.

Gay.[45]

The Supreme Court established that a patent application is directed to a person skilled in the art and that knowledge which is common and well known is as if it were written out in the patent and delineated in the drawings:

> The specification . . . proceeds to describe the mechanism of the invention by a description and reference to drawings . . . all which would be incomprehensible to a person unacquainted with looms for weaving pile fabrics, but very plain to one who understood their construction and operation at the date of the patent. A person skilled in the art of constructing or using such looms . . . would readily appreciate the meaning of the terms and the character of the improvement described. . . .
>
> When an astronomer reports that a comet is to be seen with the telescope in the constellation of Auriga,

---

[44] In re Hyatt, Appeal No. 87-1597 in patent application Serial No. 05/860,253 (Fed. Cir. 1988) (herein Hyatt-'253) (unpublished decision).

[45] In re Gay, 309 F.2d 769, 774, 135 USPQ 311, 316 (CCPA 1962).

> in so many hours and minutes of right ascension, it is all Greek to the unskilled in science; but other astronomers will instantly direct their telescopes to the very point in the heavens where the stranger has made his entrance into our system. They understand the language of their brother scientist. If a mechanical engineer invents an improvement on any of the appendages of a steam engine . . . he is not obliged, in order to make himself understood, to describe the engine, nor the particular appendage to which the improvement refers, nor its mode of connection with the principle machine. These are already familiar to others skilled in that kind of machinery. He may begin at the point where his invention begins, and describe what he has made that is new, and what it replaces of the old. That which is common and well known is as if it were written out in the patent and delineated in the drawings.

Webster.[46]

The instant disclosure includes many references to and includes many incorporations by reference of prior art product information, knowledge, and documents (e.g., Spec. at 237-38). However, the rejections are silent on these prior art disclosures and on the related skill in the art.

Notwithstanding the claimed invention being fully supported by express disclosures (e.g., Sections V, 8.1.5, 8.2.1, and 8.2.2), the skill in the art established by the instant disclosure provides extensive additional and al-

---

[46] Webster Loom Co. v. Higgins, 105 U.S. 580, 585 (1881). (emphasis added)

ternative antecedent bases for enabling the instant claimed invention (Sections 8.2.2 and 8.2.3).

A proper consideration of the skill in the relevant art would establish that the technology involved in the instant claims is very well understood and highly predictable. See Stephens.[47] Because the '112-1 enablement rejection does not address the high level of skill in the art, the '112-1 enablement rejection should be reversed.

In view of the above and notwithstanding the extensive enabling disclosure in the instant application, the skill in the art provides still further basis for enablement. However, the Examiner has not provided an analysis regarding skill in the art in support of the enablement rejection because an analysis of the skill in the art would further show that the claims meet '112-1. Hence, the enablement rejection should be reversed.

8.2.4 The Enablement Rejection Does Not Establish A Prima Facie Case

The enablement rejection does not establish a prima facie case for the reasons discussed in Section 8.1.8 and for the additional reasons discussed below.

a. The rejection fails to consider that the disclosure has schematic details down to the component level (Section 8.2.1).

b. The rejection improperly ignores the skill in the art (Section 8.2.3).

c. The rejection improperly ignores the extensive use of commercially available products and inte-

---

[47] In re Stephens, 529 F.2d 1343, 188 USPQ 659 (CCPA 1976).

grated circuit components in the disclosure (Section 8.2.2).

In view of the above, the enablement rejection does not establish a prima facie case. Hence, the enablement rejection should be reversed.[48]

8.2.5 Conclusion

The 35 USC 112-1 enablement rejection should be reversed for the reasons set forth above; the disclosure is enabling, having schematic details down to the component level; the disclosure makes extensive use of commercially available products and integrated circuit components; the enablement rejection improperly ignores the skill in the art; and the enablement rejection does not establish a prima facie case; and for the additional reasons set forth in Section 8.1.9.

8.3 35 USC 112-1 WRITTEN DESCRIPTION REJECTION REGARDING A LIST OF ALLEGED CLAIM LIMITATIONS

All claims stand rejected under 35 USC 112-1 for lack of written description regarding selected terminology (Table-1)[49].

Written description requires the disclosure to reasonably convey to an artisan that the Appellant had possession of the claimed invention. See Vas-Cath and

---

[48] In re Oetiker, 977 F.2d 1443, 24 U.S.P.Q.2d 1443 (Fed. Cir. 1992).

[49] Although the subject terminology is alleged in the Final Action to be claim terminology, a comparison of the subject terminology with the actual claims in the Appendix shows significant differences between the subject terminology and the claims.

Wertheim.[50] As established in Section 8.3.1, the instant disclosure reasonably conveys possession of the claimed invention.

The Appellant respectfully traverses the 35 USC 112-1 written description rejection for the reasons discussed in Sections 8.1 and 8.3.1 et seq.

8.3.1 Claim Terminology Does Have to Be Stated Verbatim In The Disclosure To Satisfy The Written Description Requirement

The Examiner requires that the claim language have verbatim basis in the specification. However, this requirement violates the law. Notwithstanding the fact that there is significant verbatim and literal claim terminology in the specification, it is not necessary that the application recite the claim limitations exactly.

> 2163.02 Standard for Determining Compliance With the Written Description Requirement * * *
>
> The subject matter of the claim need not be described literally (i.e., using the same terms or in haec verba) in order for the disclosure to satisfy the description requirement.

MPEP 2163.02. See also Kayton[51]:

> Where the language of the claims is descriptively supported either in a drawing or, for example, as the cumulative effect of numerous specific embodiments

---

[50] Vas-Cath Inc. v. Mahurkar, 935 F.2d 1555, 19 USPQ2d 1111 (Fed. Cir. 1991); In re Wertheim, 541 F.2d 257, 265, 191 USPQ 90, 99 (CCPA 1976).

[51] Kayton, I., Patent Practice, Fifth Edition, Vol. 3, Chapter 11, page 92 (Patent Resources Institute, 1993).

described in the application, it is not necessary that the specific language used as a definition in the claim also be used in the specification as originally filed.

See also Smythe.[52]

The Examiner objects to the disclosure of strings of words allegedly recited in the claims, but the Examiner has ignored the numerous recitations in the specification regarding the subject terminology. It must therefore be concluded that the Examiner requires verbatim recitation of strings of words in exact sequence. However, this is not the law—verbatim recitation is not necessary. Hence, for these additional reasons, the unjustified requirement of verbatim recitation of the alleged claim limitations and the ignoring of many relevant recitations in the disclosure, the '112-1 rejections fail to establish a prima facie case.

The Examiner's position is contrary to the law.

The function of the description requirement is to ensure that the inventor had possession of, as of the filing date of the application relied upon, the specific subject matter later claimed by him; how the specification accomplishes this is not material. In re Smith, 481 F.2d 910, 178 USPQ 620 (CCPA 1973). The claimed subject matter need not be described in haec verba to satisfy the description requirement. In re Smith, 59 CCPA 1025, 458 F.2d 1389, 173 USPQ 679 (CCPA 1972). It is not necessary that the application describe the claim limitations exactly, but only so clearly that one having ordinary skill in the pertinent art would recognize from the disclosure that appel-

[52] In re Smythe, 480 F.2d 1376, 178 USPQ 279 (CCPA 1973).

lants invented processes including those limitations. In re Smythe, 480 F.2d 1376, 178 U.S.P.Q. 279 (CCPA 1973).

Herschler.[53]

Notwithstanding the fact that the disclosure has extensive literal support for the claimed invention, such literal support is not required for written description.

> Compliance with the written description requirement of Section 112 only requires that appellant's application contain sufficient disclosure, expressly or inherently, to make it clear to persons skilled in the art that appellant possessed the subject matter claimed. In re Mott, 539 F.2d 1291, 190 USPQ 536, 541 (CCPA 1976). The test for determining compliance with the written description requirement is whether the disclosure of the application as originally filed reasonably conveys to the artisan that the inventor had possession of the claimed subject matter, rather than the presence or absence of literal support in the specification for the claim language. In re Maslow, 707 F.2d 1366, 217 U.S.P.Q. 1089, 1096 (Fed. Cir. 1983).

Harvey.[54]

Thus, no particular language is required and no literal language support is necessary for the claim language to meet the written description requirement. Furthermore, the drawings may be used (but are not re-

---

[53] In re Herschler, 591 F.2d 693, 700-701, 200 USPQ 711, 717 (CCPA 1979) (emphasis added).

[54] Ex Parte Harvey, 3 USPQ2d 1626, 1627 (Bd. Pat. App. and Int. 1986) (emphasis added).

quired to be used) to support the written description requirement.[55] Hence, the instant disclosure, which is extensive, is certainly adequate to comply with the '112-1 written description requirement.

In view of the above, the Examiner uses the wrong legal basis to uphold the '112-1 rejection by improperly requiring verbatim support to satisfy the written description requirement. Hence, the '112-1 written description rejection should be reversed.

8.3.2 The Written Description Rejection Does Not Establish A Prima Facie Case

The written description rejection does not establish a prima facie case for the reasons discussed in Section 8.1.8 and for the additional reasons discussed below.

a. The Examiner requires that the claim language have verbatim, basis in the disclosure, but the law does not even require literal description (Section 8.3.1).

b. The Examiner alleges complete lack of written, description while ignoring literal written description in the disclosure.

In view of the above, the written description rejection does not establish a prima facie case. Hence, the written description rejection should be reversed.[56]

---

[55] The content of the drawing may also be considered in determining compliance with the written description requirement. See In re Barker, 559 F.2d 588, 194 USPQ 470, 474 (CCPA 1977); In re Kaslow, 707 F.2d 1366, 1375, 217 USPQ 1089, 1096 (Fed. Cir. 1983).

[56] In re Oetiker, 977 F.2d 1443, 24 U.S.P.Q.2d 1443 (Fed. Cir. 1992).

8.3.3 Conclusion

The 35 USC 112-1 written description rejection should be reversed for the reasons set forth above; the claim terminology does not have to be stated verbatim and the written description rejection does not establish a prima facie case; and for the additional reasons set forth in Section 8.1.9.

8.4 ARGUMENTS COMMON TO OBVIOUSNESS-TYPE AND NONOBVIOUSNESS-TYPE DOUBLE PATENTING REJECTIONS

Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-162 stand rejected for obviousness-type double patenting and for nonobviousness-type double patenting over claims of eight copending applications. The arguments common to both the obviousness-type and the nonobviousness type double patenting rejections are set forth in this Section 8.4. The arguments primarily related to the obviousness-type double patenting rejection are set forth in Section 8.5 to supplement the arguments set forth in this Section 8.4. The arguments primarily related to the nonobviousness-type double patenting rejection are set forth in Section 8.6 to supplement the arguments set forth in this Section 8.4.

As discussed in Section 8.1.1 above (see Footnote 13), MPEP 706.03 establishes that the instant application should not have "undue emphasis" given to "technical" issues (e.g., double patenting issues). MPEP 706.03 further requires that double patenting rejections "should be stated with a full development of the reasons rather than by a mere conclusion coupled with some sterotyped expression". However, the double patenting rejections in the instant application rely on unsupported

conclusionary statements, such as unsupported statements that claim limitations are obvious or covered by the copending claims while ignoring the fact that the claims are independent or distinct (Section 8.4.2).

The double patenting rejections do not, and in fact cannot,[57] establish a prima facie case of double patenting.

The Appellant respectfully traverses the double rejections for the reasons discussed in Sections 8.4.1 et seq, 8.5, and 8.6.

8.4.1 The Double Patenting Rejections Overlook Restriction Requirements

The Examiner has overlooked restriction requirements in the parent applications and in related applications (the subject restrictions). In view of the restriction requirements placed on the Appellant, the double patenting rejections should be reversed.

In the subject restrictions, the prior examiners restricted the claims to independent or distinct species, some of which were similar there between. Hence, the prior examiners put the Appellant on notice that distinctness would be narrowly interpreted. Now, the instant Examiner changes this position by broadly interpreting distinctness. After the prior examiners put the Appellant on notice that distinctness would be interpreted narrowly and after the Appellant claimed different distinct species in the instant application, the present Examiner now alleges double patenting of the instant distinct inventions.

---

[57] The Examiner cannot establish a prima facie case of double patenting because there is no double patenting.

For example, in ancestor application Serial No. 08/034,627 the examiner therein identified two of the 12 inventions as:

> a. "a general data processing system" (emphasis added)
>
> b. "a general data processing system configured differently than the inventions cited above" (emphasis added)
>
> both inventions are "classified in Class 395, subclass 800". However, the instant claims are significantly more distinct than the claims in these two identically classified "general data processing system" inventions. Hence, to be consistent in its holdings of distinctness and in accordance with the doctrine of judicial estoppel (Section 8.10), the double patenting rejections should be reversed.

Further, in copending application Serial No. 08/471,710 (the '710 application), the examiner therein restricted the invention between the following "distinct" inventions:

> generating and storing image information
>
> generating and storing two dimensional vector information
>
> generating and storing scale factor information
>
> generating and storing weight information
>
> generating and storing two dimensional vector, scale factor, and weight information[58]

---

[58] The Appellant elected this fifth invention with traverse.

The claims recite such limitations, but the Examiner has not addressed the independence or distinctness thereof.

Still further, in copending application Serial No. 08/464,441 (the '441 application), the examiner therein restricted the invention between the following "independent or distinct" inventions:

a graphics system[59]

a memory system including a pixel memory

a two dimensional pixel address circuit

a pixel memory accessing circuit generating blocks of 64 pixels

a weight circuit generating weight information a weighting circuit

a sample memory

a sample memory writing circuit

a two dimensional scanout circuit

a sample memory sequential accessing circuit and an output memory

The examiner therein stated[60]:

> Newly submitted claims directed to an invention that is independent or distinct from the invention originally claimed for the following reasons.
>
> The above claims are directed to a memory system including a pixel memory, a two dimensional pixel

---

[59] The graphics system was held to be constructively elected by the examiner therein

[60] See the Action dated May 6, 1997 at page 2 in copending application Serial No. 08/464,441.

> address circuit, a pixel memory accessing circuit generating blocks of 64 pixels, a weight circuit generating weight information, a weighting circuit, a sample memory, a sample memory writing circuit, [a] two dimensional scanout circuit, a sample memory sequential accessing circuit and an output memory. The originally claimed invention does not include these claimed features.

The claims recite such limitations, but the Examiner has not addressed the independence or distinctness thereof. This is not surprising since many of the limitations of the claims in the different applications are independent or distinct there between. The Board is respectfully requested to compare the limitations that are established as being independent or distinct by these restriction requirements, listed above, with the limitations listed in Table-1 regarding the '112-1 rejections.

Still further, 35 USC 121 prohibits double patenting rejections in divisional applications where restriction requirements were imposed. The instant application is a constructive divisional[61] application. Hence, it is necessary for the Examiner to address the subject restrictions and the holdings of independence or distinctness therein.

The subject restrictions in the parent application represented an unequivocal message to the Appellant that claim distinctness would be narrowly construed and that the Appellant would not be able to prosecute claims

---

[61] MPEP 201.06 defines a Division as a later application for a distinct or independent invention, carved out of a pending application and disclosing and claiming only subject matter disclosed in the earlier or parent application. The instant application meets this definition.

of the type and scope in the instant application. Hence, it is manifestly appropriate and proper for the Appellant to consider the restriction requirement to be constructive notice that the claimed subject matter of the instant application claims as being independent or distinct from the claimed subject matter of the parent application.

After distinctness between the distinct inventions has been established, the Examiner cannot be permitted to now reject claims having an even greater degree of independence or distinctness. For example, subject restrictions restricted different species as being distinct there between. However, the instant claimed invention is even more distinct than the subject restricted species.

The Examiner now rejects each and every one of the claims of the instant application for nonobviousness-type double patenting on the allegation that there is no reason that the Appellant did not prosecute all of the instant claims in the copending applications. However, this allegation completely disregards the restriction requirements.

In view of the above, the double patenting rejections are inconsistent with restriction requirements placed on the other applications. Hence, the double patenting rejections should be reversed.

8.4.2 The Instant Claims Are Independent Or Distinct From The Claims Of The Copending Applications

Because the instant claims are independent or distinct from the copending claims, the double patenting rejections are prohibited. See MPEP 802.01; MPEP 804; Schneller.[62] The Examiner has made no attempt to

---

[62] In re Schneller, 397 F.2d 350, 158 USPQ 210 (CCPA 1968).

show that the claims are neither independent nor distinct. This is not surprising considering that the application claims are independent or distinct from the copending claims. See the claim charts in Exhibit-2 for side-by-side claim comparisons.

In view of the aforementioned claim charts, it is clear that the instant claims do not recite, do not need, and are not dependent on the inventions claimed in the copending applications. These inventions are not dependent on each other nor do they require each other (even though they can optionally be used together). They can function with or without each other. Hence, the instant claims and the copending claims are independent of (not dependent on) each other (MPEP 802.01).

Additionally, the instant claimed invention and the inventions claimed in the copending applications can each be separately manufactured, used, and sold. Hence, the instant claims and the copending claims are distinct from each other. (MPEP 802.01).

Similarly, in Heinle[63], the application claims were "separately usable and salable" and hence were distinct from the patent claims therein. Similarly, the instant claims and the copending claims are "separately usable and salable" and, therefore distinct from each other. See, for example, the claim charts shown in Exhibit-2 and discussed in Sections 8.4.3.

In view of the above, the instant claims are independent or distinct from the copending claims. Hence, the double patenting rejections should be reversed.

---

[63] In re Heinle, 342 F.2d 1001, 145 USPQ 131 (CCPA 1965).

8.4.3 There Are Many Novel Differences Between The Instant Claims And The Copending Claims

There are many novel differences between the instant claims and the copending claims. The Examiner even admits to the presence of differences (Final Action at 25 and 27). The claim charts establish significant novel claim differences between the claims of the instant application and the eight copending applications (Exhibit-2) and the combination summaries establish the differences between the claims of the instant application (Exhibit-3). Nevertheless, the Examiner has not even attempted to compare the claims, to compare each contested instant claim with each copending claim, to compare the contested claim limitations, or to provide the required Gechter[64] and Graham[65] analyses. This is not surprising since such comparisons and such analyses would have confirmed that the claims are independent or distinct (Exhibit-2) and the Examiner would not have been able to persist in the double patenting rejections.

The instant claims have different novel combinations of limitations which are independent or distinct from the copending claims. For example, side-by-side claim comparisons are provided for selected claims in Exhibit-2 with copending claims from each of the eight copending applications to show the two-way distinctions between the claims. These claim comparisons show significant novel differences between the instant claims and the copending claims.

---

[64] Gechter v. Davidson, 116 F.3d 1454, 43 USPQ2d 1030 (Fed. Cir. 1997).

[65] Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966).

Further, the novel combination of elements for each instant apparatus claim and the novel combination of acts for each instant process claim are set forth in Exhibit-3.[66] Because the "'ing" verb' (e.g., generating, storing, etc.)[67] limitations in the apparatus claims are similar to the "'ing" verb' limitations set forth in corresponding process claims, the "'ing" verb' limitations are not repeated for the apparatus claims in Exhibit-3. The novel combinations of contested limitations shown in Exhibit-3 illustrate the significant novel differences between the instant claims and the copending claims.

Further, each apparatus claim and each process claim recites novel combinations of responsive[68] limitations in addition to the novel combination of elements and novel combination of "'ing" verb' limitations. Because these responsive limitations are clearly set forth in the Appendix and are related to the novel combinations, it is not necessary to separately set forth these responsive limitations. However, the Appellant will set forth a separate combination of these responsive limitations if requested by the Examiner in the Answer.

Further, each apparatus claim has a novel combination of coupling limitations in addition to the novel combination of elements, novel combination of "'ing" verb'

---

[66] For simplicity of illustration, the combination shown for each dependent claim recites the parent claim number as being representative of the combination of elements or acts listed for the parent claim and intended to be further combined with the elements or acts listed for the dependent claim.

[67] The Federal Circuit uses the term "'ing" verb' (passing, heating, reacting, transferring, etc.) in its discussion in O.I. Corp. v. Tekmar, 115 F.3d 1576, 42 USPQ2d 1777 (Fed. Cir. 1997).

[68] E.g., " in response to . . . " .

limitations, and novel combination of responsive limitations. Because these coupling limitations are clearly set forth in the Appendix and are related to the combinations of contested limitations set forth in Exhibit-3, it is not necessary to separately set forth these coupling limitations. However, the Appellant will set forth a separate combination of these coupling limitations if requested by the Examiner in the Answer.

The recited elements, "'ing verb' limitations, responsiveness limitations, coupling limitations, and combinations thereof constitute contested limitations.

In view of the above, there are many novel differences between the instant claims and the copending claims. Hence, the double patenting rejections should be reversed.

8.4.4 The Double Patenting Rejections Do Not Even Provide A Claim-By-Claim Analysis, Much Less The Limitation-By-Limitation Analysis Required by The Federal Circuit

The Federal Circuit requires that double patenting rejections be supported on a limitation-by-limitation basis with specific fact findings for each contested limitation and satisfactory explanations for such findings. The claim construction used in contesting the limitations must also be explicit. The Federal Circuit also requires fact findings, adequately explained, for each relevant factor.[69] However, the double patenting rejections fail to meet these requirements. The double patenting rejections do not even provide a claim-by-claim analysis, much less a limitation-by-limitation analysis. The Gechter decision outlining the analytical requirements

[69] Gechter v. Davidson, 43 USPQ2d 1030, 1035 (Fed. Cir. 1997).

for a proper rejection followed closely on the heels of the Supreme Court decision in Warner-Jenkinson[70] affirming the requirement for an limitation-by-limitation analysis in defining the scope of a patented invention in infringement analyses.

In addition, the CCPA, in reversing a prior art rejection, ruled that all words in a claim must be considered in evaluating patent ability regarding the prior art.

> In this respect, the section 102 rejection in this case is not unlike the section 103 rejection which we reversed In re Wilson, 57 CCPA 1029, 424 F.2d 1382, 165 USPQ 494 (1970), and is unsupportable for the same reason: "All words in a claim must be considered in judging the patent ability of that claim against the prior art" (emphasis added). Id. at 1032, 424 F.2d at 1385, 165 USPQ at 496.

Miller[71] (emphasis in original). This prior art issue is relevant to the instant double patenting rejections. See Braithwaite.[72]

In violation of the aforementioned black letter law, the Examiner did not even consider any particular claim, much less all words, elements, and limitations in all claims. Hence, the Examiner violated Gechter and Warner-Jenkinson by failing to support the rejection on a claim-by-claim basis, much less on the required limitation-by-limitation basis.

---

[70] Warner-Jenkinson Co. v. Hilton Davis Chemical Co., 117 S. Ct. 1040, 41 USPQ2d 1865 (1997).

[71] In re Miller, 441 F.2d 689, 693, 169 USPQ 597, 600 (CCPA 1971).

[72] In re Braithwaite, 379 F.2d 594, 154 USPQ 29 (CCPA 1967).

Still further, the Examiner merely identified elements in the references upon which certain claim elements allegedly read. The Examiner did not make any specific fact findings for each contested limitation, nor provide a satisfactory explanation, nor explain the claim construction used in contesting the limitations as required by Gechter. The Examiner did not even perform a Gechter analysis on a single claim. The court in Gechter commented that if claim construction is not explicit or if the claims were misconstrued, a finding of anticipation must be reversed. 43 USPQ2d at 1033. The claims must first have been correctly construed to define the scope and meaning of each contested limitation. See also Paulsen.[73] The court in Paulsen commented that in order to properly compare a reference with the claims, it is necessary to construe the contested term to ascertain its scope and meaning. Id. at 1674.

The court in Gechter further commented that the PTO must expressly find that every limitation in the claim was identically shown in the single reference. 43 USPQ2d at 1035. Such findings should provide an explanation for whether, how, and why the reference contains each of the limitations of the claim. Thus, said the court, the explanation should define the exact function of the elements as well as find that the prior art reference disclosed the identical function.

Further, the Examiner is required to consider the scope and meaning of the limitations used in the claims (i.e., construe each claim limitation). However, the Examiner does not do what Gechter and Paulsen require

---

[73] In re Paulsen, 30 F.2d 1475, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994).

for determining the scope and meaning of the contested limitations.

The Gechter limitation-by-limitation analysis is required for obviousness-type double patenting rejections because Gechter addresses 35 USC 103 rejections and it is well established that an obviousness type double patenting rejection requires the same type of obviousness analysis as a 35 USC 103 obviousness rejection (Section 8.9). See Longi.[74] Hence, Gechter is equally relevant to obviousness-type double patenting rejections.

Further, the Gechter limitation-by-limitation analysis is necessary for the nonobviousness-type double patenting rejection. This is because Judge Rich in Schneller[75] performed a comparison of the limitations A, B, C, X, and Y for the patent claims and for the application claims and concluded that the application claims and the patent claims were all directed to the best mode (or preferred embodiment). Significantly, the Schneller court made a limitation-by-limitation analysis as did the court in Gechter. Hence, the Examiner must also perform such a limitation-by-limitation analysis in support of the nonobviousness-type (Schneller-type) double patenting rejections in the instant application. However, the nonobviousness-type (Schneller-type) double patenting rejections do not have any claim comparisons at all, much less the required limitation-by limitation analysis.

In direct violation of Gechter, other, court precedent, and the PTO's rules; the Examiner has not supported

---

[74] In re Longi, 759 F.2d 887, 225 USPQ 645, 648 (Fed. Cir. 1985).

[75] In re Schneller, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). Schneller is the case relied upon by the Examiner to support the nonobviousness-type double patenting rejection.

the rejections on a limitation-by-limitation basis with specific fact findings for each contested limitation and satisfactory explanations for such findings, has not provided explicit claim construction for each contested limitation, and has not supported the rejections with adequately explained fact findings for each relevant factor. This is not surprising since such analyses would have confirmed that the instant claims distinguish over the copending claims (Exhibit-2 and Exhibit-3) and the Examiner would not have been able to persist in the double patenting rejections.

In view of the above, the Examiner has not provided a Gechter analysis in support of the double patenting rejections because a Gechter analysis would show that the instant claims distinguish over the claims of the copending applications. Hence, the double patenting rejections should be reversed.

8.4.5 Simultaneous Issuance Of The Instant And Copending Patent Applications Would Obviate The Double Patenting Rejections

Applications which have similar or common subject matter and which issue on the same day have met with approval in the courts for many years. In Clark[76], the court acknowledged with approval that there is no double patenting where the patents issued on the same day. By simultaneously issuing similar patents on the same day, neither extends the life of the other and thus no harm can result insofar as extension of the patent monopoly is concerned.

---

[76] J.R. Clark Co. v. Jones & Laughlin Steel Corp., 186 F. Supp. 22, 125 USPQ 433 (D.C. Ind. 1960).

The court in Clark at 438 quoted with approval from Sheaffer[77]:

> "Whether or not the designs could have been combined in one patent, it is quite apparent that the plaintiff has obtained no advantage from the triple patenting, since the period of the monopoly has not been extended one day beyond what it would have been if a single patent had been issued, because all of them were applied for and issued on the same days."

The PTO has long facilitated simultaneous issuance of patents. See MPEP 1306.02.[78] The Appellant has previously utilized this procedure in previous ancestor applications. In particular, this Appellant filed a petition for simultaneous issuance in each of three ancestor applications, all three patents issued simultaneously on the same day[79], and all three patents expired on the same day.

In view of the above and notwithstanding the impropriety of the double patenting rejections, the Appellant hereby requests in accordance with MPEP 1306.02 simultaneous issuance of the instant application and the

---

[77] W.A. Sheaffer Pen Co. v. Eagle Pencil Co., 55 F.2d 420 (D.C.S.D. N.Y. 1931).

[78] 1306.02 Simultaneous Issuance of Patents

Where applications have been allowed and a Notice of Allowance and Issue Fee Due (PTOL-85) has been mailed in each application, a request for simultaneous issuance will be granted. Unless all the applications have reached this stage of processing, or a specific requirement of the regulations is involved (e.g., 37 CFR 1.177), a request for simultaneous issuance generally will not be granted. [emphasis added]

[79] Patent No. 4,209,843; Patent No. 4,209,852; and Patent No. 4,209,853 all issued simultaneously on June 24, 1980.

eight subject copending applications. This action will obviate the provisional double patenting rejections over the eight copending applications.

8.4.6 The Double Patenting Rejections Do Not Establish A Prima Facie Case

The double patenting rejections do not establish a prima facie case[80], as discussed below.

a. The instant claims are not addressed individually, but rather are improperly rejected as groups of claims.

b. There are significant differences between the instant claims and the copending claims that the Examiner even acknowledges, but the rejections do not address these differences.

c. The Examiner completely ignores various restriction requirements in related applications (Section 8.4.1).

d. The double patenting rejections do not even provide a proper one-way double patenting analysis and certainly do not perform the necessary two-way double patenting analysis. See Braat.[81] See also MPEP 804(B)(1)(b).

---

[80] See 37 CFR 1.106(b); Chester v. Miller, 906 F.2d 1574, 1578, 15 USPQ2d 1333, 1337 (Fed. Cir. 1990) ("Section 132 is violated when a rejection is so uninformative that it prevents the applicant from recognizing and seeking to counter the grounds for rejection."). See also In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992).

[81] In re Braat, 937 F.2d 589, 19 USPQ2d 1289 (Fed. Cir. 1991).

e. Listed features challenged under 35 USC 112-1 (Table-1) are completely ignored in the double patenting rejections.

f. The Appellant properly traversed the Examiner's unsupported statements, but the Examiner did not provide the required reference or affidavit in accordance with MPEP 2144.03.

g. The rejections are grossly inconsistent (Section 8.10) by alleging complete lack of disclosure in support of '112-1 rejections and then alleging full disclosure (Section 8.1.2) in support of double patenting rejections.

h. The Federal Circuit requires a limitation-by limitation analysis, but the double patenting rejections do not even provide a claim-by-claim analysis (Section 8.4.4).

i. The double patenting rejections do not address double patenting over systems that are non-analogous.

j. The double patenting rejections fail to provide the required Gechter analysis and Graham analysis (Sections 8.4.3, 8.4.4, 8.5, and 8.9.2).

k. The double patenting rejections do not address double patenting between apparatus and process claims.

l. A claim must be read as a whole in analyzing double patenting.[82]

---

[82] Carman Indus., Inc. v. Wahl, 724 F.2d 932, 840, 220 USPQ 481, 487 (Fed. Cir. 1983) ("[W]e wish to clarify that double patenting is determined by analysis of the claims as a whole").

The burden of establishing a prima facie case for rejecting claims rests with the examiner. However, the Examiner has never even provided a claim comparison in support of the double patenting rejections much less performed any analysis which establishes a prima facie case.[83] Hence, in view of the Examiner's failure to establish a prima facie case, the double patenting rejections should be reversed.

Each claim must be evaluated individually, particularly where, as here, the distinctions of the claims are separately argued (e.g., Sections VII and 8.4 to 8.6, Exhibit-3). See Van Geuns.[84] The rejections do not properly acknowledge that different claims in the instant application recite different combinations of features, much less compare these different combinations of features with the copending claims.

Further, there are significant differences between the instant claims and the copending claims (Section 8.5.3). However, the rejections never address these claim differences. In an obviousness-type double patenting rejection, claim differences must be evaluated using an obviousness analysis. Therefore, ignoring the claim differences is fatal to the double patenting rejections.

It is particularly noteworthy that the many application claim limitations challenged under 35 USC 112-1 (e.g., Sections 8.1 to 8.3), which provide differences between the instant claims and the copending claims, are

---

[83] In re Edwards, 568 F.2d 1349, 1354, 196 USPQ 465, 469 (CCPA 1978); In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992).

[84] In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

ignored as claim differences in the double patenting rejections.

Various related applications have restriction requirements which must be considered regarding the double patenting rejections (Section 8.4.1).

The claims are all improperly rejected as groups of claims. In order to establish a prima facie case, each claim must be evaluated individually. Since the Examiner did not evaluate the claims individually, the double patenting rejections are improper for failing to establish a prima facie case. See Van Geuns and Wright.[85]

The Appellant developed his position with reasoning and evidence and traversed the Examiner's unsupported statements, but the Examiner did not provide a reference or an affidavit in support of his position in violation of MPEP 2144.03. Further, these unsupported statements are "in areas of esoteric technology" and hence should have been supported by a citation of a reference (MPEP 2144.03), but were not thusly supported.

The double patenting rejections indiscriminately reject apparatus claims over process claims and process claims over apparatus claims without any analysis even though apparatus and process claims represent different statutory categories of invention. The double patenting rejections fail to provide the required Gechter analysis and Graham analysis regarding these apparatus and process claims.

---

[85] In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993); In re Wright, 999 F.2d 1557, 27 USPQ2d 1510 (Fed. Cir. 1993).

In view of the above, the double patenting rejections do not establish a prima facie case. Hence, the double patenting rejections should be reversed.[86]

8.4.7 Conclusion

Thus, the two types of double patenting rejections (obviousness-type and nonobviousness-type double patenting rejections) should be reversed for the reasons set forth above; the double patenting rejections overlook restriction requirements; the instant claims are independent or distinct from the claims of the copending applications; there are many differences between the instant claims and the copending claims; the Federal Circuit requires a limitation-by-limitation analysis, but the double patenting rejections do not even provide a claim by-claim analysis; simultaneous issuance would obviate the provisional double patenting rejections; and the double patenting rejections do not establish a prima facie case.

8.5 OBVIOUSNESS-TYPE DOUBLE PATENTING REJECTION

Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-162 stand rejected for obviousness-type double patenting over claims of eight copending applications. The Appellant respectfully traverses this rejection for the reasons discussed in Sections 8.4, 8.7, and 8.9 and for the additional reasons discussed in this Section 8.5 below.

The obviousness-type double patenting rejections do not establish a prima facie case for the reasons dis-

---

[86] In re Oetiker, 977 F.2d 1443, 24 U.S.P.Q.2d 1443 (Fed. Cir. 1992).

cussed in Section 8.4.6 and for the additional reasons discussed below.

a. The rejections do not establish that the claim differences are obvious.

b. The rejections do not provide the required Graham analysis or the required Gechter analysis.

The Appellant has established that there are extensive differences between the instant claims and the copending claims (Sections 8.4.3). Hence, to support an obviousness-type double patenting rejection, it is incumbent upon the Examiner to establish that the differences are obvious. See Longi.[87] However, the obviousness-type double patenting rejection does not establish that these differences are obvious and hence the obviousness-type double patenting rejection should be reversed.

An obviousness-type double patenting rejection is similar to an obviousness rejection under 35 USC 103. See Braithwaite.[88] Thus, a prima facie case of obviousness-type double patenting must be established in the same manner that it is required for a rejection under 35 USC 103. See Longi. Accordingly, the factual inquiries set forth in Graham (Section 8.9.2) must be employed when making an obviousness-type double patenting analysis. However, the rejections do not provide this analysis. Instead, the rejections dismiss distinct limitations as "minor differences" (Final Action at 25 and 27). Further, the Examiner contends obviousness of claim differences without any support whatsoever (Final Action at 25 and 27). This is improper. Unsupported

---

[87] In re Longi, 759 F.2d 887, 225 USPQ 645, 648 (Fed. Cir. 1985).

[88] In re Braithwaite, 379 F.2d 594, 154 USPQ 29 (CCPA 1967).

conclusionary statements are no substitute for the required Graham analysis and a Gechter analysis.

In view of the above and in view of Section 8.4, the obviousness-type double patenting rejections should be reversed.

8.6 NONOBVIOUSNESS-TYPE DOUBLE PATENTING REJECTION

Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-162 stand rejected for nonobviousness-type nonobviousness-type (Schneller-type) double patenting over claims of eight copending applications. The Appellant respectfully traverses this rejection for the reasons discussed in Sections 8.4 and 8.6.1 et seq.

The long established law of double patenting is clear and requires a two-part test. The first test is for same-invention type double patenting. The second test is for obviousness-type double patenting. If a claim passes both tests "there is no double patenting." See Vogel.[89]

The Schneller-type double patenting rejections do not establish a prima facie case of double patenting under either the first test (same-invention-type double patenting) or the second test (obviousness-type double patenting). Instead, the Examiner seeks to change the long established black letter law of double patenting by applying an ill-defined third test for double patenting that is based upon Schneller[90], which has since been superseded by Vogel. The Appellant demonstrates below

---

[89] In re Vogel, 422 F.2d 438, 442, 164 USPQ 619, 622 (CCPA 1970).

[90] In re Schneller, 397 F.2d 350, 158 USPQ 210 (CCPA 1968).

(1) that Schneller does not represent the law and (2) that the present claims nevertheless satisfy the Schneller test.

8.6.1 The Controlling Two-Part Test For Double Patenting Has Been Established By In Re Vogel

The two-part test for double patenting as it exists today was enunciated by the CCPA in the in banc decision of Vogel and later adopted by the Federal Circuit in Longi. Vogel expressly restated the controlling law of double patenting and thereby laid the foundation for the law of double patenting as it exists today. The court stated:

> The proceedings below in this case indicate the advisability of a restatement, of the law of double patenting as enunciated by this court.

Vogel.[91]

In the Federal Circuit, the judges usually sit as a three judge panel and earlier decisions are given precedence over later decisions except when a decision is rendered in banc. However, all CCPA cases, including Vogel, were rendered in banc and later decisions therefore took precedence over earlier decisions. Later decisions sub silentio overruled any prior decisions to the extent that a prior decision was inconsistent with a later decision. As stated by the Federal Circuit:

> To the extent that [the later decision] language is inconsistent with that in [earlier decisions], that inconsistency has already been sub silentio removed. The CCPA's later decisions control because that court always sat en banc.

---

[91] 422 F.2d at 441, 164 USPQ at 621.

Gosteli.[92]

Thus, Vogel's two-part test for double patenting became controlling law and sub silentio overruled any prior CCPA decisions, including Schneller, that were inconsistent with the two-part test. The first part of the Vogel test was defined as follows:

> The first question in the analysis is: Is the same invention being claimed twice? . . . By "same invention" we mean identical-subject matter.

422 F.2d at 441, 164 USPQ at 621.

The court explained that a patent cannot be granted, whether or not a terminal disclaimer is filed, if the same invention is being claimed. However, if the same invention is not being claimed, a second test must be considered.

> The second analysis question is: Does any claim in the application define merely an obvious variation of an invention disclosed and claimed in the patent?

422 F.2d at 442, 164 USPQ at 622. The conclusions to be drawn from the tests were stated as follows,

> If the answer to the second question is no, there is not a double patenting involved and no terminal disclaimer need be filed. If the answer is yes, a terminal disclaimer is required to prevent undue timewise extension of monopoly.

422 F.2d at 442, 164 USPQ at 622 (emphasis added).

---

[92] In re Gosteli, 872 F.2d 1008, 1011, 10 USPQ2d 1614, 1617 (Fed. Cir. 1989).

Since the third test for double patenting used in Schneller is wholly inconsistent with the two-part test enunciated in Vogel, Schneller is necessarily overruled by Vogel and therefore cannot be applied by the PTO.

The two-part test for double patenting has been consistently followed by subsequent CCPA and Federal Circuit decisions. For example, in the case of Avery[93], the CCPA expressly recognized the restatement of the law of double patenting by Vogel and applied the two-part double patenting test of Vogel. The court in Avery reached the decision that there was no same-invention-type double patenting under the first test but that there was obviousness-type double patenting under the second test.

The Federal Circuit adopted the Vogel two-part test for double patenting in Longi[94] stating:

> A double patenting rejection precludes one person from obtaining more than one valid patent for either (a) the "same invention," or (b) an "obvious" modification of the same invention.

The adoption of the two-part test was later affirmed by the Federal Circuit in Braat.[95]

The Schneller-type double patenting rejections are neither (1) same-invention-type double patenting nor (2) obviousness-type double patenting. The Schneller-type double patenting rejections thus fail to fit within any acceptable type of double patenting rejection

---

[93] In re Avery, 518 F.2d 1228, 186 USPQ 161 (CCPA 1975).

[94] In re Longi, 759 F.2d 887, 892, 225 USPQ 645, 648 (Fed. Cir. 1985).

[95] In re Braat, 937 F.2d 589, 19 USPQ2d 1289 (Fed. Cir. 1991).

and the rejections that rely upon the earlier case of Schneller to justify a third "nonobviousness" test for double Patenting should be reversed.

8.6.2 The Board Should Not Ignore In Re Vogel By Creating A Third Test For Double Patenting

The Final Action seeks to add a third "nonobviousness" test to the two-part test that was established by the in banc Vogel decision and later adopted by the Federal Circuit in Longi. In particular, the Final Action seeks to reinstate Schneller. Schneller was a bad decision which was mercifully overruled sub silentio when the in banc decision in Vogel restated the law of double patenting. Schneller should not be resurrected some 30 years after its timely demise.

Vogel expressly defines a two-part test for double patenting and then states if "the answer to the second question is no, there is no double patenting involved and no terminal disclaimer need be filed." 422 F.2d at 442, 164 USPQ at 622 (emphasis added). To add a third Schneller test for double patenting as asserted by the Final Action would thus require the Board to ignore the controlling law as enunciated in Vogel and the subsequent Federal Circuit cases defining a two-part test for double patenting.

8.6.3 The Present Claims Satisfy The Overruled Schneller Inquiries For Double Patenting

Even if the controlling precedent handed down in Vogel were ignored and the third Schneller test for patentability applied, the present claims nevertheless fully satisfy the third Schneller test. In addition to the absence of any legal basis for the third test, the Appel-

lant traverses the rejections based upon Schneller for double patenting for the following reasons.

1. The rejections fail to establish a prima facie case of Schneller-type double patenting (Sections 8.6.7. and 8.6.8).

2. The instant claims are independent or distinct from all of the copending claims (Section 8.4.2).

3. Schneller is limited to cases where a patent and an application claim the same preferred embodiment, which does not apply to the present case (Section 8.6.4).

4. The facts in the instant application are distinguishable from the Schneller facts (Section 8.6.5).

Thus, even if Schneller were a valid legal precedent for the Examiner to invoke, any one of these reasons is sufficient reason for reversing the Schneller-type double patenting rejections and the combination of all of these reasons represent overwhelming grounds for reversal.

8.6.4 Schneller Only Applies Where The Patent Claims And The Application Claims Are Directed To The Same Preferred Embodiment

Schneller double patenting is limited to use where a patent and an application both claim the same preferred embodiment or the same beat mode. This is in direct contrast to the present application.

Schneller double patenting is specifically applied to "patent protection on the preferred embodiment of the invention, ABCXY". 397 F.2d at 355, 158 USPQ at 215 (emphasis added). See also 397 F.2d at 354, 158 USPQ at 215 ([The patent claims] '"cover" the preferred form ABCXY common to the patent and this application')

(emphasis added); 397 F.2d at 356, 158 USPQ at 216 ("Anyone attempting to utilize what he disclosed in the patent . . . in preferred and only form in which he described these clips, would thus run afoul of a still unexpired patent if the application claims were allowed.") (emphasis in original); 397 F.2d at 355, 158 USPQ at 216 ("[T]he greatest advantage and best mode of practicing the invention as disclosed is obtained by using both inventions in the combination ABCXY." (emphasis added).) Schneller even admitted that the preferred embodiment ABCXY was the "best mode" of practicing his invention. 397 F.2d at 354, 158 USPQ at 214.

In further contrast to Schneller, the disclosures in the instant application and in the eight copending applications recite many different features, inventions, and alternate embodiments. See, e.g., the Table of Contents at Exhibit-1. Further, the disclosures in the copending applications and in the instant application are extensive (Sections V and 8.1 to 8.3). The different inventions claimed in the instant application and in the copending applications are not disclosed as being component parts of the same preferred embodiment. Numerous different embodiments are disclosed. The disclosure has over 30 occurrences of "alternate" type terminology. Also, the instant application discloses different embodiments. In contrast, Schneller has only two sheets of drawings and only six columns of specification which are indicated to be directed to a single preferred embodiment.

In further contrast to Schneller, the disclosures in the instant and copending applications expressly state plural preferred embodiments at various places. Conversely, the Schneller patent and application were specifically drawn to a single preferred embodiment. This

was an important factor in the Schneller decision. The Final Action does not contend that the instant application discloses only a single preferred embodiment, because it does not. Rather, the instant application discloses numerous alternate embodiments and plural preferred embodiments.

It is not surprising that the Examiner does not contend that the copending claims are directed to the same specific type of system recited in the instant claims nor that the instant claims and the copending claims cover a single preferred embodiment. They, in fact, are not directed to the same type-of system and do not cover a single preferred embodiment. For these reasons alone, the nonobviousness-type double patenting rejections should be reversed.

8.6.5 The Facts In The Instant Application Are Significantly Different From The Facts Of Schneller

8.6.5.1 Introduction

Schneller is a very narrow fact-specific decision. The Court in Schneller stated:

> Once more we "caution again against the tendency 'to freeze into rules of general application what, at best, are statements applicable to particular fact situations'." In re Riden, 50 CCPA 1411, 1415, 318 F.2d 761, 763, 138 U.S.P.Q. 112, 114 [(1963)].

397 F.2d at 355, 158 USPQ at 215. Schneller itself is a very specific fact sensitive and fact intensive case that must be very narrowly construed. See Section 8.6.4 entitled Schneller Only Applies Where The Patent Claims And The Application Claims Are Directed To The Same

Preferred Embodiment. See also Sections 8.6.5.1 to 8.6.5.5 herein.

The PTO acknowledges that Schneller-type double patenting rejections are only appropriate in certain rare and unique circumstances. According to the MPEP:

> There are some unique circumstances where it has been recognized that another type of nonstatutory double patenting rejection, is applicable even where the inventions claimed in two or more applications/patents are considered nonobvious over each other. These circumstances are illustrated by the facts before the court in In re Schneller, 397 F.2d 350, 158 U.S.P.Q. 210 (CCPA 1968).

MPEP 804 (emphasis added).

The facts surrounding the instant application are vastly different from the facts in Schneller. As such, the "unique circumstances" surrounding Schneller are not present in the instant application and therefore the nonobviousness-type double patenting rejections based on Schneller are inappropriate to the instant application, as discussed below.

1. The Schneller inventions involve multiple bends in the same piece of wire while the present inventions are different combinations of different elements in different types of systems (Section 8.6.5.2).

2. The present application claims are independent or distinct from the copending claims (Section 8.4.2).

3. It contrast to Schneller, the instant application has ample justification for separate patents (Section 8.6.5.3).

4. In contrast to Schneller, the instant claims are not "covered" by the patent claims (Section 8.6.5.4).

5. It is contrary to Schneller to reject the instant claims over copending applications (Section 8.6.5.5).

8.6.5.2 Schneller's Invention Is A Unitary Device, A Single Piece Of Wire Having Five Bends

In Schneller, the applicant disclosed a single invention, a single unitary bent wire forming a clip. The invention was in the bends in the wire. The same preferred embodiment was claimed in the patent and was also claimed in the application (Section 8.6.4). Hence, additional claims in a second patent would extend Schneller's patent rights over the same preferred embodiment.

Conversely, the eight copending applications and the instant application disclose plural preferred embodiments (Section 8.6.4).

The facts in the instant application are thus very different from Schneller. In Schneller, a person practicing the only disclosed embodiment of the invention would infringe both the patent claims as well as the application claims. Thus, allowance of the application claims without a terminal disclaimer would extend the patent coverage of the only disclosed embodiment beyond 17 years, creating a so-called "unjustified timewise extension." Conversely, in the instant application a person could practice a disclosed embodiment without necessarily infringing both the instant claims and the claims of the copending applications. This is because of the multiple disclosed embodiments. This is also because the claims are independent or distinct (Section 8.4.2). Because of the disclosure of multiple embodiments and because the

claims are independent or distinct in the present case, there is no timewise—let alone an unjustified timewise—extension of patent rights.

8.6.5.3 The Present Case Has Ample Justification For Multiple Applications

In contrast to Schneller, the filing of the instant continuing application is justified. In Schneller, the Court several times expressed concern for a lack of any justification for the multiple applications. See e.g., 397 F.2d at 353, 158 USPQ at 214 ("There is, therefore, no direct indication before us why appellant chose this voluntary division method of claiming"); 397 F.2d at 355, 158 USPQ at 215 ("Neither do we have any requirement of restriction"). However, in contrast to Schneller, the present application has ample justification for the multiple patent applications.

First, the instant claims are independent or distinct from the copending claims (Section 8.4.2). Hence, presentation of the instant claims in the other applications would likely have resulted in a restriction requirement.

Second, the examiners in related applications restricted the claims (Section 8.4.1), informing the applicant therein (the Appellant herein) that claiming of additional distinct inventions would not be permitted in those applications.

Third, the patent and the application in Schneller had very few claims in contrast to the copending applications and the instant application in the present case which have many claims. The Schneller patent and application have 5 claims and 7 claims, respectively, while the eight copending applications and the instant application have over 500 claims. In view of the claims being

directed to independent or distinct inventions (Section 8.4.2), it is expected that examiners in the other applications would have objected to such a number of claims in the same application. In contrast, it is submitted that, in Schneller, the CCPA considered the grouping of the 5 patent claims and the 7 application claims into a single application to be a reasonable grouping.

Thus, in contrast to Schneller, there is ample justification for not grouping the instant claims with the claims in the copending applications. In light of these differences between the present application and the facts in Schneller, the holding in Schneller is inapplicable to the instant claims and the double patenting rejections based upon Schneller should therefore be reversed.

8.6.5.4 The Claims In The Instant Application Are Not "Covered" By The Copending Application Claims

The term "cover" in Schneller involves claiming the same preferred embodiment (Sections 8.6.4 and 8.6.5.4). The patent claims "cover" the preferred form ABCXY common to the patent and this application'.[96] In Schneller, the patent claims and the application claims were found to be directed to the "best mode" (the single preferred embodiment).[97] This does not apply in the present case because the instant application and the copending applications disclose numerous alternate embodiments. The CCPA did not offer any comments to suggest that the facts of Schneller could be broadened to the facts which exist in the instant application.

---

[96] 397 F.2d at 356, 158 USPQ at 216.

[97] 397 F.2d at 354, 158 USPQ at 214.

In Schneller, a product infringing the preferred embodiment ABCXY must infringe both the application claims and the patent claims. This is far from the present case. In the present case, the instant claims and the copending claims are not directed to a common preferred embodiment, hence the instant claims are not covered by the copending claims. The instant claims are clearly independent or distinct from the copending claims (Section 8.4.2). Hence, no form of double patenting, certainly not nonobviousness-type double patenting, applies to the present case and hence the Schneller-type double patenting rejections should be reversed.

8.6.5.5 It Is Contrary To Schneller To Reject The Instant Claims Over Copending Applications

Schneller deals with the filing of a continuing application years after the patent was issued. There is no basis in Schneller for rejecting the instant claims over copending applications.[98] The rejections offer no clarification of what in Schneller is relied upon to support such a unique interpretation.

In view of the above, the rejections of the instant claims for nonobviousness-type double patenting over the claims of copending applications are contradicted by the Schneller decision itself.

---

[98] MPEP 804 offers guidance as to the applicability of Schneller-type double patenting rejections to copending applications. Such guidance appears tenuous since Schneller does not provide for such a rejection and no legal basis is cited in the MPEP Schneller discussion.

8.6.6 Schneller Is Distinguished Pursuant To In Re Heinle

The Schneller decision distinguished Heinle[99] on the basis of distinctness because the combinations of the patent claims and the application claims in Heinle were "separately usable and salable" while the Schneller device was not separately salable and usable. As stated in Schneller:

> The issued patent (in Heinle) claimed a mechanical combination for holding a toilet paper roll. The application claimed a separately usable and salable element of that combination, a particular core for the roll. A combination claim does not "cover" or read on a single element. The protection of the combination afforded by the single Heinle patent claim would not have been extended by the application claims directed to the element.

Schneller.[100] As in Heinle, the system of the instant claims and the copending claims are combination claims, the systems of which are "separately usable and salable" (Exhibit-2). The instant claims are therefore independent or distinct from the copending claims and hence are distinguishable from Schneller and its holding, thus meriting the reversal of the double patenting rejections based upon Schneller.

---

[99] In re Heinle, 342 F.2d 1001, 145 USPQ 131 (CCPA 1965)

[100] 397 F.2d at 355, 158 USPQ at 215. (emphasis in original removed, emphasis added, citations omitted).

8.6.7 The Examiner Improperly Attempts To Support The Rejection With Uninformative Schneller Cliches

The Examiner does not support the nonobviousness-type double patenting rejections. Instead, the Examiner merely recites uninformative and conclusionary Schneller cliches (Final Action at 26-27). The Final Action does not develop the rejections nor explain why these cliches are applicable to the instant application. This is not surprising since the cliches are not applicable to the instant application, as discussed below.

The Final Action states that the subject matter of the application claims is fully disclosed in the copending application and is covered by any patent granted on the copending application and that there is no reason for not presenting the instant claims in the copending application. This is effectively all that the rejection states. Notwithstanding the fact that these cliches are wrong, as discussed below, reciting such cliches does not establish a prima facie case.

The fact that the subject matter of the application claims is fully disclosed in the copending application is not texticularly relevant to the nonobviousness-type double patenting rejection. Common disclosures are a basic characteristic of proper continuation and divisional applications. See 35 USC 120 and 35 USC 121.

The Examiner's contention that the subject matter of the application claims is covered by the claims of the copending application is unsupported and just plain wrong. This statement is in direct conflict with the plain words of Schneller. The "covered" terminology in

Schneller represents a best mode issue (Section 8.6.5.4), not a general cliche to be indiscriminately thrown about without qualification. The Examiner should have provided a limitation-by-limitation analysis, such as with a side-by-side claim chart, to show why he believes that the application claims are covered by the copending claims in accordance with Gechter (Section-8.4.4) and Graham (Section 8.9.2). Clearly, the instant claims are not covered by the copending claims.

The Examiner's contention that there is no reason for not presenting the application claims in the copending application conflicts with the facts of the instant application. The instant application has ample justification for being in a separate application (Section 8.6.5.3). For example, the rejections completely disregard the restriction requirements in the parent applications.

8.6.8 The Nonobviousness-Type Double Patenting Rejection Does Not Establish A Prima Facie Case

For the reasons discussed in Section 8.4.6 and for the additional reasons discussed below, the nonobviousness-type double patenting rejections do not establish a prima facie case.

1. The rejections do not address the independence or distinctness of the claims (Section 8.4.2)

2. The rejections improperly rely on unsupported conclusionary contentions.

3. The rejections ignore significant limitations recited in the claims (Section 8.4.3).

4. The rejections are based upon a discussion of the disclosure instead of the required limitation-by limitation comparison of the claims (Section 8.4.4).

5. The Examiner does not properly support the rejections (Section 8.6.7).

Because the instant claims are independent or distinct from the copending claims (Section 8.4.2), Schneller-type double patenting does not apply. 397 F.2d at 354, 158 USPQ at 214.

The rejections improperly rely on conclusionary, unsupported contentions, as discussed below.

The rejections are based upon the erroneous position that the instant claims are "covered" by the copending claims since the copending applications and the instant application are claiming common subject matter. However, the instant claims are not covered by the copending claims. There are significant differences between the compared claims (Section 8.4.3), but the rejections do not properly address the differences nor do they make any claim comparisons that are necessary to ascertain these differences. Hence, the rejections cannot and do not establish what is common subject matter nor that the instant claims are "covered" by the copending claims.

Further, the rejections do not even attempt to establish what is covered by the copending claims; the rejections do not attempt to explain why the instant claims are held to be covered by the copending claims, which have significantly different limitations; and the rejections do not attempt to explain how the systems claimed in the copending applications can "cover" the signifi-

cantly different system claimed in the instant application.

Further, the rejections ignore the significant limitations recited in the body of the claims. See, for example, Section 8.4.3 which addresses the significant differences between the instant claims and the copending claims. Clearly, a proper analysis of the instant claims and the copending claims confirms that there is no nonobviousness-type double patenting.

The rejections state that since the instant claims are fully disclosed in the copending application, the instant application and the copending application are claiming common subject matter. This is not correct. Claiming of common subject matter can only be determined by comparing the claims of the copending applications with the claims of the instant application. However, when such a comparison is made, it is apparent that the claimed subject matter in the instant application is significantly different from the subject matter claimed in the copending applications (Section 8.4.3).

In view of the above, the Schneller-type "nonobviousness" double patenting rejections do not establish a prima facie case. Hence, the Schneller-type "nonobviousness" double patenting rejections should be reversed.[101]

8.6.9 Conclusion

The law of double patenting requires a two-part test. This well-established law should not be changed by ignoring Vogel and adding a third test for double patenting based upon the overruled Schneller case. Neverthe-

---

[101] In re Oetiker, 977 F.2d 1443, 24 U.S.P.Q.2d 1443 (Fed. Cir. 1992).

less, the present claims would clearly satisfy a Schneller test for double patenting even if the Schneller test were to be added to the existing law. The Final Action, moreover, does not establish a prima facie case for double patenting under a Schneller analysis or any other analysis.

The nonobviousness-type double patenting rejections should be reversed for the reasons set forth above; a two-part test for double patenting has been established by Vogel; the Board should not ignore Vogel by creating a third test for double patenting; the present claims satisfy the overruled Schneller inquiries for double patenting; Schneller only applies where the patent claims and the application claims are directed to the same preferred embodiment; the facts in the instant application are significantly different from the facts of Schneller; Schneller's invention is a unitary device, a single piece of wire having five bends; the present case has ample justification for multiple applications; the claims in the instant application are not "covered" by the copending application claims; it is contrary to Schnellner to reject the instant claims over-copending applications; Schneller is distinguished pursuant to Heinle; the Examiner does not properly support the rejection; the nonobviousness-type double patenting rejections do not establish a prima facie case; and for the additional reasons set forth in Section 8.4.7.

8.7 ARGUMENTS COMMON TO BOTH THE 35 USC 102 ANTICIPATION REJECTION AND THE 35 USC 103 OBVIOUSNESS REJECTION

Claims 22, 23, 82-84, 95, 99, 137, and 138 stand rejected under 35 USC 102 ("'102") regarding anticipation and claims 19, 25, 96, 100, 101, 140, and 135 stand re-

jected under 35 USC 103 ("'103") regarding obviousness. The arguments common to both the '102 anticipation rejections and the '103 obviousness rejection are set forth in this Section 8.7. The arguments primarily related to the '102 anticipation rejection are set forth in Section 8.8 to supplement the arguments set forth in this Section 8.7. The arguments primarily related to the '103 obviousness rejection are set forth in Section 8.9 to supplement the arguments set forth in this Section 8.7.

The art rejections do not, and in fact cannot,[102] establish a prima facie case of either anticipation or obviousness.

The Appellant respectfully traverses the art rejections for the reasons discussed in Sections 8.7.1 et seq, 8.8, and 8.9.

8.7.1 The Art Rejections Do Not Even Provide Claim-By-Claim Analysis, Much Less Ths Limitation-By-Limitation Analysis, Required By The Federal Circuit

The Federal Circuit requires that art rejections be supported on a limitation-by-limitation basis with specific fact findings for each contested limitation and satisfactory explanations for such findings. The claim construction used in contesting the limitations must also be explicit. The Federal Circuit also requires fact findings, adequately explained, for each relevant factor.[103] However, the instant art rejections fail to meet these requirements. The art rejections do not even provide a

---

[102] The Examiner cannot establish a prima facie case of either anticipation or obviousness because the prior art references do not anticipate the claims nor render the claims obvious.

[103] Gechter v. Davidson, 43 USFQ2d 1030, 1035 (Fed. Cir. 1997).

claim-by-claim analysis, much less the required limitation-by-limitation analysis. The Gechter decision outlining the analytical requirements for a proper rejection followed closely on the heels of the Supreme Court decision in Warner-Jenkinson[104] affirming the requirement for an limitation-by-limitation analysis in defining the scope of a patented invention in infringement analyses.

In addition, the CCPA, in reversing a prior art rejection, ruled that all words in a claim must be considered in evaluating patent ability regarding the prior art.

> In this respect, the section 102 rejection in this case is not unlike the section 103 rejection which we reversed in In re Wilson, 57 CCPA 1029, 4.24 F.2d 1382, 165 USPQ 494 (1970), and is unsupportable for the same reason: "All words in a claim must be considered in judging the patent ability of that claim against the prior art" (emphasis added). Id. at 1032, 424 F.2d at 1385, 165 USPQ at 496.

Miller[105] (emphasis in original).

In violation of the aforementioned black letter law, the Examiner did not even consider all claims much less all words, elements, and limitations in the claims. Hence, the Examiner violated Gechter and Warner-Jenkinson by failing to support the art rejections on a claim-by-claim basis, much less on the required limitation-by-limitation basis.

Still further, the Examiner merely identified elements in the references upon which certain claim ele-

---

[104] Warner-Jenkinson Co. v. Hilton Davis Chemical Co., 117 S. Ct. 1040, 41 USPQ2d 1865 (1997).

[105] In re Miller, 441 F.2d 689, 169 USPQ 597 (CCPA 1971).

ments allegedly read. The Examiner did not make any specific fact findings for each contested limitation, nor provide a satisfactory explanation, nor explain the claim construction used in contesting the limitations as required by Gechter. The Examiner did not even acknowledge that the limitations in the claims have different names and functions than the elements with which they are compared. The Examiner did not perform a Gechter analysis on a single claim. The court in Gechter commented that if claim construction is not explicit or if the claims were misconstrued, a finding of anticipation must be reversed. 43 USPQ2d at 1033. The claims must first have been correctly construed to define the scope and meaning of each contested limitation. See also Paulsen.[106] The Court in Paulsen commented that in order to properly compare a reference with the claims, it is necessary to construe the contested term to ascertain its scope and meaning. Id. at 1674.

The court in Gechter further commented that the PTO must expressly find that every limitation in the claim was identically shown in the single reference. 43 USPQ2d at 1035. Such findings should provide an explanation for whether, how, and why the reference contains each of the limitations of the claim. Thus, said the court, the explanation should define the exact function of the elements as well as find that the prior art reference disclosed the identical function.

Further, the Examiner is required to consider the scope and meaning of the limitations used in the claims; i.e., construe each claim limitation. However, the Exam-

---

[106] In re Paulsen, 30 F.2d 1475, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994).

iner does not do what Gechter and Paulsen require for determining the scope and meaning of the contested limitations.

In direct violation of Gechter, other court precedent, and the PTO's rules; the Examiner disregards important claim limitations, has not supported the art rejections on a limitation-by-limitation basis with specific fact findings for each contested limitation and satisfactory explanations for such findings, has not explicitly explained the claim construction used in contesting the limitations and has not supported the art rejections with adequately explained fact findings for each relevant factor. This is not surprising since such analyses would have confirmed that the claims distinguish over the references and the Examiner would not have been able to persist in the art rejections.

In view of the above, the Examiner has not provided a Gechter analysis in support of the art rejections because a Gechter analysis would show that the claims distinguish over the references. Hence, the art rejections should be reversed.

8.7.2 The Present Examiner Was Previously Reversed By The Board For Similarly Improper Rejections

The same examiner who issued the Final rejection in the instant application has been reversed by the Board for similarly improper art rejections in two other patent applications of the present Appellant.[107]

---

[107] Ex parte Hyatt, Appeal No. 93-2572, Paper No. 31 in patent application Serial No. 07/515,886 which issued as U.S. Patent No. 5,398,041 on March 14, 1995 (Bd. Pat. App. & Int. March 24, 1994) [herein Hyatt-'886] (unpublished PTO decision).

Ex parte Hyatt, Appeal No. 93-2573, Paper No. 28 in patent applica-

As in the instant application (Section 8.9.3), the same examiner involved in the Hyatt-'886 appeal relied on disparate references. However, the Board reversed the '103 rejection over those disparate references. Judge Hairston stated:

> In the absence of a convincing reason for combining the teachings of such disparate display teachings, we will reverse the 35 U.S.C. 103 rejection of claims 42 and 43.

Hyatt-'886 at 6.

As in the instant application (Section 8.9.1), the same examiner involved in the Hyatt-'881 appeal relied on improper hindsight. However, the Board reversed the '103 rejection for improper hindsight. Judge Hairston stated:

> The only teaching of separate heat removal for each liquid crystal display is appellant's teaching, and that teaching is not available to the examiner. Accordingly, the 35 U.S.C. 103 rejection of claims 20 through 26 is reversed.

Hyatt-'881 at 6.

8.7.3 The Art Rejections Do Not Establish A Prima Facie Case

The art rejections do not establish a prima facie case[108], as discussed below.

---

tion Serial No. 07/515,881 which issued as U.S. Patent No. 5,432,526 on July 11, 1995 (Bd. Pat. App. & Int. March 24, 1994) [herein Hyatt-'881] (unpublished PTO decision).

[108] See 37 CFR 1.106(b); Chester v. Miller, 906 F.2d 1574, 1578, 15 USPQ2d 1333, 1337 (Fed. Cir. 1990) ("Section 132 is violated when a

a. The art rejections do not consider the claims as a whole.

b. The art rejections do not consider the references as a whole.

c. The art rejections do not consider the scope and content of the prior art.

d. The references do not teach or even suggest all the claim limitations.

e. The art rejections disregard relevant claim limitations (Sections 8.8.2 and 8.9.3 and Exhibit-3).

f. Discussing of broad claims does not establish anticipation or obviousness for the other claims.

g. The Federal Circuit requires a limitation-by limitation analysis, but the art rejections do not even provide a claim-by-claim analysis.

h. The Appellant properly traversed the Examiner's unsupported statements, but the Examiner did not provide the required reference or affidavit in accordance with MPEP 2144.03.

i. The art rejections do not address references that are non-analogous.

Judge Fleming in Hyatt-'041[109] stated:

---

rejection is so uninformative that it prevents the applicant from recognizing and seeking to counter the grounds for rejection."). See also In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992).

[109] Ex Parte Hyatt, Appeal No. 94-4132, Paper No. 28 at 4 in patent application Serial No. 07/578,041 which issued as U.S. Patent NO. 5,526,506 on June 11, 1996 (Bd. Pat. App. & Int. October 31, 1995) [herein Hyatt-'041] (unpublished PTO decision).

OPINION

We will not sustain the rejection of claims 1 through 76 under U.S.C. 103.

The Examiner has failed to set forth a prima facie case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the reasonable teachings or suggestions found in the prior art, or by a reasonable inference to the artisan contained in such teachings or suggestions. In re Sernaker, 702 F.2d 989, 217 USPQ 1 (Fed. Cir. 1983).

The burden of establishing a prima facie case is not satisfied by a mere matching up of elements in a reference with those in a claim. See Hyatt-'041 (overturning a rejection which matched up a claimed detector with a prior art decoder). See also Edwards and Oetiker.[110]

The claims are all rejected together as groups of claims. This is improper. In order to establish a prima facie case, each claim must be evaluated individually to determine whether the individual claim is anticipated or rendered obvious by the references, particularly where, as here, the distinctions of the claims are separately argued (e.g., Sections VII, 8.8.2, and 8.9.3). Since the Examiner did not evaluate the claims individually, the art rejections are improper for failing to establish a

---

[110] In re Edwards, 568 F.2d 1349, 1354, 196 USPQ 465, 469 (CCPA 1978); In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992).

prima facie case. See also Van Geuns and Wright.[111] See also Nielson and Beaver.[112]

The art rejections do not properly acknowledge that different claims in the instant application recite different combinations of features than taught by the references, much less read these different combinations of features on the references.

The Examiner admits that there are differences between the claims and the references (Final Action at 28-29). See also Sections VII, 8.8.2, and 8.9.3 for discussions of the differences. However, the art rejections do not properly analyze the differences acknowledged by the Examiner.

Vice Chief Judge Harkcom in Hyatt-'061[113] stated:

> The examiner implies that the recited memory is well known in the memory art but provides no documentation of this despite a challenge from Appellant. Examiner's Answer at 14, lines 2-5; Appeal Brief at 10, lines 18-32. Without such support we will not sustain the rejection on the present record.
>
> * * *

---

[111] In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993); In re Wright, 999 F.2d 1557, 27 USPQ2d 1510 (Fed. Cir. 1993).

[112] In re Nielson, 816 F.2d 1567, 2 USPQ2d 1525 (Fed. Cir. 1987); In re Beaver, 893 F.2d 329, 13 USPQ2d 1409 (Fed. Cir. 1989).

[113] Ex parte Hyatt, Appeal No. 94-0665, Paper No. 28 at 17, 19, and 22-23 in patent application Serial No. 07/493,061 (Bd. Pat. App. & Int. June 30, 1998) [herein Hyatt-'061] (unpublished PTO decision) (emphasis added).

> This rejection hinges on the examiner's finding that analog refresh circuits were well known in the art. Appellant has challenged that finding and the examiner has not supported the finding with any evidence in the present record. Lacking such support, we are constrained to reverse the rejection. Thus, the rejection of Claim 63 is not sustained on the present record.
>
> * * *
>
> This rejection hinges on the examiner's finding that analog refresh circuits were well known in the art. Appellant has challenged that finding and the examiner has not supported the finding with any evidence in the present record. Lacking such support, we are constrained to reverse the rejection. Thus, the rejection of Claims 5, 6, 8, 10, 12, 13, 15, 16, 26-28, 40, 41, 43, 45, 47, 50, 61, and 62 is not sustained on the present record.

Judge Lee in Hyatt-'570[114] stated:

> We disagree with the examiner . . . . The examiner's conclusion is without adequate support in the record.

For this and other reasons, the Board reversed the '103 rejection of claims 9 and 13. Hyatt-'570 at 27-32. As in Hyatt-'570, in the instant application "[t]he examiner's conclusion is without adequate support in the record." Hence, the instant '103 rejection should be reversed.

---

[114] Ex parte Hyatt, Appeal No. 95-4759, Paper No. 30 at 29 in patent application Serial No. 07/357,570 (Bd. Pat. App. & Int. September 25, 1996) [herein Hyatt-'570] (unpublished PTO decision).

Judge Lee in Hyatt-'570[115] further stated:

> Without explaining how one would arrive at the particular structure required by the claims, the examiner has not made out a prima facie case that the claimed invention would have been rendered obvious by the prior art.

Judge Krass in Hyatt-'243[116], in reversing all of the rejections under 35 USC 102 and 35 USC 103, stated:

> The examiner's approach appears to suggest that the generation of one certain frequency means that there is suppression of other frequencies and that somehow this equates to filter processing. In our view, the examiner's interpretation is a stretch which goes beyond all bounds of reasonableness.

In view of the above, the art rejections do not establish a prima facie case. Hence, the art rejections should be reversed.[117]

8.7.5 Conclusion

The art rejections should be reversed for the reasons set forth above; the art rejections do not even provide a claim-by claim analysis, much less the limitation-by-limitation analysis required by the Federal Circuit; the present Examiner was previously reversed by the

---

[115] Ex parte Hyatt, Appeal No. 95-4759, Paper No. 30 at 45 in patent application Serial No. 07/357,570 (Bd. Pat. App. & Int. September 25, 1996) [herein Hyatt-'570] (unpublished PTO decision).

[116] Ex Parte Hyatt, Appeal No. 92-1284, Paper No. 66 at 4-5 in patent application Serial No. 07/849,243 which issued as U.S. Patent No. 5,410,621 on April 25, 1995 (Bd. Pat. App. & Int. May 17, 1994) [herein Hyatt-'243] (unpublished PTO decision).

[117] In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992).

Board for similarly improper rejections; and the art rejections do not establish a prima facie case.

8.8.1 35 USC 102 ANTICIPATION REJECTION

Claims 22, 23, 82-84, 95, 99, 137, and 138 stand rejected under 35 USC 102 ("'102") for anticipation. The Appellant respectfully traverses the '102 rejection for the reasons discussed in Sections 8.7 and 8.8.1 et seq.

8.8. The '102 Rejection Does Not Provide The Identity Required By The Federal Circuit

The law of the Federal Circuit requires identity between the rejected claims and the reference in order to support a '102 rejection. However, the Examiner has not established this identity for the '102 rejection. This is not surprising considering that there is no such identity to be found. The claims set forth clear and distinct limitations that distinguish over the reference (e.g., Section 8.8.2).

The Examiner alleges correspondence between some claim elements and elements shown in the reference. However, allegations of correspondence between claimed elements is no substitute for a proper showing of identity.

A party asserting that a patent claim is anticipated under '102 must demonstrate, among other things, identity of invention. See Kalman.[118] See also SRI.[119] Identity of invention is a question of fact—one who seeks

---

[118] Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 771, 218 USPQ 781, 789 (Fed. Cir. 1983), cert. denied, 465 U.S. 1026, 224 USPQ 520 (1984), overruled in part on another ground.

[119] SRI Int'l v. Matsushita Elec. Corp. of Am., 775 F.2d 1107, 1125, 227 USPQ 577, 588-89 (Fed. Cir. 1985) (in banc).

such a finding must show that each element of the claim in issue is found, either expressly or under principles of inherency, in a single prior art reference, or that the claimed invention was previously known or embodied in a single prior art device or practice. See Minnesota.[120] The reference must describe the claimed invention sufficiently to have placed a person of ordinary skill in the field of the invention in possession of it. See Spada.[121]

The Federal Circuit further requires for a finding of anticipation that the same arrangement be literally present in the claim as it is in the reference and be shown in as complete detail as in the claim.

> The district court correctly instructed the jury that an invention is anticipated if the same device, including all the claim limitations, is shown in a single prior art reference. Every element of the claimed invention must be literally present, arranged as in the claim. Perkin-Elmer Corp., 732 F.2d at 894, 221 USPQ at 673; Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 771-72, 218 USPQ 781, 789 (Fed. Cir. 1983), cert. denied, 465 U.S. 1026 [224 USPQ 520] (1984). The identical invention must be shown in as complete detail as is contained in the patent claim. Jamesbury Corp., 756 F.2d at 1560, 225 USPQ at 256; Connell, 722 F.2d at 1548, 220 USPQ at 198.

---

[120] Minnesota Mining and Manufacturing v. Johnson & Johnson, 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992).

[121] In re Spada, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990).

Richardson[122] (emphasis added). Hence, the required identity must also consider the recited coupling and the recited responsiveness in the claims.

Judge Smith in Hyatt-'430[123], in reversing the rejection under 35 USC 102, stated:

> There can be many different structures which carry out identical functions, and these different structures do not automatically anticipate each other within the meaning of 35 U.S.C. 102.

In view of the above, the instant claims do not have identity with the reference applied in the '102 rejection. Hence, the '102 rejection should be reversed.

8.8.2 The '102 Rejection Overlooks The Many Novel Differences Between The Instant Claims And The References

There are many novel differences between the instant claims and the references. The Examiner even admits to differences (Final Action at 25 and 27). Nevertheless, even though the arguments herein establish significant novel claim differences, the Examiner has not even attempted to reconcile these differences, much less to read each contested instant claim on each applied reference, nor to read the contested claim limitations on

---

[122] Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), cert. denied, 110 S.Ct. 154 (1989),

[123] Ex Parte Hyatt, Appeal No. 95-2551, Paper No. 27 at 8-9 in patent application Serial No. 07/468,430 which issued as U.S. Patent No. 5,594,980 on January 14, 1997 (Bd. Pat. App. & Int. May 22, 1996) [herein Hyatt-'430] (unpublished PTO decision).

the applied references, nor to provide the required Gechter[124] and Graham[125] analyses.

Further, the novel combination of elements for each instant apparatus claim and the novel combination of acts for each instant process claim are set forth in Exhibit-3.[126] Because the "'ing" verb' (e.g., generating, storing, etc.)[127] limitations in the apparatus claims are similar to the "'ing" verb' limitations set forth in corresponding process claims, the "'ing" verb' limitations are not repeated for the apparatus claims in Exhibit-3. The novel combinations of contested limitations shown in Exhibit-3 illustrate the significant novel differences between the instant claims and the references.

Further, each apparatus claim and each process claim recites novel combinations of responsive[128] limitations in addition to the novel combination of elements and novel combination of "'ing" verb' limitations. Because these responsive limitations are clearly set forth in the Appendix and are related to the novel combinations, it is not necessary to separately set forth these

---

[124] Gechter v. Davidson, 116 F.3d 1454, 43 USPQ2d 1030 (Fed. Cir. 1997).

[125] Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966).

[126] For simplicity of illustration, the combination shown for each dependent claim recites the parent claim number as being representative of the combination of elements or acts listed for the parent claim and intended to be further combined with the elements or acts listed for the dependent claim.

[127] The Federal Circuit uses the term "'ing" verb' (passing, heating, reacting, transferring, etc.) in its discussion in O.I. Corp. v. Tekmar, 115 F.3d 1576, 42 USPQ2d 1777 (Fed. Cir. 1997).

[128] E.g., "in response to . . .".

responsive limitations. However, the Appellant will set forth a separate combination of these responsive limitations if requested by the Examiner in the Answer.

Further, each apparatus claim has a novel combination of coupling limitations in addition to the novel combination of elements, novel combination of '"ing" verb' limitations, and novel combination of responsive limitations. Because these coupling limitations are clearly set forth in the Appendix and are related to the combinations of contested limitations set forth in Exhibit-3, it is not necessary to separately set forth these coupling limitations. However, the Appellant will set forth a separate combination of these coupling limitations if requested by the Examiner in the Answer.

The recited elements, '"ing" verb' limitations, responsiveness limitations, coupling limitations, and combinations thereof all constitute contested limitations.

Further, the Examiner alleges lack of disclosure of terminology that in fact has hundreds of occurrences in the disclosure (Section 8.1.5 and Table-1), yet the Examiner alleges full anticipation of claim terminology that is not disclosed by the references (Section 8.8.2).

The claims rejected over Hill under '102 have novel distinctions thereover. Representative limitations that distinguish over Hill are excerpted from the claims and are set forth below.[129]

22. A memory system comprising:

---

[129] Important limitations; such as coupling, responsiveness, and elements of the combination; are not included in the excerpts for brevity. However, these other limitations are also contested limitations (e.g., Exhibit-3).

an image input circuit generating input image information;

a two dimensional frame buffer storing a frame of image information, the frame of image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

an address generator generating write addresses and generating read addresses;

a frame buffer writing circuit coupled to the image input circuit, coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer writing circuit writing the frame of image information into the two dimensional frame buffer in response to the input image information generated by the image input circuit and in response to the write addresses generated by the address generator;

a frame buffer accessing circuit coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer accessing circuit accessing blocks of pixel image information in response to the read addresses generated by the address generator;

a two dimensional processor coupled to the frame buffer accessing circuit and generating two dimensional output processed image information in response to the blocks of pixel image information accessed by the frame buffer accessing circuit; and

an output circuit coupled to the two dimensional processor and generating output image information in response to the two dimensional output processed

image information generated by the two dimensional processor.

23. A memory system comprising:

an image input circuit generating input image information;

a two dimensional pixel block memory storing a two dimensional array of blocks of pixel image information, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

an address generator generating write addresses and generating read addresses;

a pixel block memory writing circuit coupled to the image input circuit, coupled to the two dimensional pixel block memory and coupled to the address generator, the pixel block memory writing circuit writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory in response to the input image information generated by the image input circuit and in response to the write addresses generated by the address generator;

a pixel block memory accessing circuit coupled to the two dimensional pixel block memory and coupled to the address generator, the pixel block memory accessing circuit accessing blocks of pixel image information in response to the read addresses generated by the address generator;

a two dimensional processor coupled to the pixel block memory accessing circuit and generating two

dimensional output processed image information in response to the blocks of pixel image information accessed by the pixel block memory accessing circuit; and

an output circuit coupled to the two dimensional processor and generating output image information in response to the two dimensional output processed image information generated by the two dimensional processor.

82. A process of operating a memory system comprising the acts of:

generating input image information;

storing a two dimensional array of blocks of pixel image information by a two dimensional pixel block memory, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

generating write addresses and generating read addresses;

writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory in response to the input image information and in response to the write addresses;

generating a first clock signal having a first clock rate;

accessing blocks of pixel image information from the two dimensional frame buffer in response to the read addresses, wherein the accessing of blocks of pixel image information from the two dimensional frame

buffer is at a first information rate in response to the first clock signal;

generating two dimensional processed image information in response to the accessed blocks of pixel image information;

generating a second clock signal having a second clock rate that is different than the first clock rate of the first clock signal; and generating output image information in response to the two dimensional processed image information, wherein the generation of the output image information is at a different information rate than the first information rate in response to the second clock signal.

83. A process of operating a memory system comprising the acts of:

generating input image information;

storing a frame of image information by a two dimensional frame buffer, the frame of image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

generating write addresses and generating read addresses;

writing the frame of image information into the two dimensional frame buffer in response to the input image information and in response to the write addresses;

accessing blocks of pixel image information from the two dimensional frame buffer in response to the read addresses;

generating two dimensional processed image information in response to the accessed blocks of pixel image information; and

generating output image information in response to the two dimensional processed image information.

84. A process of operating a memory system comprising the acts of:

generating input image information;

storing a two dimensional array of blocks of pixel image information by a two dimensional pixel block memory, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

generating write addresses and generating read addresses;

writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory in response to the input image information and in response to the write addresses;

accessing blocks of pixel image information from the two dimensional pixel block memory in response to the read addresses;

generating two dimensional processed image information in response to the accessed blocks of pixel image information; and

generating output image information in response to the two dimensional processed image information.

95. A process of operating a memory system comprising the acts of:

generating input image information;

storing a two dimensional array of blocks of pixel image information in a two dimensional pixel block image memory in response to the input image information, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

generating read addresses;

accessing blocks of pixel image information from the two dimensional pixel block image memory in response to the read addresses;

generating output image information in response to the accessed blocks of pixel image information; and

storing buffered output image information by a buffer memory in response to the output image information.

99. A process of operating a memory system comprising the acts of:

generating input image information at a first information rate;

storing a two dimensional array of blocks of pixel image information in a two dimensional pixel block memory in response to the input image information, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

generating read addresses;

accessing blocks of pixel image information in response to the read addresses;

generating output processed image information in response to the accessed blocks of pixel image information;

generating output image information in response to the output processed image information; and

outputting the output image information at a second information rate that is greater than the first information rate.

137. A memory system as set forth in claim 22, further comprising:

a display coupled to the output circuit and displaying an image in response to the output image information generated by the output circuit.

138. A memory system as set forth in claim 23, further comprising:

a display coupled to the output circuit and displaying an image in response to the output image information generated by the output circuit.

In view of the above, the instant claims have significant novel differences that are not anticipated by the reference. Hence, the '102 rejection should be reversed.

8.8.3 The 102 Rejection Does Not Establish A Prima Facie Case

The 35 USC 102 rejection does not establish a prima facie case for the reasons discussed in Section 8.7.3 and for the additional reasons outlined below.

The Examiner must support art rejections with a proper explanation of why the claims are anticipated by

the reference. Such support of the art rejections requires, as stated above, an evaluation of the claims as a whole, the references as a whole, a proper construction of each of the claims to determine their scope and meaning, a limitation-by-limitation analysis of each claim element, a claim-by-claim analysis of each of the claims subject to rejection and consideration of all of the words in each claim.

The prima facie case, for purposes of anticipation, requires that the anticipation analysis be conducted on a limitation-by limitation basis with specific fact findings for each limitation and an explanation for the findings, as well as explicit claim construction. See Gechter.[130] It is well-established that identity of invention is required for anticipation. This means that every limitation in the claim must be identically shown in a single reference. Identity of invention also requires identity of function. Failure to meet these basic criteria, as in the instant case, constitutes a failure to establish a prima face case of anticipation.

In view of the above, the '102 rejection does not establish a prima facie case. Hence, the '102 rejection should be reversed.[131]

8.8.4 Conclusion

The 35 USC 102 rejection should be reversed for the reasons set forth above; the '102 rejection does not provide the identity required by the Federal Circuit; the

---

[130] Gechter v. Davidson, 116 F.3d 1454, 43 USPQ2d 1030 (Fed. Cir. 1997).

[131] In re Oetiker, 977 F.2d 1443, 24 U.S.P.Q.2d 1443 (Fed. Cir. 1992).

'102 rejection overlooks the many novel differences between the instant claims and the references; and the '102 rejection does not establish a prima facie case; and for the additional reasons set forth in Section 8.7.

8.9 35 USC 103 OBVIOUSNESS REJECTION

Claims 19, 25, 96, 100, 101, 140, and 135 stand rejected under 35 USC 103 ("'103") for obviousness. The Appellant respectfully traverses the '103 rejection for the reasons discussed in Sections 8.7 and 8.9.1 et seq.

8.9.1 The '103 Rejection Relies Upon Improper Hindsight

The 35 USC 103 rejection relies on improper hindsight. This reliance is fatal to the '103 rejection.

> It is difficult but necessary that the decision maker forget what he or she has been taught . . . about the claimed invention and cast the mind back to the time the invention was made (often as here many years), to occupy the mind of one skilled in the art who is presented only with the references, and who is normally guided by the then-accepted wisdom in the art. W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

MPEP 2141.01. The Examiner must ascertain what would have been obvious to an artisan at the time the invention was made, and not to a layman. See MPEP 2141.03. See also the Supreme Court decision in Webster[132] (Section 8.2.3).

---

[132] Webster Loom Co. v. Higgins, 105 U.S. 580 (1881).

The prior art references themselves must suggest the desirability and thus the obviousness of making the combination without the slightest recourse to the teachings of the application. More specifically, the court in Amgen[133] stated that "Both the suggestion and the expectation of success must be founded in the prior art, not in applicant's disclosure." The court said that hindsight is not a justifiable basis on which to find obviousness. Id. at 1023. See also Heidelberiter.[134]

> When the patented invention is made by combining known components to achieve a new system, the prior art must provide a suggestion or motivation to make such a combination.

Obviousness is tested by what the combined teachings of the references would have suggested to an artisan. Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. The Examiner cannot rely upon hindsight.

> "To imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher." . . . It is essential that "the decision maker forget what he

---

[133] Amgen, Inc. v. Chugai Pharmaceutical Co., Ltd., 927 F.2d 1200, 1207, 18 USPQ2d 1016, 1022 (Fed. Cir. 1991).

[134] Heidelberger Druckmaschinen AG v. Hantscho Commercial Products Inc., 21 F.3d 1068, 1072, 30 USPQ2d 1377, 1379 (Fed. Cir. 1994).

> or she has been taught at trial about the claimed invention and cast the mind back to the time the invention was made . . . to occupy the mind of one skilled in the art who is presented only with the references, and who is normally guided by the then-accepted wisdom in the art." . . . One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.

Fine.[135]

Vice Chief Judge Harkcom in Hyatt-'061[136] stated:

> The mere fact that the prior art may be modified in the manner suggested by the examiner does not make the modification obvious under '103 unless the prior art suggested the desirability of the modification. In re Fritch, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992).

The claimed invention cannot be used as an instruction manual or template to piece together the teachings of the prior art so that the claimed invention is rendered obvious. See Fritch.

Judge Hairston in Hyatt-'881[137] stated:

---

[135] In re Fine, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988) (emphasis added) (citations omitted).

[136] Ex parte Hyatt, Appeal No. 94-0655, Paper No. 28 at 15 in patent application Serial No. 07/493,061 (Bd. Pat. App. & Int. June 30, 1998) [herein Hyatt-'061] (unpublished PTO decision).

[137] Ex parte Hyatt, Appeal No. 93-2573, Paper No. 28 at 6 in patent application Serial No. 07/515,881 which issued as U.S. Patent No. 5,432,526 on July 11, 1995 (Bd. Pat. App. & Int. March 24, 1994) [herein Hyatt-'881] (unpublished PTO decision). (emphasis added).

> The only teaching of separate heat removal for each liquid crystal display is appellant's teaching, and that teaching is not available to the examiner. Accordingly, the 35 U.S.C. 103 rejection of claims 20 through 26 is reversed.

Judge Lee in Hyatt-'570[138] stated:

> Additionally, the teachings of Fleming and Heilmeier are not readily combinable in the manner as suggested by the examiner for a separate and independent reason . . . . In that regard, the examiner provided no explanation as to why one with ordinary skill would have expected a reasonable certainty of success when using Heilmeier's liquid crystal device to simulate a turning "off" of Fleming's light.
>
> * * *
>
> In light of the foregoing, we conclude that the examiner has not demonstrated reasonable motivation, without application of hindsight, for one with ordinary skill in the art to combine the teachings of Heilmeier and Fleming in the manner as proposed by the examiner. Even assuming that the mental twist of turning a light "off" by leaving it "on" is within the scope of common sense and rudimentary skill, it only would have been just obvious to try the suggestion proposed by the examiner without having the required reasonable certainty of success. "Obvious to try" without reasonable expectation of success is in-

---

[138] Ex parte Hyatt, Appeal No. 95-4759, Paper No. 30 at 30-32 in patent application Serial No. 07/357,570 (Bd. Pat. App. & Int. September 25, 1996) [herein Hyatt-'570] (unpublished PTO decision) (emphasis added).

sufficient to render a claimed invention obvious under 35 U.S.C. 103. See, e.g., In re Eli Lilly & Co., 902 F.2d 943, 945, 14 USPQ2d 1741, 1743 (Fed. Cir. 1990); In re O'Farrell, 853 F.2d 894, 903, 7 USPQ2d 1673, 1681 (Fed. Cir. 1988).

Judge Lee in Hyatt-'570[139] further stated:

> Additionally, the rejection is improper for another reason. The appellant has not simply claimed using a liquid crystal device to regulate the output illumination from a source to provide a range of responses. The claimed invention is more specific. The examiner does not adequately explain why the particular structural arrangement required by claims 71 and 81 would have been rendered obvious by Stevens and Heilmeier.
>
> How would the liquid crystal device fit into a system such as that disclosed by Stevens? Which component would it replace? How would it be connected? How would a comparator such as that allegedly disclosed in Mengert fit into a system such as that disclosed by Stevens? Which component would it replace, if any, and why? How would it be connected? The examiner provides no answer to these questions. . . .
>
> Without explaining how one would arrive at the particular structure required by the claims, the examiner has not made out a prima facie case that the claimed invention would have been rendered obvious by the prior art.

---

[139] Ex parte Hyatt, Appeal No. 95-4759, Paper No. 30 in patent application Serial No. 07/357,570 (Bd. Pat. App. & Int. September 25, 1996) [herein Hyatt-'570] (unpublished PTO decision).

Hyatt-'570 at 44-45 (emphasis added). For these and other reasons, the Board reversed the rejection of claims 71 and 81. Hyatt-'570 at 42-47. As in Hyatt-'570, in the instant application "[t]he examiner provides no answer to these questions." Hence, the instant '103 rejection should be reversed.

Lunsford[140] made clear that the law on obviousness requires an evaluation of the differences between the claimed invention and the prior art. The court in Lunsford stated that it is not realistic

> to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art.

Id. at 726. The PTO must consider the references as a whole.

The Federal Circuit, in the recently decided case of In re Rouffet, ___ F.3d ___, 47 USPQ2d 1453 (Fed. Cir. 1998), provided revealing guidance regarding motivation and hindsight in evaluating obviousness. More particularly, the court found that the Board committed reversible error in determining that simply having a high level of skill in the art would have been motivated to combine references in a manner that rendered the claimed invention obvious. The court said that the examiner must show a motivation to combine the references that creates the case of obviousness (i.e., the examiner must show reasons why the skilled artisan would select the elements from the references for combination in the

---

[140] In re Lunsford, 357 F.2d 385, 148 USPQ 721 (CCPA 1966).

manner claimed). The court made clear that it was reversible error to simply invoke the high level of skill in the field of art to show motivation without some explanation of the principle that suggests the claimed combination. Thus, the Federal Circuit forbids the use of hindsight in the selection of references that comprise the case of obviousness and concludes that there can be no prima facie case without a showing of motivation. Where, as here, the Examiner, with knowledge of the Appellant's invention, has picked and chosen a combination of references without expressing any motivation for doing so, it is the consummate example of improper hindsight.

In view of the above, the '103 rejection relies upon improper hindsight. Hence, the '103 rejection should be reversed.

8.9.2 The '103 Rejection Does Not Perform The Required Graham Analysis

The starting point of any '103 analysis is the Supreme Court's decision in Graham v. Deere.[141] The Supreme Court in Graham focused on the procedural steps necessary to establish a factual basis for a rejection under section 103 and held that an examiner must evaluate (1) the scope and content of the prior art, (2) the differences between the prior art and the claims at issue, and (3) the level of ordinary skill in the art. Secondary considerations such as commercial success, long felt but unsolved needs, failure of others, etc. may have relevancy as indicia of obviousness or nonobviousness. The instant '103 rejection, however, fails to provide this required Graham analysis.

---

[141] Graham v. Deere, 383 U.S. 1, 148 USPQ 459 (1966).

Further, in Gechter the Federal Circuit stated that it expects an obviousness analysis to be conducted on a limitation-by-limitation basis, with specific fact findings for each limitation and claim construction must be explicit. (Section 8.7.1). However, the '103 rejection also fails to provide this required Gechter analysis.

The Board in Horton[142] reflected the position now clarified by the Federal Circuit in Gechter. In Horton, the Board found that the analysis performed by the examiner was insufficient to make out a case for anticipation or obviousness:

> We find that Horton has failed to present an appropriate analysis of the prior art reference vis-a-vis the claimed subject matter which would be sufficient to make out a case for anticipation or obviousness. There is little explanation in the Horton brief to provide adequate factual support for the conclusory statements set forth therein. If Horton considered the subject matter of any Stevens claim to have been anticipated or rendered obvious by Levendusky, he should have analyzed the reference in detail in accordance with the guidelines set forth in Graham v. John Deere Co., ... Specifically, he should have separately addressed each claim limitation in explaining where in the reference relevant subject matter is disclosed, what the differences are, and why the claimed invention as a whole would have been obvious to a person having ordinary skill in the art. Horton did not do this.

Id. at 1246. The Board went on to list the limitations which were not separately addressed. The Board stated

---

[142] Horton v. Stevens, 7 USPQ2d 1245 (Bd. Pat. App. & Int. 1988).

that the proponent of unpatentability has the burden of establishing that the claims are either anticipated or rendered obvious and emphasized the necessity to employ the factual inquiries set forth in Graham.

The Examiner's failure to make a Graham analysis is fatal to the '103 rejection.

> In patent cases, the need for express Graham findings takes on an especially significant role because of an occasional tendency of district courts to depart from the Graham test, and from the statutory standard of unobviousness that it helps determine, to the tempting but forbidden zone of hindsight.

Loctite.[143] The court in Loctite stressed the importance of Graham findings in order to evaluate the question of obviousness/nonobviousness. Here, the '103 rejection should be reversed because there is an insufficient factual basis upon which to reach a conclusion of obviousness. Whether characterized as a dereliction of duty or error, a failure by the Examiner to make specific Graham findings is proper grounds for reversing the instant '103 rejection.

In view of the above, the Examiner has not provided a Graham analysis in support of the '103 rejection because a Graham analysis would show that the claims are not obvious over the references. Hence, the '103 rejection should be reversed.

8.9.3 The Claims Distinguish Over The References

The claims distinguish over the references. The references (Hill, Lord, and Lelke) are incompatible and

---

[143] Loctite Corp. v. Ultraseal Ltd., 781 F.2d 861, 873, 228 USPQ 90, 98 (Fed. Cir. 1985).

cannot properly be combined. For example, Hill has a video painting system, Lord has a resolution improvement television system, and Lelke has an advertising-composition system. The systems are implemented differently for different purposes and the rejection is devoid of any indication of how an artisan would combine the references in an operable manner, or where the references suggest the combination, or why an artisan would expect success. Judge Hairston stated in Hyatt-'886[144]:

> In the absence of a convincing reason for combining the teachings of such disparate display teachings, we will reverse the 35 U.S.C. 103 rejection of claims 42 and 43.

The claims rejected over Hill, Lord, and Lelke under '103 have novel distinctions thereover. Representative limitations that distinguish over these references are excerpted from the claims and are set forth below.[145]

> 19. A memory system comprising:
>
> an image input circuit generating input image information;
>
> a two dimensional frame buffer storing a frame of image information, the frame of image information

---

[144] Ex parte Hyatt, Appeal No. 93-2572, Paper No. 31 at 6 in patent application Serial No. 07/515,886 which issued as U.S. Patent No. 5,398,041 on March 14, 1995 (Bd. Pat. App. & Int. March 24, 1994) [herein Hyatt-'886] (unpublished PTO decision).

[145] Important limitations; such as coupling, responsiveness, and elements of the combination; are not included in the excerpts for brevity. However, these other limitations are also contested limitations (e.g., Exhibit-3).

arranged in a two dimensional array of rows and columns of blocks of pixel image information;

an address generator generating write addresses and generating read addresses;

a frame buffer writing circuit coupled to the image input circuit, coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer writing circuit writing the frame of image information into the two dimensional frame buffer in response to the input image information generated by the image input circuit and in response to the write addresses generated by the address generator;

a frame buffer accessing circuit coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer accessing circuit accessing blocks of pixel image information in response to the read addresses generated by the address generator;

a two dimensional spatial processor coupled to the frame buffer accessing circuit and generating two dimensional spatially processed image information in response to the blocks of pixel image information accessed by the frame buffer accessing, circuit; and

an output circuit coupled to the two dimensional spatial processor and generating output image information in response to the two dimensional spatially processed image information generated by the two dimensional spatial processor.

25. A memory system comprising:

an image input circuit generating input image information;

a two dimensional pixel block memory storing a two dimensional array of blocks of pixel image information, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

an address generator generating write addresses and generating read addresses;

a pixel block memory writing circuit coupled to the image input circuit, coupled to the two dimensional pixel block memory and coupled to the address generator, the pixel block memory writing circuit writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory in response to the input image information generated by the image input circuit and in response to the write addresses generated by the address generator;

a first clock circuit generating a first clock signal having a first clock rate;

a pixel block memory accessing circuit coupled to the two dimensional pixel block memory, coupled to the first clock circuit and coupled to the address generator, the pixel block memory accessing circuit accessing blocks of pixel image information in response to the read addresses generated by the address generator, wherein the accessing of blocks of pixel image information from the two dimensional pixel block memory by the pixel block memory accessing circuit

is at a first information rate in response to the first clock signal;

a two dimensional spatial processor coupled to the pixel block memory accessing circuit and generating two dimensional spatially processed image information in response to the blocks of pixel image information accessed by the pixel block memory accessing circuit;

a second clock circuit generating a second clock signal having a second clock rate that is different than the first rate of the first clock signal; and

an output circuit coupled to the two dimensional spatial processor and coupled to the second clock circuit, the output circuit generating output image information in response to the two dimensional spatially processed image information generated by the two dimensional spatial processor, wherein the generation of the output image information by the output circuit is at a different information rate than the first information rate in response to the second clock signal.

96. A process of operating a memory system comprising the acts of:

generating input image information;

storing a two dimensional array of blocks of pixel image information in a two dimensional pixel block image memory in response to the input image information, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

generating read addresses;

accessing blocks of pixel image information from the two dimensional pixel block image memory in response to the read addresses;

generating two dimensional spatially processed image information in response to the accessed blocks of pixel image information; and

storing buffered two dimensional spatially processed image information in a buffer memory in response to the two dimensional spatially processed image information.

100. A process of operating a memory system comprising the acts of:

generating input image information at a first information rate;

storing a two dimensional array of blocks of pixel image information in a two dimensional pixel block memory in response to the input image information, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

generating read addresses;

accessing blocks of pixel image information in response to the read addresses;

generating two dimensional spatially processed image information in response to the accessed blocks of pixel image information;

generating output image information in response to the two dimensional spatially processed image information; and

outputting the output image information at a second information rate that is greater than the first information rate.

101. A process of operating a memory system comprising the acts of:

generating input image information at a first information rate;

storing a two dimensional array of blocks of pixel image information in a two dimensional pixel block memory in response to the input image information, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information;

accessing blocks of pixel image information;

generating two dimensional spatially processed image information in response to the accessed blocks of pixel image information;

generating output image information in response to the two dimensional spatially processed image information; and

outputting the output image information at a second information rate that is greater than the first information rate.

135. A memory system as set forth in claim 19, further comprising:

a display coupled to the output circuit and displaying an image in response to the output image information generated by the output circuit.

140. A memory system as set forth in claim 25, further comprising:

a display coupled to the output circuit and displaying an image in response to the output image information generated by the output circuit.

8.9.4 The '103 Rejection Does Not Establish A Prima Facie Case

The Examiner must support art rejections with a proper explanation of why the claims are rendered obvious by the references. Such support of the art rejections requires, as stated above, an evaluation of the claims as a whole, the references as a whole, a proper construction of each of the claims to determine their scope and meaning, a limitation-by-limitation analysis of each claim element, a claim-by-claim analysis of each of the claims subject to rejection, and consideration of all of the words in each claim. These legal requirements, which have been established by case law, must, in conjunction with the well-established Graham analysis, result in the establishment of a prima facie case.

Establishing a prima facie case of obviousness requires meeting three basic criteria. See MPEP 2143. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to an artisan, to modify the reference or to combine reference teachings (the references must also suggest the desirability of the modification or combination). Second, there must be a reasonable expectation of success in making the modification or combina-

tion. Third, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on the applicant's disclosure. See Vaeck.[146] See also MPEP 2142. Because the '103 rejection is not supported by the required analysis, the '103 rejection fails to establish a prima facie case.

The Board in Levengood[147] made clear that some objective reason to combine the teachings of the references is necessary. The mere statement that the modification would have been within the skill of the art is not sufficient to establish a prima facie case. See MPEP 2143.01. The instant '103 rejection therefore fails to establish a prima facie case of obviousness.

The legal concept of prima facie obviousness is a procedural tool of examination which applies broadly to all arts. It allocates who has the burden of going forward with production of evidence in each step of the examination process. See MPEP 2142.

The burden of establishing a prima facie case rests with the Examiner[148] and is not satisfied by the mere pairing up of claimed elements with elements in the references.[149] Rather, the Examiner must support a '103 rejection with a proper explanation of why the claims

---

[146] In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

[147] Ex parte Levengood, 28 USPQ2d 1300, 1301 (Bd. Pat. App. & Int. 1993).

[148] In re Piasecki, 745 F.2d 1468, 223 USPQ 785 (Fed. Cir. 1984).

[149] In re Edwards, 568 F.2d 1349, 1354, 196 USPQ 465, 469 (CCPA 1978); In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992).

are obvious and must provide acceptable evidence reasoning.[150] However, the instant '103 rejection provides neither a proper explanation mr acceptable evidence or reasoning.

Even though a Graham analysis is required to support a '103 rejection[151], the '103 rejection fails to make a Graham analysis (Section 8.9.2). Graham requires that the Examiner determine the scope and content of the prior art, ascertain the differences between the prior art and the claims in issue, resolve the level of ordinary skill in the pertinent art, and evaluate evidence of secondary considerations. However, the '103 rejection does not address any of these requirements much less satisfy these requirements.

The instant '103 rejection fails to evaluate the claim differences, which is fatal to the '103 rejection.

> Appellant was entitled to have differences between the claimed invention, the subject matter as a whole, and the prior art references of record evaluated. . . . This the examiner failed to do.

Lunsford.[152]

The '103 rejection fails to consider important claim limitations even though a '103 rejection must consider all of the words in the claims. See Wilson.[153] See also MPEP 2143.03 and Section 8.7.1.

---

150 In re Piasecki, 745 F.2d 1468, 223 USPQ 785 (Fed. Cir. 1984).

151 See MPEP 2141, 2141.01, 2141.03, 2142, 2143.01, and 2143.03.

152 In re Lunsford, 357 F.2d 385, 391, 148 USPQ 721, 725 (CCPA 1966).

153 In re Wilson, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970).

The Appellant has established that there are extensive novel differences between the instant claims and the references (e.g., Sections 8.8.2 and 8.9.3). However, the '103 rejection does not establish that these novel differences are obvious.

The prior art must teach or suggest all of the claim limitations to support a '103 rejection. See Royka.[154] See also MPEP 2143.03. However, the instant '103 rejection does not establish what is relied on in the references to teach or suggest each of the claim limitations (Section 8.7.1).

In view of the above, the '103 rejection does not establish a prima facie case. Hence, the '103 rejection should be reversed.[155]

8.9.5 Conclusion

The 35 USC 103 rejection should be reversed for the reasons set forth above; the '103 rejection relies on improper hindsight; the '103 rejection does not perform the required Graham analysis; the claims distinguish over the references; and the '103 rejection does not establish a prima facie case; and for the additional reasons set forth in Section 8.7.

8.10 THE 35 USC 112-1 AND THE DOUBLE PATENTING REJECTIONS ARE JUDICIALLY ESTOPPED

The '112-1 rejections and the double patenting rejections are judicially estopped. The Examiner contends that there is no relevant disclosure whatsoever in sup-

---

[154] In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

[155] In re Oetiker, 977 F.2d 1443, 24 U.S.P.Q.2d 1443 (Fed. Cir. 1992).

port of the '112-1 rejections, but then admits to the instant claims being fully disclosed (Section 8.1.2) in support of the double patenting rejections. This scheme is judicially estopped. In addition, the Examiner ignores extensive basis for the claim limitations (Sections 8.1.5, 8.1.7, and 8.2.1 and Table-1) in the instant disclosure while alleging full anticipation by references that do not teach the claimed invention. This scheme is also judicially estopped. Further, other examiners have restricted claims in related applications, and yet the Examiner now rejects the instant claims for double patenting without even considering the restriction requirements. This scheme is also judicially estopped.

Under the doctrine of judicial estoppel, where a party assumes a certain position, he may not thereafter assume a contrary position.[156] As the Federal Circuit explained in Sears, judicial estoppel is designed to preserve the integrity of the judicial process by "protecting against litigants who 'play fast and loose with the courts.'" Id. at 596-97.

The rejections in the instant application are grossly inconsistent, alleging complete lack of disclosure regarding the '112-1 rejections (Sections 8.1 to 8.3) and then alleging full disclosure in support of the double patenting rejections (Section 8.1.2). By maintaining one position to support the '112-1 rejections and taking a contrary position to support the double patenting rejections, the Examiner has violated the doctrine of judicial estoppel because, in making such grossly inconsistent

---

[156] Davis v. Wakelee, 156 U.S. 680, 689 (1895); see also U.S. Philips v. Sears Roebuck & Co., 55 F.3d 592, 596 (Fed. Cir. 1995), cert. denied, 116 S.Ct. 567, and cert. denied, 116 S.Ct. 672 (1995).

rejections, the Examiner is playing "fast and loose" with the judicial system. Because the taking of such inconsistent positions is not allowed, the '112-1 rejections and the double patenting rejections should be reversed.

8.11 THE APPELLANT IS ENTITLED TO A PATENT

Because the rejections fail to establish a prima facie case (Sections 8.1.8, 8.2.4, 8.3.2, 8.4.6, 8.6.8, 8.7.3, 8.8.3, and 8.9.4 herein), then according to the Federal Circuit, the Appellant is entitled to a patent, as discussed below.

Judge Plager stated the following in his concurring opinion in Oetiker[157]:

> An applicant for a patent is entitled to the patent unless the application fails to meet the requirements established by law. It is the Commissioner's duty (acting through the examining officials) to determine that all requirements of the Patent Act are met. The burden is on the Commissioner to establish that the applicant is not entitled under the law to a patent. In re Warner, 379 F.2d 1011, 1016, 154 USPQ 173, 177 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968). In rejecting an application, factual determinations by the PTO must be based on a preponderance of the evidence, and legal conclusions must be correct. In re Caveney, 761 F.2d 671, 674, 226 USPQ 1, 3 (Fed. Cir. 1985).
>
> The process of patent examination is an interactive one. See generally, Chisum, Patents, § 11.03 et seq. (1992). The examiner cannot sit mum, leaving the

---

[157] In re Oetiker, 977 F.2d 1443, 1449, 24 USPQ2d 1443, 1447 (Fed. Cir. 1992).

applicant to shoot arrows into the dark hoping to somehow hit a secret objection harbored by the examiner. The 'prima facie case' notion, the exact origin of which appears obscure (see In re Piasecki, 745 F.2d 1468, 1472, 233 USPQ 785, 788 (Fed. Cir. 1984)), seemingly was intended to leave no doubt among examiners that they must state clearly and specifically any objections (the prima facie case) to patentability, and give the applicant fair opportunity to meet those objections with evidence and argument. To that extent the concept serves to level the playing field and reduces the likelihood of administrative arbitrariness.

* * *

Specifically, when obviousness is at issue, the examiner has the burden of persuasion and therefore the initial burden of production. Satisfying the burden of production, and thus initially the burden of persuasion, constitutes the so-called prima facie showing. Once that burden is met, the applicant has the burden of production to demonstrate that the examiner's preliminary determination is not correct. The examiner, and if later involved, the Board, retain the ultimate burden of persuasion on the issue.

If, as a matter of law, the issue is in equipoise, the applicant is entitled to the patent. Thus on appeal to this court as in the PTO, the applicant does not bear the ultimate burden of persuasion on the issue. In the end there is no reason there or here to argue over whether a 'prima facie' case was made out. The only determinative issue is whether the record as a

whole supports the legal conclusion that the invention would have been obvious.

Similarly, in the instant case, the Examiner has not met his legal burden with factual determinations, with a preponderance of the evidence, or with proper legal conclusions. Hence, the Appellant is entitled to a patent asa matter of law.

IX. CONCLUSION

The Appellant has established that the disclosure is adequate, and meets the requirements of 35 USC 112-1. The Appellant has further established that the rejections under 35 USC 112-1 do not establish a prima facie case, violate the law of the Federal Circuit, and are based upon erroneous and unsupported allegations. For each of these reasons, the Appellant respectfully requests that the 35 USC 112-1 rejections be reversed.

The Appellant has established that the claims of the instant application patentably distinguish over and are independent or distinct relative to the claims of the eight copending applications. The Appellant has further established that the double patenting rejections do not establish a prima facie case, violate the law of the Federal Circuit, and are based upon erroneous and unsupported allegations. For each of these reasons, the Appellant respectfully requests that the double patenting rejections be reversed.

The Appellant has established that the claims of the instant application patentably distinguish over the prior art references. The Appellant has further established that the art rejections do not establish a prima facie case and violate the law of the Federal Circuit. For each of

these reasons, the Appellant respectfully requests that the art rejections be reversed.

Because the Examiner has failed to, and in fact cannot,[158] establish a prima facie case, the Appellant is entitled to a patent.[159]

CERTIFICATION OF MAILING BY EXPRESS MAIL:

I hereby certify that this correspondence is being deposited with the United States Postal Service with Express Mail post office to addressee service under 37 CFR 1.10, postage prepaid, in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231 with the express mail label number EN375192599 on September 2, 1998.

Respectfully submitted,

/s/ GILBERT P. HYATT
GILBERT P. HYATT
Registration No. 27,647
[address and phone
number omitted]

Dated: Sept. 2, 1998

---

[158] The Examiner cannot establish a prima facie case because the claims find ample antecedent basis in the disclosure, there is no double patenting, and the prior art references do not anticipate the claims nor render the claims obvious.

[159] In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992).

No. 10-1219

In the Supreme Court of the United States

DAVID J. KAPPOS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR, UNITED STATES PATENT AND TRADEMARK OFFICE, PETITIONER

v.

GILBERT P. HYATT

ON WRIT OF CERTIORARI TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

VOLUME 4
JOINT APPENDIX

DONALD B. VERRILLI, JR.
Solicitor General
Department of Justice
Washington, D.C. 20530-0001
SupremeCtBriefs@usdoj.gov
(202) 514-2217

Counsel of Record for Petitioner

AARON M. PANNER*
Kellogg, Huber, Hansen, Todd, Evans & Figel, P.L.L.C.
1615 M Street, N.W.
Suite 400
Washington, D.C. 20036
apanner@khhte.com
(202) 723-6871

GREGORY L. ROTH
5712 Parkwest Circle
La Palma, CA 90623
(714) 723-6871

* *Counsel of Record for Respondent*

PETITION FOR A WRIT OF CERTIORARI FILED: APR. 7, 2011
CERTIORARI GRANTED: JUNE 27, 2011

TABLE OF CONTENTS

Page

VOLUME 1

Court of appeals docket entries 1
District court docket entries 4
In re Application of Gilbert P. Hyatt:
Specification (June 6, 1995) 9

VOLUME 2

Specification Diagrams (June 6, 1995) 146

VOLUME 3

Amendment Under 37 C.F.R. § 1.111 (Oct. 15, 1996) 263
Final Office Action (July 30, 1997) 365
Appeal Brief (Sept. 2, 1998) 393

VOLUME 4

Examiner's Answer (Aug. 13, 1999) 541
Reply Brief Under 37 C.F.R. § 1.193(b) (July 31, 2000) 588
Request for Rehearing (Sept. 30, 2002) 670

[SEAL OMITTED]

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
ASSISTANT SECRETARY AND COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

[Filed: May 31, 2000]

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 34

Application Number: 08/471,702
Filing Date: 6/6/95
Appellant(s): Gilbert P. Hyatt

Gilbert P. Hyatt
For Appellant

EXAMINER'S ANSWER

This is in response to appellant's brief on appeal filed 9/2/98.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is deficient because it does not provide a summary of the claimed invention. Appellants summary is a summary of the detailed description and not a summary of the claimed invention. The claimed invention is directed to the portions of the specification which describe a vector memory storing vectors, reading the vectors from the vector memory, sending the read vectors to the address generators, strobing (writing) color values into image memory at the locations defined by the address generators, reading the image memory during display system readout, storing the readout values in a buffer memory, applying in parallel 9 pixels of information from the buffer memory to a spatial filter, applying the spatially

filtered pixel information to a digital to analog convertor, and sending the analog signal to a monitor.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that the claims do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

4,069,511	Lelke	01/17/78
4,200,867	Hill	04/29/80
4,322,750	Lord	03/30/82

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 112

10.1 The claims of this application are directed to the portions of the specification which describe a vector memory storing vectors, reading the vectors from the vector memory, sending the read vectors to the address generators, strobing (writing) color values into image memory at the locations defined by the address genera-

tors, reading the image memory during display system readout, storing the readout values in a buffer memory, applying in parallel 9 pixels of information from the buffer memory to a spatial filter, applying the spatially filtered pixel information to a digital to analog convertor, and sending the analog signal to a monitor. It is clear from the following rejections based upon 35 U.S.C. 112, first paragraph, that the claims of this application are not supported and/or enabled by the specification.

10.2 Claims 1-14 and 119-132 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 1-14 and 119-132 claim "a data decompressed video image input circuit generating data decompressed image information". The claimed feature of a circuit for compressing video image information was not described in the specification at the time of filing this application nor at the time of filing parent application serial no. 06/662,211. This specification briefly describes compressing database images and data compression but the specification is totally silent as to compressing video images or to compressing images. The specification at page 23 lines 1-18 states "Image processing can be performed on digitized images stored in the database. A stored image can be loaded from the database into image memory for image processing online with a hardware-implemented image processor. A stored image can be preprocessed, such as offline in the database and such as online with a preprocessor. Offline processing can be performed during database generation, such

as filtering database images before storing the images in the database. Online preprocessing can be performed during system operation, such as by accessing database images and preprocessing the accessed database imageswith compression and filtering, prior to loading into image memory. Offline preprocessing can be performed for filtering of images, which is illustrative of other forms of offline preprocessing and is also illustrative of online preprocessing. For example, other forms of offline preprocessing includes data compression, image enhancement, and other forms of filtering. Also, other forms of online preprocessing includes data decompression, image expansion, image compression, and filtering.". Thus, applicants originally filed specification does not manifest that applicant had possession of the currently claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

10.3 Claims 1-14 and 119-132 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 1-14 and 119-132 claim "a data decompressed video image input circuit generating data decompressed graphic image information". The claimed feature of a circuit for or method of compressing video image information was not enabled in the specification at the time of filing this application nor at the time of filing parent application serial no. 06/662,211. Thus, applicants specification fails to enable one of ordi-

nary skill in the art at the time of filing the parent to practice applicants invention.

10.4 Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, 95-112, 117, and 118 claim a writing circuit and an accessing circuit for writing and reading a block of video pixel image data into the block memory or the process of writing and reading a block of video pixel image data into the block memory. These claims cover simultaneous writing and reading of a block of graphic image data (note claims 110 and 117). Claims 112 or 118 solve the accessing problem but does not solve the writing. The specification does not describe this. This claimed feature was not described in the specification at the time of filing this application nor at the time of filing parent application serial no. 06/662,211. The specification describes a sequential write to and read from the block memory. Thus, applicants originally filed specification does not manifest that applicant had possession of the currently broadly claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

10.5 Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable

one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, 95-110, 112, 117, and 118 claim a writing circuit and an accessing circuit for writing and reading a block of video pixel image data into the block memory. These claims cover simultaneous writing and reading of a block of video pixel image data (note claims 110 and 117). Claims 112 or 118 solve the accessing problem but does not solve the writing. The specification does not describe this. The specification describes a sequential write to and read from the block memory. The specification fails to enable one of ordinary skill in the art at the time of filing this application and at the time of filing parent application serial no. 06/662,211 to build a circuit which simultaneously writes block of information into the block memory or to build a circuit which simultaneously reads a block of information out the block memory.

10.6 Claims 1, 2, 5, 9, 10, 12, 20, 81, 85, 98, 110-114, 119, 120, 123, 127, 128, 130, 136, 153, 157, and 161 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 1, 2, 5, 9, 10, 12, 20, 81, 85, and 98 claim a vector processor responsive to an accessed block of video pixel image information and to vector information. This feature of the claims is not supported by applicants originally filed specification nor by parent application serial no. 06/662,211. Thus, applicants originally filed specification does not manifest that

applicant had possession of the currently claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

10.7 Claims 1, 2, 5, 9, 10, 12, 20, 81, 85, 98, 110-114, 119, 120, 123, 127, 128, 130, 136, 153, 157, and 161 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 1, 2, 5, 9, 10, 12, 20, 81, 85, and 98 claim a vector processor responsive to an accessed block of video pixel image information and to vector information. This feature of the claims is not enabled by applicants originally filed specification nor by parent application serial no. 06/662,211. Thus, applicants specification fails to enable one of ordinary skill in the art at the time of filing to practice applicants invention.

10.8 Claims 3, 4, 11, 121, 122, and 129 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 3, 4, and 11 claim a processor responsive to an accessed block of video pixel image information. This feature of the claims is not supported by applicants originally filed specification nor by parent application serial no. 06/662,211. Thus, applicants originally filed specification does not manifest that applicant had possession of the currently claimed invention at the time of filing. In

re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

10.9 Claims 3, 4, 11, 121, 122, and 129 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 3, 4, and 11 claim a processor responsive to an accessed block of video pixel image information. This feature of the claims is not enabled by applicants originally filed specification nor by parent application serial no. 06/662,211. Thus, applicants specification fails to enable one of ordinary skill in the art at the time of filing to practice applicants invention.

10.10 Claims 1, 85, 95, 110-112, 119, 157, and 158 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 1, 85, and 95 claim a spatial processor responsive to an accessed block of video pixel image information and to vector information and generating data compressed video. This feature of the claims is not supported by applicants originally filed specification nor by parent application serial no. 06/662,211. Thus, applicants originally filed specification does not manifest that applicant had possession of the currently claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and

Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

10.11 Claims 1, 85, 95, 110-112, 119, 157, and 158 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 1, 85, and 95 claim a spatial processor responsive to an accessed block of video pixel image information and to vector information and generating data compressed video. This feature of the claims is not enabled by applicants originally filed specification nor by parent application serial no. 06/662,211. Thus, applicants specification fails to enable one of ordinary skill in the art at the time of filing to practice applicants invention.

10.12 Claims 6-9, 13, 14, 24, 34, 36, 42, 49, 50, 102, 106, 115-118, 124-127, 131, 132, 139, 141, 143, 145, 149, 150, 165, and 169 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 6-9, 13, 14, 24, 34, 36, 42, 49, 50, 102, 106, 115-118, 139, 141, 143, 145, 149, 150, 165, and 169 claim a frequency domain processor or generating frequency domain image information or frequency domain information. The specification does not describe frequency domain, frequency domain processor, frequency domain image information or frequency domain information. This claimed feature was not described in the specification at the time of filing this application nor at the time of filing parent applica-

tion serial no. 06/662,211. Thus, applicants originally filed specification does not manifest that applicant had possession of the currently claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

10.13 Claims 6-9, 13, 14, 24, 34, 36, 42, 49, 50, 102, 106, 115-118, 124-127, 131, 132, 139, 141, 143, 145, 150, 165, and 169 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 6-9, 13, 14, 24, 34, 36, 42, 49, 50, 102, 106, 115-118, 139, 141, 143, 145, 149, 150, 165, and 169 claim frequency a frequency domain processor or generating frequency domain image information or frequency domain information. The specification does not enable one of ordinary skill in the art at the time of filing this application nor at the time of filing the parent application to build a system using frequency domain, frequency domain processor, frequency domain image information, or frequency domain information. This claimed feature was not enabled by the specification at the time of filing this application nor at the time of filing parent application serial no. 06/662,211. Thus, applicants specification fails to enable one of ordinary skill in the art at the time of filing to practice applicants invention.

10.14 Claims 17, 18, 133, and 134 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a

way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 17 and 18 claim a block processor responsive to an accessed block of pixel image information and to vector information. This feature of the claims is not supported by applicants originally filed specification nor by parent application serial no. 06/662,211. Thus, applicants originally filed specification does not manifest that applicant had possession of the currently claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

10.15 Claims 17, 18, 133, and 134 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 17 and 18 claim a processor responsive to an accessed block of pixel image information and to vector information. This feature of the claims is not enabled by applicants originally filed specification nor by parent application serial no. 06/662,211. Thus, applicants specification fails to enable one of ordinary skill in the art at the time of filing to practice applicants invention.

10.16 Claims 24, 34-37, 42-45, 49-51, 102-109, 115-118, 139-151, and 165-172 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had

possession of the claimed invention. No claims in this application directly claim an input weight circuit generating input weight information, however, claims 24, 34-37, 42-45, 49-51, 102-109, 115, and 116 claim other weight related elements. An input weight circuit generating input weight information is not supported by the specification. This implicitly claimed feature was not described in the specification at the time of filing this application nor at the time of filing parent application serial no. 06/662,211. The specification at page 147 lines 12-17 and figures 6Y and 6Z teach applying addresses through multiplexers U5C and U6C to the address inputs of RAMs U5E and U6E so these RAMs may store weight addresses supplied on input lines IO0 to IO3 from address generators. The same lines of page 147 describe the line buffers U4F to U6F as applying the intensity bits from image memory to RAMs U3E and U4E and applying the weight addresses from the address generators to RAMs U5E and U6E. Page 142 lines 13 to 29 and figure 6X describe an address counter for generating the addresses to be applied to the address lines of RAMs U3E, U4E, U5E, and U6E so these RAMS will be able to store the intensity and weight addresses at storage locations determined by the addresses. Page 149 lines 1-9 describes reading the weight addresses from RAMs U5E and U6E and applying those weight addresses on a weight bus. Page 162 lines 5-7 describes outputting the weight addresses stored in the line buffers to the weight RAMs U21E toU23E for accessing of the weights associated therewith in order for those weights to be applied to the spatial filter (spatial filter shown in figure 5A). Page 12 lines 1-6 describes using address generators for performing a vector to raster conversion by using the address generators to step

through addresses and by strobing a color value into each memory location represented by each address of the generated addresses. Pages 118 to 127 and figures 6O to 6R describes address generators for generating addresses. Applicant has failed to describe an address generator which will generate weight addresses and has failed to describe an address generator which will apply the weight addresses to the inputs of RAMS U5E and U6E at the same time the intensity bits are being applied to RAMS U3E and U4E. This portion of applicants specification is critical in supporting the claimed invention because each weight address associated with an intensity value for a pixel must select a weight value from the weight table which will perform the correct filtering of a matrix of pixels in the spatial filter in order for the desired filtered image to be generated. Applicant has thus failed to teach an address generator which will generate weight addresses for selecting weight values from the weight table to perform the desired weighting function at the spatial filter. Thus, applicants originally filed specification does not manifest that applicant had possession of the currently claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

10.17 Claims 24, 34-37, 42-45, 49-51, 102-109, 115-118, 139-151, and 165-172 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. No claims in this application directly

claim an input weight circuit generating input weight information, however, claims 24, 34-37, 42-45, 49-51, 102-109, 115, and 116 claim other weight related elements. Claims 24, 34-37, 42-45, 49-51, 102-109, 115, and 116 "rely upon the input weight circuit for supporting the weight functions performed by the other weight elements. The specification, at the time of filing this application and at the time of filing parent application serial no. 06/662,211, does not enable one of ordinary skill in the art to build an address generator which will generate weight addresses and to build an address generator which will apply the weight addresses to the inputs of RAMS U5E and U6E at the same time the intensity bits are being applied to RAMS U3E and U4E. This portion of applicants specification is critical in supporting the claimed invention because each weight address associated with an intensity value for a pixel must select a weight value from the weight table which will perform the correct filtering of a matrix of pixels in the spatial filter in order for the desired filtered image to be generated. Therefore, at the time of filing the oldest parent application, applicant has also failed to enable one of ordinary skill in the art with the knowledge to build an address generator which will generate weight addresses for selecting weight values from the weight table in order to perform the desired weighting function at the spatial filter. Thus, applicants specification fails to enable one of ordinary skill in the art at the time of filing to practice applicants invention and to build a complete working kernel processor.

10.18 Claims 34, 36, 42-45, 106-109, 141-148, and 169-172 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in

the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 34, 36, 42-45, and 106-109 claim block boundary smoothing. This type of processing was not described in the specification. This claimed feature was not described in the specification at the time of filing this application nor at the time of filing parent application serial no. 06/662,211. Thus, applicants originally filed specification does not manifest that applicant had possession of the currently claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

10.19 Claims 34, 36, 42-45, 106-109, 141-148, and 169-172 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 34, 36, 42-45, and 106-109 claim block boundary smoothing. This type of processing was not described in the specification. The specification does not enable one of ordinary skill in the art at the time of filing the parent application to build a memory system using a block boundary processor or generating block boundary smoothing information. Thus, applicants specification fails to enable one of ordinary skill in the art at the time of filing to practice applicants invention.

10.20 Claim 112 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reason-

ably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. This claim claims that the memory system is a video image data compression system. This claimed feature was not described in the specification at the time of filing this application nor at the time of filing parent application serial no. 06/662,211. Thus, applicants originally filed specification does not manifest that applicant had possession of the currently claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

10.21 Claim 112 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. This claim claims that the memory system is a video image data compression system. This claimed feature was not enabled by the specification at the time of filing this application nor at the time of filing parent application serial no. 06/662,211. Thus, applicants specification fails to enable one of ordinary skill in the art at the time of filing to practice applicants invention.

10.22 Claim 116 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. This claim claims a quantization weighting processor. This processor was

not described in the specification. This claimed feature was not described in the specification at the time of filing this application nor at the time of filing parent application serial no. 06/662,211. Thus, applicants originally filed specification does not manifest that applicant had possession of the currently claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

10.23 Claim 116 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. This claim claims a quantization weighting processor. The specification does not enable one of ordinary skill in the art at the time of filing the parent application to build a memory system using a quantization weighting processor. Thus, applicants specification fails to enable one of ordinary skill in the art at the time of filing to practice applicants invention.

10.24 Claims 2-14, 113, 114, and 120-132 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 2-14 claim generating data compressed video image information. This type of image information was not described in the specification let alone the processor needed to perform the generation. Thus, this claimed feature was not described in the specification at

the time of filing this application nor at the time of filing parent application serial no. 06/662,211. Thus, applicants originally filed specification does not manifest that applicant had possession of the currently claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

10.25 Claims 2-14, 113, 114, and 120-132 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 2-14 claim generating data compressed video image information. This type of image information was not enabled in the specification let alone the processor needed to perform the generation. The specification does not enable one of ordinary skill in the art at the time of filing the parent application to build a memory system using a quantization weighting processor. Thus, applicants specification fails to enable one of ordinary skill in the art at the time of filing to practice applicants invention.

10.26 Claims 153-172 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. These claims claim the act of making a product in response to image information. The originally filed specification did not describe making a product in response to information. This claimed feature was not described in the specification at

the time of filing this application nor at the time of filing parent application serial no. 06/662,211. Thus, applicants originally filed specification does not manifest that applicant had possession of the currently claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

10.27 Claims 153-172 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. These claims claim the act of making a product in response to image information. The originally filed specification did not describe making a product in response to information. This claimed feature was not enabled by the specification at the time of filing this application nor at the time of filing parent application serial no. 06/662,211. Thus, applicants specification fails to enable one of ordinary skill in the art at the time of filing to practice applicants invention.

Double Patenting

10.28 The non-statutory double patenting rejection, whether of the obviousness-type or non-obviousness-type, is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985) *In re Van Ornum*, 686 F.2d 937, 214 USPQ

761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a non-statutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10.29 Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-162 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over:

claims 17-20, 22-25, 42-45, 49-52, 71-74, 81-85, and 110-162 of copending Application No. 08/472,062;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 96-173 of copending Application No. 08/479,088;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 of copending Application No. 08/471,925;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 of copending Application No. 08/479,086;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 of copending Application No. 08/479,087;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 of copending Application No. 08/471,712;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 96-173 of copending Application No. 08/471,704; and

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 90-167 of copending Application No. 08/483,016. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims in these nine copending applications claim a memory system for storing image information and for processing the stored image information and for outputting the processed image information. The minor differences between the claims in these nine applications are obvious variations of the same claimed invention. A grant of a second patent from these nine patent applications would unjustly extend the right given in a first patent from these nine patent applications.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

10.30 Claims 1-14, 17-20, 22-25, 34-37 42-45, 49-52, 81-85, and 95-162 are provisionally rejected under the judicially created doctrine of double patenting over:

claims 17-20, 22-25, 42-45, 49-52, 71-74, 81-85, and 110-162 of copending Application No. 08/472,062;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 96-173 of copending Application No. 08/479,088;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 of copending Application No. 08/471,925;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 of copending Application No. 08/479,086;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 of copending Application No. 08/479,087;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 of copending Application No. 08/471,712;

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 96-173 of copending Application No. 08/471,704; and

claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 90-167 of copending Application No. 08/483,016. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows: the claims in these nine copending applications claim a memory system for storing image information and for processing the stored image information and for outputting the processed image information. The minor differences between the claims in these nine applications are obvious variations of the same claimed invention. A grant of a second patent from these nine patent applications would unjustly extend the right given in a first patent from these nine patent applications.

Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Claim Rejections - 35 USC § 102

10.31 The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless—
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10.32 Claims 22, 23, 83, 84, 95, 137, and 138 are rejected under 35 U.S.C. 102(b) as being anticipated by Hill U.S. Patent No. 4,200,867. Hill describes a picture matrix memory which stores a block of video data. A processor (MPU 162) is connected to a memory accessing circuit and thus generates output video image information which is then stored in a buffer memory (shift registers 400A, 400B, 400C).

10.33 Claims 82 and 99 are rejected under 35 U.S.C. 102(b) as being anticipated by Hill U.S. Patent No. 4,200,867. The MPU generates the video image information at a first word rate and the shift registers output the video image information at a second word rate.

Claim Rejections - 35 USC § 103

10.34 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set

> forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvions at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10.35 Claims 19, 25, 96, 100, 101, 140, and 135 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Lord et al U.S. Patent No. 4,322,750 and Hill U.S. Patent No. 4,200,867 and Lelke U.S. Patent No. 4,069,511. Lord et al describes a memory system for a display system were a spatial processor 21 is connected to an accessing circuit 20 for reading a block of image information. Lord does not describe the field store as being formed with blocks of storage locations and Lord does not describe a buffer connected to the output of the spatial processor. Lelke shows that it is old and well known to form a field memory with blocks of memory locations. Figures 6 and 13 show a field memory formed out of blocks of storage locations with figure 13 showing a block of memory locations. Hill shows that it is old and well known to use a buffer memory (shift registers 400A, 400B, 400C) to store the output of a processor. It would have been obvious to one of ordinary skill in the art at the time of applicants invention to use a block memory in Lord because the chips from which the memory is formed from lead one of ordinary skill in the art to forming a field memory with blocks of chips. It would have been obvious to one of ordinary skill in the art at the time of applicants invention to use a buffer memory to temporally store the out-

put of the spatial processor in order to buffer the data prior to sending the spatially filtered image information to an output device.

10.36 Re claims 25, 100, 101, and 140:

These claims add the additional feature of a first clock and a second clock. The processor of Hill operates at one clock rate while the shift registers output the video image information at a second word rate. Thus, it would have been obvious to one of ordinary skill in the art at the time of applicants invention access the image memory at one clock rate while operating the buffers at a second clock rate.

(11) Response to Argument

In sections 8.1 to 8.3 and 8.10 appellant argues against the 35 USC 112 first paragraph written description and enablement rejections.

In section 8.1.1 appellant argues that since the ancestor specification became a patent (5,584,032), then this identical specification is presumed to be correct. This is incorrect since the specification of a patent is normally analyzed with respect to the claims and could not be analyzed for all aspects. The claims in the patent are different than the claims in this application (unless appellant is implying that the claims in this application are the same as the claims in the patent). Thus, this argument is not persuasive.

In section 8.1.1 appellant further argues that an applicant's disclosure is to be presumptively correct and that an examiner is required to proved sufficient objective reasons to challenge this presumption. Appellant alleges that the examiner did not provide the required

objective reasons to overcome the presumption of correctness. Appellant also alleges that due to the extensive disclosure the claims must be supported by the disclosure. The examiner has followed MPEP 2163.04 in making the 35 USC 112 first paragraph rejections made in the final rejection. The portion relied upon by the examiner is *"A typical reason points out the differences between what is disclosed and what is claimed. A simple statement that "There does not appear to be a written description of the claim limitation '____' in the application as filed." may be sufficient where the support is not apparent and the applicant has not pointed out where the limitation is supported.".* The presumptively accurate disclosure was questioned by the examiner by specifically pointing to the portion of the claim at question and by stating that the specification did not have support for the limitation in question. In view of the above the examiner correctly followed MPEP 2163.04 when the 35 USC 112 first paragraph rejection was made.

In section 8.1.2 appellant alleges that the examiner expressly admits the disclosure is adequate when the examiner wrote in the double patenting rejection that the claimed invention was fully disclosed in the copending applications. The "fully disclosed" used in the nonstatutory double patenting rejection is a statement that the copending applications have the same specification. It is not an admission that the specification supports the claims at issue. Thus, the Board should not give weight to this argument.

In section 8.1.3 appellant refers to the 200 plus pages of specification and detailed schematic diagrams as being evidence that the claims are supported by the

specification. The examiner counters by stating that a lengthy and detailed specification is not proof that a newly drafted claim is supported by the specification. This specification was originally drafted in serial no. 06/662,211 filed on 10/18/84 and these claims were submitted on 10/21/96. Clearly that which is claimed now may not have been present in the 1984 specification and the 35 USC 112 first paragraph rejection proves that is the case. Appellant also refers to Table 1 located on page 25 of the Brief as specifying where in the specification support may be found for the claimed invention. This Table is merely a list of simply terms and does not list the complex combinations of elements claimed in the claims. Therefore the specification, while extensive, does not support the claims.

In section 8.1.4 appellant argues that certain claims are erroneously based upon unclaimed subject matter. Appellant does not point to which claims are at question so it is assumed that appellant is referring to claims 24, 34-37, 42-45, 49-51, 102-109, 115-118, 139-151, and 165-172. The Board should note this rejection is derived from the copending applications which explicitly claimed *an input weight circuit generating input weight information.* This element is very critical to the weight circuit for it loads important information into the weight tables from the described address generators, but, the specification does not describe nor suggest how the address generators will generate values which correspond to desired brightness values. Without the correct values in the weight tables then the pixel values applied to the weight tables will address incorrect brightness values resulting in a image with incorrect brightness values. Therefore, the rejection of what appears to be unclaimed limitations is actually necessary to the claim for support.

Thus, the 35 USC 112 first paragraph rejection of claims 24, 34-37, 42-45, 49-51, 102-109, 115-118, 139-151, and 165-172 is proper.

In section 8.1.5 raises numerous arguments and appellant actually attempts to correlate questioned limitations to portions of the specification. On page 23 and 24 appellant has made general allegations of broad disclosure for unspecified claimed limitations. On page 25 appellant has provided Table 1 which attempts to correlate individual words with locations in the specification. In the first paragraph on page 26 appellant has again made reference to broad disclosure as supporting the claimed invention. The same applies to the first paragraph on page 28. These arguments as well as Table 1 do not point to where in the specification support may be found for the claim elements specifically pointed out by the examiner as not being supported by the specification. Note A alleges that the disclosure describes memory technology while it does not attempt to correlate specifically the rejected limitation with a specific portion of the specification which may support the rejected limitation. Note B allegation is similar in structure to that of Note A. The filter and spatial argument is not persuasive for the same reason given for Note A. Note C alleges that a mere reference to "FFT" is sufficient to support the claim limitations rejected in the claims. Appellant has failed to realize that the mere mention of FFT on pages 33-34 does not prove that applicant had possession of the rejected limitation including the data operated on and produced by the rejected limitation. Note D alleges that the broad disclosure of a graphics processor overcomes the various graphics rejections made. This allegation is incorrect since the graphic processor described in the spec and in the program are not

the same as the rejected graphics. Note E alleges that there is support for the "%" integer declaration, "FIX" truncated integer arithmetic function, and "INT" integer arithmetic function. This argument does not support the truncation limitation because the part of the program supporting the truncation limitations uses the "%" declaration which according to the Microsoft Basic Reference Book (exhibit 3) in section 1.7 is clearly rounding and not truncation. Thus, this argument does not support any truncation limitations. Not all of the copending application claimed truncation. Note F alleges that the broad disclosure of weighting in the specification and weighting and scaling in the program FTR.ASC overcomes the various weight rejections made. This allegation is incorrect since the weight described in the specification and in the program are not the same as the rejected weight. In the second paragraph on page 28 appellant directs the examiner to review figure 6H which illustrates a weighting circuit. Appellant has failed to grasp that an address generator for loading the weight tables was not described to a level which will convey to one of ordinary skill in the art that appellant had a means to load the weight table with values that correspond to desired intensity values for each possible pixel value. Without the correct values in the weight tables then the pixel values applied to the weight tables will address incorrect brightness values resulting in a image with incorrect brightness values. The program FTR.ASC does not solve for the deficiency manifested by the detailed specification.

In section 8.1.6 appellant argues that the "making a product claims" are supported by the specification and appellant attempts to correlate the product made to "the disclosed apparatuses (e.g., circuits and devices) and the

disclosed signals", at page 30 last sentence. On page 31 last paragraph appellant alleged that appellant received a patent with "making a product" claims and appellant made reference to patent no. 5,584,032. An analysis of the patented claims reveals there were NO patented claims which claimed "making a product in response to". The examiner does not dispute appellants right to claim making a product but the product made should be claimed such that support for the product may be readily found in the specification. This is where appellant claims are lacking and appellant arguments fail to point to support for at least one specific product claim. Without adding more detailed limitations to the product claims or without a very specific argument the rejection of the product claims is maintained.

In section 8.1.7 appellant further argues for the making a product claims by alleging that circuit components support the making a product in response to information claims. Clearly the referenced circuitry is not made in response to the information made by the referenced circuitry.

In section 8.1.8 appellant lists in items a-j a summary of the items argued in sections 8.1 to 8.1.7 and they were addressed by the examiner in the rebuttal of each of sections 8.1-8.1.7 above. No more response is deemed necessary. On page 36 appellant has made general allegations that the examiner did not provide proper explanations in the 35 USC 112 rejection and alleged that evidence must be provided by the examiner and appellant makes reference to MPEP 2144.03. This position held by appellant is incorrect. The examiner has given extensive reasons why the claims are not supported by the originally filed specification and the examiner does

not need in a written description objection to provide a reference to support a holding that the claims do not convey that appellant had possession of the claimed invention at the time the original specification was filed.

Section 8.1.9 Conclusion. In view of the above rebuttal of sections 8.1 to 8.1.8 the examiner believes the written description rejections are proper and prays that they are sustained.

In sections 8.2 to 8.2.5 appellant contest the enablement rejections.

In sections 8.2.1 and 8.2.2 appellant directs attention to documents incorporated by reference portions of the specification. However, these documents and referenced portions of the specification do not provide the information needed by one of ordinary skill in the art to practice the alleged invention.

In section 8.2.3 appellant argues that the examiner ignored the skill in the art when making the nonenablement rejection. The skill in the art is shown by the documents listed by appellant on pages 43 and 44. The examiner has followed MPEP 2163.04 in making the 35 USC 112 first paragraph rejections made in the final rejection. The portion relied upon by the examiner is "*A typical reason points out the differences between what is disclosed and what is claimed. A simple statement that "There does not appear to be a written description of the claim limitation ' ___ ' in the application as filed." may be sufficient where the support is not apparent and the applicant has not pointed out where the limitation is supported.*". The disclosure was questioned by the examiner by specifically pointing to the portion of the claim at question and by stating that the specification did not have support for and did not enable the limi-

tation in question. In view of the above the examiner correctly followed MPEP 2163.04 when the 35 USC 112 first paragraph rejection was made.

In section 8.2.4 appellant summarizes the arguments presented in sections 8.2 to 8.2.3 and they were addressed by the examiner in the rebuttal of each of sections 8.2 to 8.2.3.

Section 8.2.5 Conclusion. In view of the above rebuttal of sections 8.2 to 8.2.3 the examiner believes the non-enablement rejections are proper and prays that they are sustained.

In section 8.3 appellant traverses the written description rejection. The examiner maintains that appellant did not have possession of the claims in question.

In section 8.3.1 appellant argues that the examiner is requiring a verbatim recitation of the terms found not to have any support in the specification. The examiner agrees that a verbatim recitation of claim limitations in the specification would be too stringent. However, the disclosure must support the claim limitations. In this case the specification does not support the claims which have limitations rejected for failure to convey that applicant had possession of the claimed invention, lack of adequate written description.

In section 8.3.2 appellant summarizes the arguments given in sections 8.3 and 8.3.1 and they were addressed by the examiner in the rebuttal of each of sections 8.3 and 8.3.1.

Section 8.3.3 Conclusion. In view of the above rebuttal of sections 8.3 and 8.3.1 the examiner believes the written description rejections are proper and prays that they are sustained.

In section 8.4 appellant briefly traverses the obvious-type and nonobviousness-type double patenting rejections.

In section 8.4.1 appellant argues that restriction requirements made in copending application prevent a double patenting rejection from being made. In the third paragraph of section 8.4.1 appellant refers to a parent application (08/034,627) and alleges that a 12 way restriction was made by the PTO in that application. It is not clear if this application is a result of that restriction. Appellant presents two inventions a and b for analysis. Appellant characterized each of those inventions as "a general data processing system". The claims in this application are "A memory system comprising". Clearly the invention claimed in this application is different from the invention restricted in the parent application. On page 54 both of the restriction requirements referenced to by appellant in two of the copending applications were made after the double patenting rejections were made in this application. Clearly restrictions after the fact did not force applicant to file this application as well as the eight copending applications. On page 55 last full paragraph appellant alleges that this application is a divisional, however, it should be noted that this continuation application is not the result of a restriction in the parent application and, as such, a double patenting rejection can be considered and can be made in this application. On page 56 appellant argues that a double patenting rejection may not be made because of the previous restriction requirement. This is not true. If this group of copending applications are claiming the same invention or an obvious variation of the same invention then restriction is proper. This rejection would not be proper if these applications are claiming non-obvious

inventions. Currently these applications are claiming the same invention in an obvious variation way.

In section 8.4.2 appellant argues that the claims in this application are independent and distinct from the claims in the copending applications. Appellant also refers to Exhibit 2 in which appellant has chosen to compare diverse claims rather than comparing the most similar claims. The Board is requested to compare:

claims of	serial no. corresponding to one level of claim detail
7, 8, 97, 98	08/479,088
4, 6, 96	08/471,712
7, 8, 83	08/479,086
22, 23, 84	08/471,702
23	08/479,087
7, 8, 9, 97	08/471,925
43, 112	08/472,062
3, 6, 91	08/483,016
25, 105	08/471,704 [*JB 4-21-00*]

with each other; and

claims of	serial no. corresponding to another level of claim detail
25, 102	08/479,088
25, 82	08/471,712
25, 82	08/479,086
25, 100	08/471,702

25, 52	08/479,087
25, 100	08/471,925
45	08/472,062
22, 94, 96	08/483,016

with each other.

A copy of these claims is attached to this answer. Clearly claims in this application claim the same obvious invention that is claimed in the copending applications

In section 8.4.3 appellant further argues about alleged differences between the claims in the copending applications and this application. After a review of the above listed claims it should be apparent that appellants arguments are incorrect.

In section 8.4.4 appellant stated that the examiner failed to make a limitation by limitation comparison of each of the claims in each of the copending applications. Such a comparison is not necessary. All that is needed is to compare similar claims in each of the applications. A limitation by limitation analysis of those claims is preformed when the claims listed above are compared to each other. It is not necessary to rewrite each of the claims here.

In section 8.4.5 appellant argues that simultaneous issue would obviate the double patenting rejections. This can not be done since the applications are not allowed.

In section 8.4.6 appellant summarizes the arguments presented in sections 8.4 to 8.4.5 and they were addressed by the examiner in the rebuttal of each of sections 8.4 to 8.4.5.

Section 8.4.7 Conclusion. In view of the above rebuttal of sections 8.4 to 8.4.5 the examiner believes the obvious-type and nonobviousness-type double patenting rejections are proper and prays that they are sustained.

In section 8.5 appellant argues against the obvious-type double rejections and alleges that the examiner has made an improper obvious-type double patenting rejection when the examiner referred to "minor differences between the claims in these nine applications" and stated that the minor differences "are obvious variations of the same claimed invention". However, when the above listed claims are compared it is clear that small variations exist between at least some of the claims in the copending applications.

In section 8.6 appellant argues against the nonobvious-type double rejections and alleges that the examiner is attempting to change the law. For the reasons give below it will be seen that the examiner is following current patent office policy.

In section 8.6.1 appellant alleges that Schneller is overruled by Vogel. Schneller rejections are described in MPEP 804 section B part 2. Thus, they are still valid law.

In section 8.6.2 appellant further alleges that Schneller was overruled sub silentio by Vogel. The examiner disagrees because the issues in Schneller were different than the issues in Vogel. In Schneller two applications described the same thing, ABCXY, while in Vogel different processes were described in two applications with the second application claiming the same process that the first application described. Since the technical relationship of the applications involved in Schneller does not correspond to technical relationship

of the applications involved in Vogel, Vogel could not overrule Schneller.

In section 8.6.3 appellant argues that even if Schneller is valid law, the claims are not rejectable because the same preferred embodiment is not being claimed in the copending applications. The examiner disagrees with this. The claims in these nine copending applications claim a memory system for storing image information and for processing the stored image information and for outputting the processed image information. Thus, it is clear that the same preferred embodiment is claimed in these nine applications.

In section 8.6.4 appellant alleges that the same preferred embodiment is not claimed in the nine copending applications. On page 77 second paragraph appellant states that this specification discloses many different inventions. The examiner does not dispute the fact that the specification is lengthy and that one would be able to draft claims directed to different inventions. However, in these nine applications the same obvious/nonobvious invention is being claimed. Therefore appellants remarks are not persuasive.

In section 8.6.5 appellant alleges that the facts in this application are different than the facts in Schneller. Appellant expounds upon this statement in sections 8.6.5.1 to 8.6.5.5.

In section 8.6.5.1 appellant alleges the facts in Schneller and these applications are different because of the lengthy specifications. However, it is not the issue is not the number of items in the specification but that the claims are claiming the same item in all of the applications. Thus, the facts in these applications correspond to the facts in Schneller.

In section 8.6.5.2 appellants alleges that this application and the eight copending applications disclose plural embodiments and each application claims one of those embodiments. The examiner disagrees because the claims in the nine applications are so close that they can not claim anything else but the same embodiment.

In section 8.6.5.3 appellant alleges that the 500 claims in this application and the eight copending applications proves that different inventions are claimed. While an analysis of the claims in the nine applications reveals that at least some of the claims in each of the applications claim the same obvious/nonobvious invention

In section 8.6.5.4 appellant alleges that the claims in the copending applications are not directed to a common preferred embodiment. This is not the case. After reviewing the claims in the nine copending applications it is clear that the same preferred embodiment is being claimed.

In section 8.6.5.5 appellant alleges that the Patent Office can not reject copending applications with Schneller for appellant alleges that the second application was filed after the first was patented. There is nothing in Schneller that limits Schneller based rejections to applications filed after a patent has been granted. The court in Schneller was concerned with the public being denied property for a time longer than a patentee is normally given. This concern would equally apply to applications filed while the patent was still pending as well as after the patent has been granted.

In section 8.6.6 appellant argues that it is improper to hold a claim to an element as extending the monopoly of a combination claim that included that element. How-

ever, this is not the issue in these claims for the claims in these cases claim the same system. Some claims are more broader and some are more narrower, but, in essence the same system is claimed in all of the nine copending applications.

In section 8.6.7 on page 86 lines 3-5 appellant alleges that the "Examiner's contention that the subject matter of the application claims is covered by the claims of the copending application is unsupported and just plain wrong". Appellant's position is clearly wrong. A side by side analysis of the claims clearly shows the claims in this application claim the same invention that is claimed in the copending applications in an obvious way.

In section 8.6.8 appellant summarizes the arguments presented in sections 8.4.2, 8.4.3, 8.4.4, and 8.6 to 8.6.7 and they were addressed by the examiner in the rebuttal of each of sections 8.4.2, 8.4.3, 8.4.4, and 8.6 to 8.6.7.

Section 8.6.9 Conclusion. In view of the above rebuttal of sections 8.6 to 8.6.7 the examiner believes the obvious-type and nonobviousness-type double patenting rejections are proper and prays that they are sustained.

In section 8.7 appellant states that "the art rejections do not, and in fact cannot, establish a prima facie case of either anticipation or obviousness". This statement is incorrect because the reference(s) relied upon do teach applicants invention and the examiner made statements in the final rejection supporting the holding of anticipation and obviousness. Thus, the examiner made a prima facie case of either anticipation or obviousness.

In section 8.7.1 appellant argues that a claim by claim analysis and a limitation by limitation analysis was not made in the final office action. Appellant refers to Getchter, Paulsen, Miller, and Warner as setting the rules for making a art rejections. Appellant alleges that the examiner failed to follow the rules set forth by these court cases. However, these court cases do not require the examiner rewrite the claims in an element by element comparison with the prior art, but, do require to the examiner to consider all of the limitations in each claim. A comparison of the claims with the prior art shows that all of the claimed elements are taught or suggested by the prior art.

In section 8.7.2 appellant asserts that the present examiner was previously reversed by the Board for similarly improper rejections. This statement is not entirely correct. Appellant should appreciate that in one of '881 or '886 the examiner was affirmed in part resulting in an amendment to the affirmed claims being made to overcome the affirmed prior art rejection. Therefore, the results of the '881 and '886 applications do not prove that the present examiner makes improper rejections.

In section 8.7.3 appellant makes reference to numerous board decisions which were favorable to appellant or had some favorable decisions for both the appellant and the examiner. For example in 07/357,570 the examiner was affirmed in part and reversed in part. Some of the art rejections were affirmed while others were reversed. Therefore, it is clear that all rejections of Hyatt claims are not reversed, just, some of them. It is not clear how the results of unrelated appeals affects the outcome of the claims in this application. The examiner has followed the rules in making the art rejections

and the only way they may be reversed is if the references do not teach or suggest the claimed invention.

Section 8.7.4? There is no section labeled 8.7.4.

Section 8.7.5 Conclusion In view of the above rebuttal of sections 8.7 to 8.7.3 the examiner believes the anticipation and the obvious rejections are proper and prays that they are sustained.

In section 8.8 appellant makes reference to the 35 USC 102 anticipation rejections.

In section 8.8.1 appellant makes reference to several federal circuit court cases. Kalman, Minnesota, and Spada are agreed with. Richardson is disagreed with because a prior art reference does not need to literally describe every element and interconnection of a claim because that which is understood to be a part of the described device is inherently a part of the disclosure of that device. In re Graves (CA FC) 36 USPQ2d 1697, 1701 (11/9/1995). Which made reference to In re LeGrice, 301 F.2d 929, 133 USPQ 365 (CCPA 1962) (A reference anticipates a claim if it discloses the claimed invention "such that a skilled artisan could take its teachings in combination with his own knowledge of the particular art and be in possession of the invention." Id. at 936, 133 USPQ at 372 (emphasis in original)). The statements in Graves were made in support of a 35 USC 102 rejection. Appellant further makes reference to a Board Decision quoting Judge Smith. This examiner would agree that a claimed specific structure for performing a claimed function is not anticipated by a different prior art structure for performing the same function. It is not clear how the quoted statement applies to the final rejection for the same claimed structure is described by the prior art reference.

In section 8.8.2 appellant has rewritten claims 22, 23, 82, 83, 84, 95, 99, 137, and 138 and has alleged that their limitations are not taught by Hill. Appellant has not pointed to any specific differences between Hill and the rejected claims. Appellant alleged to have excerpted from the claims limitations that distinguish over Hill. Appellant did not do this. Instead appellant has reproduced the rejected claims. Claims 22 and 23 are similar. The only difference being that claim 22 uses a frame buffer and claim 23 uses a pixel block memory. Claims 83 and 84 are similar. The only difference being that claim 83 uses a frame buffer and claim 84 uses a pixel block memory. Claims 83 and 99 are similar to claim 82 except that claims 83 and 99 have the additional limitations of outputting image information at a rate which is different than the input rate. Claims 83 and 99 are similar with both claims outputting image information at a rate different than the input rate with claim 99 outputting at a rate greater than the input rate. Claim 22 and Hill compare as follows. Hill teaches an image input circuit (col. 9 lines 30 & 31), a two dimensional frame buffer (164), an address generator (174), a writing circuit (167, 171), an accessing circuit (167, 169), a two dimensional processor (166), and an output circuit (168). Claim 23 and Hill compare as follows. Hill teaches an image input circuit (col. 9 lines 30 & 31), a two dimensional pixel block memory (164), an address generator (174), a writing circuit (167, 171), an accessing circuit (167, 169), a two dimensional processor (166), and an output circuit (168). Claim 82 and Hill compare as follows. Hill teaches generating input image information (col. 9 lines 30 & 31), storing an array of blocks (164), writing the array of blocks into a block memory (167, 171), generating a first clock signal having a first clock

rate (176), accessing blocks of pixel image information from the frame buffer (167, 168, 169), generating two dimensional processed image information (166), generating a second clock signal having a second clock rate that is different than the first clock rate (174), and generating output image information in response to the two dimensional processed image information (168).

In section 8.8.3 appellant argues that a prima facie case was not developed. Appellant is incorrect for the Hill reference teaches the claimed invention. Note the above analysis of Hill and the claims.

Section 8.8.4 Conclusion. In view of the above rebuttal of sections 8.8 to 8.8.3 the examiner believes the anticipation rejections are proper and prays that they are sustained.

In section 8.9 appellant traverses the 35 USC 103 rejections.

In section 8.9.1 appellant argues that hindsight is being used in the 35 USC 103 rejection. Appellant stated that the examiner must ascertain what would have been obvious to an artisan at the time of the invention was made and not to a layman. This was done in the rejection by the reliance upon prior art references which date prior to the time of appellants invention. Appellant also states that the references must provide the suggestion or motivation to combine. The rejection states why the references provide the suggestion and motivation to combine the references. Appellant states that the "claimed invention cannot be used as an instruction manual or template to piece together the teachings of the prior art so that the claimed invention is rendered obvious". This statement is correct. Appellant later alleges that "the Examiner, with knowledge of the Appel-

lant's invention, has picked and chosen a combination of references without expressing any motivation for doing so". This is not true for the final rejection set forth the motivation for combining the references.

In section 8.9.2 appellant argues that the examiner has failed to make the required analysis established in Grahm v. Deere. The rejection made by the examiner shows (1) the scope and content of the prior art in the references cited, (2) the differences between the prior art and the claims at issue in the body of the rejection, and (3) the level of ordinary skill in the art is shown by the cited references. Thus, appellants allegations are without support.

In section 8.9.3 appellant alleges that the claims distinguish over the applied references. Appellant has rewritten claims 19, 25, 96, 100, 101, 135, and 140 has alleged that their limitations are not taught by Hill, Lord, and Lelke. Appellant has not pointed to any specific differences between Hill and the rejected claims. Appellant alleged to have excerpted from the claims limitations that distinguish over Hill, Lord, and Lelke. Appellant did not do this. Instead appellant has reproduced the rejected claims. Thus, it is impossible to determine which limitations are not taught by the references because they are taught by the references.

In section 8.9.4 appellant argues that the examiner did not provide a prima facie case of obviousness. Appellant alleges that the Graham analysis was not followed, Appellant is incorrect for the rejection states the differences between the claims and the main reference. The rejection determines the skill level of the art with the references used in the rejection. The references themselves provide the motivation to modify the main

reference. Appellant further alleges that the examiner has failed to consider important claim limitations, has established novel differences between the claims and the references without establishing that these novel differences are obvious, and does not establish what is relied on in the references to teach or suggest each of the claim limitations. These arguments are not persuasive because the established important claim limitations are the argued novel differences and are what is relied upon in the references to teach or suggest the claim limitations.

Section 8.9.5 Conclusion. In view of the above rebuttal of sections 8.9 to 8.9.4 the examiner believes the 35 USC 103 obvious rejections are proper and prays that they are sustained.

In section 8.10 appellant alleges that the 112 first and the double patenting rejections are judicially estopped due to the wording used in the non-obviousness-type (Schneller) double patenting rejection which states that "subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter". The "fully disclosed" used in the rejection is not an admission that the claims are fully supported but a statement that the disclosures of the copending applications are identical. Thus, the similar claims in the copending applications are claiming the same invention. Patent law states that an applicant may receive only one patent for each distinct invention. Therefore, filing claims covering the same invention in many identical applications is prohib-

ited by patent law and may only be overcome by the filing of a terminal disclaimer.

In section 8.11 appellant alleges that the examiner has failed to provide a prima facie showing of why appellant should not be granted a patent. Appellant made reference to Judge Plager's concurring opinion in Oetiker. Plager stated the examiner has the initial burden of production and persuasion. Once this is done a prima facie case has been established. Appellant's position is wrong because the examiner did provide "production" and "persuasion" in each of the rejections made by the examiner. Thus, the examiner has provided a prima facie case of unpatentability.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/s/ JEFFERY A. BRIER
JEFFERY BRIER
PRIMARY EXAMINER

JAB
August 13, 1999

UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

IN RE APPLICATION OF
GILBERT P. HYATT

SERIAL NO. 08/471,702
DOCKET NO. 516
GROUP ART UNIT: 2775
EXAMINER: JEFFERY BRIER

Filed: June 6, 1995
[Received: Aug. 7, 2000]

REPLY BRIEF UNDER 37 CFR 1.193(B)

For: A DATA COMPRESSION SYSTEM

Hon. Assistant Commissioner For Patents
Washington, D.C. 20231

ATTENTION: Board of Patent Appeals and Interferences

May It Please The Honorable Board:

This is a Reply Brief in accordance with 37 CFR 1.193(b), submitted in response to the Examiner's Answer in the appeal from the final rejection of all claims

(claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172).

The Examiner's Answer is an extensive document that includes a significant re-development of the various issues. Hence, the Appellant has found it necessary to thoroughly respond to the re-developed issues.

TABLE OF CONTENTS

I. DISCUSSIONS COMMON TO ALL REJECTIONS 4

1.1 Introduction 4

1.2 The Examiner Concurs That The Claims Do Not Stand Or Fall Together But Then Violates This Position 5

1.3 The Examiner Defies The Federal Circuit By Refusing to Establish A Prima Facie Case 6

1.4 The Rejections Lack Integrity And The Examiner Even Admits To Making Misleading Statements 9

II. § 112-1 REJECTIONS 12

2.1 The Examiner Persists In § 112-1 Rejections That Are Based Upon Unclaimed Subject Matter Even When Thus Informed In The Appeal Brief 12

2.2 The Claims Of The Ancestor '032 Patent Establish That The Common Disclosure Adequately Discloses Instant Claimed Features 17

2.3 The Issue Of Being Fully Disclosed 19

2.4 Many Of The Examiner's § 112-1 Arguments Simply Do Not Make Any Sense 20

2.5 The Fact That The Appellant Reduced-To-Practice An "Experimental System" Is Very Significant To The § 112-1 Rejections 21

2.6 Each And Every One Of The § 112-1 Rejections Are Based Upon Nothing But Conclusory "Boilerplate" Statements 22

2.7 The § 112-1 Rejections Make Various Admissions About The Disclosure 23

2.8 The Examiner's Rebuttal To The Appeal Brief Establishes The Impropriety Of The § 112-1 Rejections 25

III. DOUBLE PATENTING REJECTIONS .. 32

3.1 The Controlling Law Establishes That The Provisional Double Patenting Rejections Must Be Reversed—Affirmance Is Legally Untenable 32

3.2 The Examiner Admits That Appellant's Claim Charts Are Pursuasive 38

3.3 The Examiner's Refusal To Address The Claim Differences Is Fatal To The Double Patenting Rejections ... 39

3.4 The Nonobviousness Double Patenting Rejections Are Fatally Defective 44

3.5 The Instant Schneller-Type Double Patenting Rejections Violate PTO Policy and Recent Board Decisions 46

3.6 The Examiner's Rebuttal To The Appeal Brief Establishes The Impropriety Of The Double Patenting Rejections 48

IV. ART REJECTIONS 51

4.1 The Examiner's Rebuttal To The Appeal Brief Establishes The Impropriety Of The Art Rejections 51

4.2 Distinctions Of The Claims Rejected Under § 102 Over Hill 53

4.3 Distinctions Of The Claims Rejected Under § 103 Over Hill, Lord, And Lelke .. 58

V. ORAL HEARING 63

VI. CONCLUSION 64

EXHIBIT—A
SIDE BY SIDE CLAIM COMPARISON

I. DISCUSSIONS COMMON TO ALL REJECTIONS

1.1 Introduction

The Appellant generated an Appeal Brief in response to the final Action. The Appeal Brief provided many facts and many citations to the law. After almost two years,[1] the Examiner finally generated an Answer which primarily repeated the final Action, substantially disregarding the Appeal Brief, and then provided rebuttal arguments in response to the Appeal Brief. However, these rebuttal arguments are primarily unsupported conclusory statements without factual or legal basis and hence cannot rebut the factual and legal arguments presented in the Appeal Brief. Much of the rebuttal is merely a table of contents and a summary of sections of the Appeal Brief. Hence, the Answer certainly cannot and does not establish a prima facie case any more than does the fatally defective final Action. See, e.g., the Appeal Brief at Sections 8.1.8, 8.2.4, 8.3.2, 8.4.6, 8.6.8, 8.7.3, 8.8.3, and 8.9.4 addressing the failure of the Examiner to establish a prima facie case.

Further, the Appeal Brief established that the § 112-1 and the double patenting rejections are judicially estopped and that the Appellant is entitled to a patent (Appeal Brief at Sections 8.10 and 8.11), but the Examiner did not adequately respond thereto. The response is effectively a challenge to the integrity of the rejections (Section 1.4).

---

[1] It is particularly notworthy that the draft of the Answer may have been generated a year ago, in August 1999. See Answer at 50.

1.2 The Examiner Concurs That The Claims Do Not Stand Or Fall Together But Then Violates This Position

The Appellant established that the claims do not stand or fall together[2] and the Examiner concurred therewith[3]. Nevertheless, the Examiner then inconsistently provides a few specific examples in support of the rejections and then rejects many claims altogether therewith.

After admitting that the Appellant's claim charts distinguish, the Examiner then proceeds to violate the principle that the claims do not stand or fall together by grouping all of the claims together with his few examples for double patenting and by grouping over 100 claims together that do not recite "simultaneous" in a § 112-1 rejection regarding disclosure of "simultaneous".

For example, the Examiner noted that two claims, claims 110 and 117, recite "simultaneous" and then he rejected over 100 claims that do not recite "simultaneous" under § 112-1 regarding disclosure of this unclaimed terminology (Answer at Sections 10.4-10.5 and Sections 1.4 and 2.1 herein).

As another example, the Examiner rejected all claims for provisional double patenting without a single claim pair comparison. The Applicant then provided

---

[2] See Appeal Brief at Section VII.

[3] "Grouping of Claims

Appellant's brief includes a statement that the claims do not stand or fall together and provides reasons as set forth in 37 CFR 1.92(c)(7) and (c)(8)."

See the Answer at 3, Section (3).

claim charts to show that the instant claims do not conflict with the copending claims[4] and the Examiner apparently agreed therewith[5]. But then the Examiner listed five instant claims (22, 23, 25, 84, and 100) as conflicting with 36 copending claims,[6] yet he rejected all of the instant claims based upon these five instant claims.[7] Because the claims do not stand or fall together and because the Examiner admits that many of the claim pairs are "diverse claims" (Answer at 37), the only instant claims that are relevant are the Examiner's listed five instant claims (22, 23, 25, 84, and 100) and the only copending claims that are relevant are the Examiner's listed 36 copending claims.

The Examiner is responsible for analyzing each and every claim where the Appellant has established that the claims do not stand or fall together. Nevertheless, the Examiner decided to short cut his responsibilities and grouped all of the claims together in supporting his rejections. The Board should not have to sort these out.

1.3 The Examiner Defies The Federal Circuit By Refusing To Establish A Prima Facie Case

The Examiner ignores the controlling law of the Federal Circuit regarding the disclosure being legally correct and presumptively valid and the MPEP confirmation thereof (Appeal Brief at 8.1.1 and Answer at 4-21

---

[4] See Appeal Brief at Exhibit-2.

[5] The Examiner stated "Appellant also refers to Exhibit 2 in which appellant has chosed to compare diverse claims rather than comparing the most similar claims". See the Answer at 37 (emphasis added).

[6] See Answer at 37-38.

[7] See Answer at 22-25.

and 28-29). See Marzocchi[8] and Gould[9]. See also MPEP 2164.04.

For example, totally disregarding the legally correct and presumptively valid nature of the disclosure and totally ignoring the details of the disclosure presented in the Appeal Brief at Sections 8.1.1, the Examiner relies entirely on unsupported conclusory "boilerplate" statements (Section 2.6 herein). He has never explained why he doubts the truth or accuracy of any statement in the disclosure nor to support his assertions with acceptable evidence or reasoning as required by Marzocchi, he has never provided the required "acceptable evidence or reasoning" as required by Gould, and he has never provided sufficient objective reasons to challenge the presumption of correctness of the disclosure as required by MPEP 2164.04.

The Examiner states—"Richardson is disagreed with . . ." (Answer at 44)—and the Examiner refuses to comply with Richardson. This is fatal to the § 102 rejections.

The pertinence of Richardson is discussed in the Appeal Brief at Section 8.8.1 and restated below:

The Federal Circuit further requires for a finding of anticipation that the same arrangement be literally present in the claim as it is in the reference and be shown in as complete detail as in the claim.

---

[8] In re Marzocchi, 439 F.2d 220, 223-24, 169 USPQ 367, 369-70 (CCPA 1967). (emphasis added).

[9] Gould v. Mossinghoff, 229 U.S.P.Q. 1, 13-14 (D.D.C. 1985), aff'd in part, vacated in part, and remanded sub nom. See also Gould v. Quigg, 822 F.2d 1074, 3 U.S.P.Q.2d 1302 (Fed. Cir. 1987).

> The district court correctly instructed the jury that an invention is anticipated if the same device, including all the claim limitations, is shown in a single prior art reference. Every element of the claimed invention must be literally present, **arranged as in the claim**. Perkin-Elmer Corp., 732 F.2d at 894, 221 USPQ at 673; Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 771-72, 218 USPQ 781, 789 (Fed. Cir. 1983), cert. denied, 465 U.S. 1026 [224 USPQ 520] (1984). The identical invention must be shown **in as complete detail as is contained in the patent claim**. Jamesbury Corp., 756 F.2d at 1560, 225 USPQ at 256; Connell, 722 F.2d at 1548, 220 USPQ at 198.

Richardson[10] (emphasis added). Hence, the required identity must also consider the recited coupling and the recited responsiveness in the claims.

The Examiner also erroneously refuses to consider the disclosure in the ancestor '032 patent in violation of the controlling law.[11] He argues that the claims are different and totally disregards the '032 disclosure. However, this is not the law, but rather the Examiner's own made-up rule. The presumption covers the disclosure as a whole. "A patent shall be presumed valid. . . . The burden of establishing invalidity of a patent or any claim thereof shall rest on the party asserting such invalidity." (35 USC § 282-1, emphasis added). Further, the claims in the '032 disclosure cover issues relevant to the instant application (Section 2.2 herein).

---

[10] Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), cert. denied, 110 S. Ct. 154 (1989).

[11] The ancestor '032 patent has the same disclosure in pertinent part as in the instant application.

While the Examiner says that he followed MPEP 2163.04, he in fact violated this section of the MPEP. This provision is permissive if and only if "the support is not apparent and the applicant has not pointed out where the limitation is supported." However, the support is apparent,[12] the Examiner himself admits to much of the support, and the Appellant has clearly pointed out where each of the limitations are supported[13]. The Examiner blatantly admits to violating the law of the Federal Circuit and the MPEP:

> The presumptively accurate disclosure was questioned by the examiner by specifically pointing to the portion of the claim at question and by stating that the specification did not have support for the limitation in question.

See Answer at 29. However, pointing out the portion of a claim and making a self-serving unsupported conclusory statement does not satisfy the law—it violates the law.

1.4 The Rejections Lack Integrity And The Examiner Even Admits To Making Misleading Statements

In order to support the nonobviousness double patenting rejections, the Examiner admitted that the disclosure is adequate:

---

[12] See the table of contents attached as Exhibit-1 to the Appeal Brief.

[13] See, e.g., Appeal Brief at Sections V, 8.1.5, and 8.2.1 and Table-1 on page 25. See also, e.g., Section 2.9 herein.

> The subject matter claimed in the instant application is fully disclosed in the referenced copending application . . . .

See the Appeal Brief at Section 8.1.2 and the final Action at pages 26-27 (emphasis added). **Then, when the Appellant relied on what the Examiner said**, the Examiner says that he didn't mean what he said (Answer at 29 and 49). Clearly, the Examiner recited Schneller cliches without any concern for what they mean or the correctness thereof (Appeal Brief at Section 8.6.7). Hence, the nonobviousness double patenting rejections should be reversed as lacking integrity and being prima facie erroneous.

The above situation is just the type of scheme that the Federal Circuit prohibits under the doctrine of judicial estoppel.[14] The Examiner is prohibited from assuming contrary positions. Just as the Federal Circuit explained in Sears, the Examiner here is playing fast and loose with the courts. See Appeal Brief at Section 8.10. Hence, for this reason alone, the § 112-1 rejections and the nonobviousness double patenting rejections should be reversed. Similarly, for this reason alone, the art rejections and the § 112-1 rejections should be reversed. See Appeal Brief at Section 8.10.

There can be no question that nonobviousness double patenting rejections require the disclosure in the prior patent to provide § 112-1 support for the contested claims. Otherwise the basic premise in Schneller, that

---

[14] Davis v. Wakelee, 156 U.S. 680, 689 (1895); see also U.S. Philips v. Sears Roebuck & Co., 55 F.3d 592, 596 (Fed. Cir. 1995), cert. denied, 116 S. Ct. 567, and cert. denied, 116 S. Ct. 672 (1995).

the contested claims could have been patented in the parent patent, would not be satisfied. However, such a position is fundamentally inconsistent with a § 112-1 rejection on the same or similar disclosures. Therefore, persisting in the nonobviousness double patenting rejections overcomes the § 112-1 rejections and persisting in the § 112-1 rejections overcomes the nonobviousness double patenting rejections.

The Examiner erroneously tells this Board that the application does not disclose certain features **at all** (Answer at 4-21); e.g., "simultaneous" accessing from and writing to memory (Sections 1.4 and 2.1 herein). However, the Appellant expressly pointed out where these features can be found in the disclosure and the extensive details thereof in the disclosure.[15] At a widely separated location in the Answer, the Examiner finally admits to significant disclosure; but qualifying this admission by stating that "the 200 plus pages of specification and detailed schematic diagrams . . . is not proof" and that citations to the verbatim terminology in the specification "is merely a list". Then, the Examiner makes a remarkable unsupported, self-serving, and conclusory statement that "[t]herefore the specification, while extensive, does not support the claims." (Answer at 29-30). This is an extreme example of the improper rejections prohibited by the Federal Circuit—disregarding extensive disclosures, "detailed schematic diagrams", and verbatim disclosures and relying instead on self-serving, unsupported, and conclusory statements.

The Examiner's complaint that "the 200 plus pages of specification and detailed schematic diagrams is not

---

[15] See, e.g., Appeal brief at Sections V, 8.1.5, and 8.2.1 and Table-1 on page 25.

proof" further violates the law of the Federal Circuit. It is the Examiner that must provide "acceptable evidence or reasoning" because the disclosure is "presumptively accurate" (Appeal Brief at Section 8.1.1). Erroneously denying that such disclosure even exists and trying to place the Examiner's burden on the Appellant is improper. The extensive disclosures, "detailed schematic diagrams", and verbatim disclosures are prima facie adequate in the absence of "acceptable evidence or reasoning" from the Examiner.

As discussed in the Appeal Brief at Section 8.10, the Examiner is improperly playing "fast and loose" with the rejections. This scheme now continues in the Answer. As discussed in the Appeal Brief, under the doctrine of judicial estoppel, where a party assumes a certain position, he may not thereafter assume a contrary position.[16] As the Federal Circuit explained in Sears, judicial estoppel is designed to preserve the integrity of the judicial process by "protecting against litigants who 'play fast and loose with the courts.'" Id. at 596-97.

The Examiner's integrity is in question. First he says that the claims are fully disclosed, then he says that he didn't mean it, he just has to say it to support the rejection. Otherwise stated, for this additional reason, the Board should reverse the Schneller-type double patenting rejections and § 112-1 rejections because of the lack of integrity of these rejections and because this scheme is judicially estopped.

---

[16] Davis v. Wakelee, 156 U.S. 680, 689 (1895); see also U.S. Philips v. Sears Roebuck & Co., 55 F.3d 592, 596 (Fed. Cir. 1995), cert. denied, 116 S. Ct. 567, and cert. denied, 116 S.Ct. 672 (1995)

II. § 112-1 REJECTIONS

2.1 The Examiner Persists In § 112-1 Rejections That Are Based Upon Unclaimed Subject Matter Even When Thus Informed In The Appeal Brief

The Examiner rejects many claims under § 112-1 for terminology that is not recited in the claims. Remarkably, these subject features (although unclaimed) are adequately disclosed in the application. Then the Examiner ignores the portions of the Appeal Brief that informed him of the fundamental premises (a) that rejections based upon unclaimed terminology violate § 112-1[17] and (b) that the subject terminology (even though unclaimed) is adequately disclosed with express citations to the specification[18].

The Examiner ignores an inherent principle in patent law—a claim cannot be rejected under § 112-1 regarding disclosure of terminology that it does not recite. The Examiner was informed about this fundamental principle in the Appeal Brief, but he ignored it in the Answer.

Even worse, the Examiner recognizes and admits to intentionally basing the § 112-1 rejections on unclaimed subject matter—"[t]herefore, the rejection of what appears to be unclaimed limitations is actually necessary to the claim for support." (Answer at 30). **Yet worse**, the Examiner appears to reject claims in the instant

---

[17] See Appeal Brief at 21, Section 8.1.4 entitled "The '112-1 Rejections Are Erroneously Based Upon Unclaimed Subject Matter".

[18] See Appeal Brief at 23, Section 8.1.5 entitled "The Examiner Alleges Insufficient Disclosure While Ignoring Hundreds Of Relevant Recitations In The Disclosure". See also Appeal Brief at 25, Table-1 citing to the specification for subject terminology.

application for features claimed, not in the instant application, but in copending applications—"[t]he Board should note this rejection is derived from the copending applications which explicitly claimed an input weight circuit generating input weight information." (Answer at 30, emphasis in original). It is not clear if this is a new concept created by the Examiner—a provisional § 112-1 rejection derived from the prohibited provisional double patenting rejections over copending applications (Section 3.1). The Examiner does not explain this issue.

Yet still worse, all of this fuss is concerning reading information to and writing information from a memory which is, in general, so well known that it is unbelievable that the Examiner would even mention such a consideration even if there was no reading and writing disclosure at all, much less in view of the extensive detailed disclosure in the instant application of reading from and writing to a memory. See, e.g., Spec. at 25-62 and 128-135 and particularly Spec. at 36-43 and Figs. 6E-6N for reading and writing disclosure regarding the image memory and see, e.g., Spec. at 136-164 and particularly Spec. at 162-164 and Figs. 6W-6AH and particularly Fig. 6AH for reading and writing disclosure regarding the weight memory. See also, e.g., Spec. at 11-22, 185-186, and 214-236 and Fig. 7A for an actually reduced-to-practice computer program that discloses in extensive detail generation of and reading and writing of image information, weight information, scale factor information, and other information.

And probably worst of all, the Examiner now questions the values of the weights stored in the memory—"[w]ithout the correct values in the weight tables then the pixel values applied to the weight tables will address

incorrect brightness values resulting in a[n] image with incorrect brightness values." (Answer at 30). But the Examiner totally ignores the specific weight values disclosed in the computer program (Spec. at 232, lines 170-200 and 260-340), totally ignores the section in the specification addressing loading of weight information from the computer (Spec. at 232, lines 130-340 and Spec. at 178 and 185-18), and totally ignores the skill in the art regarding generation of weight values. All of this fuss is about unclaimed terminology, which incidentally is adequately disclosed in the application. The Examiner should have, but did not, concentrate on claimed features that are not disclosed, but he could not and he did not because the claimed features are adequately disclosed.

Further, the Examiner ignored the Appellant's citation to the disclosure for the relevant recitations of the terminology.[19]

For example, the Examiner rejected over 100 claims that **do not** recite "simultaneous" memory accessing and writing terminology under §112-1 for lack of disclosure of "simultaneous" terminology[20] while ignoring the Appellant's citations to "simultaneous" terminology in the specification[21] and ignoring the extensive supporting disclosure for this "simultaneous" terminology regarding memory accessing and writing. This "simultaneous" disclosure issue is further discussed below.

---

[19] See, e.g., Appeal Brief at Sections V, 8.1.5, and 8.2.1 and Table-1 on page 25.

[20] See Answer at pages 6-7, paragraphs 10.4 and 10.5.

[21] See Appeal Brief at 25, Table-1 stating:

"simultaneous . . . [pages] 36, 45, 46, 50,".

Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, 95-109, 111, 112, and 118 stand rejected under § 112-1 regarding unclaimed subject matter (Answer at 6-7, paragraphs 10.4 and 10.5)— "simultaneous". Notwithstanding the irrelevance of such unclaimed disclosure, "simultaneous" reading and writing are disclosed in great detail. See Appeal Brief at 8.1.5, Table-1, Spec. at 25. In fact, whole sections of the specification deal with the reading from and the writing into the disclosed memory. See, e.g., the sections entitled Re-addressing and Scanout Memory Architecture (Spec. at 36-43) and Figs. 6E-6N.

All claims stand rejected regarding the following terminology:

> ". . . a writing circuit and an accessing circuit for writing and reading a block of video pixel image data into the block memory or the process of writing and reading a block of video pixel image data into the block memory."

See Answer at 6-7, paragraphs 10.4 and 10.5. However, claims 4, 7, 14, 95, 96, 97, 99, 100, and 101 do not recite "writing"; claims 17, 18, 19, 22, 34, 42, 43, 49, 50, 51, 81, 83, 102, 104, 106, and 108 do not recite a "block memory"; and claims 17, 18, 19, 20, 22, 23, 24, 25, 34, 35, 36, 37, 42, 43, 44, 45, 49, 50, 51, 52, 81, 82, 83, 84, 85, 95, 96, 97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 108, and 109 do not recite "video".

Notwithstanding the irrelevance of such unclaimed features, these features are adequately disclosed in great detail.[22]

---

[22] See, e.g., Appeal Brief at Sections V, 8.1.5, and 8.2.1 and Table-1 on page 25.

The Board is requested to take notice that the disclosures cited to in Table-1 of the Appeal Brief relate to the verbatim recitation of the terminology. However, the lengthy application provides extensive additional disclosure of the detailed implementation of these features. For example, the "simultaneous" accessing and writing terminology characterizes the Re-addressing and Scanout Memory Architecture (Spec. at 36-43) and Figs. 6E-6N showing detailed memory disclosure down to the wire and component level of detail that implements this feature. See also Spec. at 36 lines 1-5 (emphasis added):

> Re-Addressing And Scanout Memory Architecture
>
> Multiple dimension image memory architecture, as previously discussed, **involves simultaneous accessing** of multiple pixels, such as in a 2-dimensional X/Y array, to increase effective memory speed.

Further, the Examiner rejects over 100 claims for terminology that he admits is not recited in these claims. This is notwithstanding the fact that this unclaimed terminology is adequately and extensively disclosed in the instant application.

Claims 24, 34-37, 42-45, 49-51, 102-109, 115-118, 139-151, and 165-172 stand rejected under § 112-1 regarding unclaimed subject matter (Answer at 13-16, paragraphs 10.16 and 10.17). Even worse, the Examiner admits that these claims stand rejected based upon unclaimed subject matter even after being informed in the Appeal Brief at Section 8.1.4 that such a rejection is inappropriate. The Examiner states:

> No claims in this application directly claim an input weight circuit generating input weight information
>
> . . . .

See Answer at 13 and 15. But the Examiner rejects these 45 claims on this admitted unclaimed subject matter—"[a]n input weight circuit generating input weight information is not supported by the specification." See Answer at 14. Notwithstanding the irrelevance of such unclaimed disclosure, such features are disclosed in great detail. See Fig. AH and Spec. at 162-164, where the weight memory is shown as RAM chips U21E, U22E, and U23E (Fig. AH), the weight addressing is the circuits that generate the signals to address input pins A0-A9 of these RAM chips, and the weight information is the circuits that generate the signals to data input pins IO0-IO3 of these RAM chips. See also Answer at 14 where the Examiner admits to the significant disclosure of such features in Figs. 5A and 6O-6R and in the Spec. at 118-127, 142, 147, 149, and 162.

Claims 24, 34-37, 42-45, 49-51, 102-109, 115-118, 139-151, and 165-172 stand further rejected under § 112-1 regarding additional unclaimed subject matter (Answer at 13-16, paragraphs 10.16 and 10.17)—"an address generator which will generate weight addresses and . . . an address generator which will apply the weight addresses to the inputs of RAMS U5E and U6E at the same time the intensity bits are being applied to RAMS U3E and U4E." (Answer at 14-15, bridging sentence).[23] However, these claims do not recite such limi-

---

[23] The Examiner does not cite to a particular figure for RAMS U5E and U6E. The Weight RAMS are type-2149H RAM chips designated U21E, U22E, and U23E shown in Fig. AH. See Spec. at 162-164.

tations. Notwithstanding the irrelevance of such unclaimed disclosure, such features are disclosed in great detail. See Figs. 6AH and 7A and Spec. at 18-22, 162-164, 231-236. See also Answer at 14 where the Examiner admits to the significant disclosure of such features in Figs. 5A and 6O-6R and in the Spec. at 118-127, 142, 147, 149, and 162.

Claims 2-14, 113, 114, and 120-132 stand rejected under § 112-1 regarding unclaimed subject matter (Answer at 20, paragraph 10.25)—"a quantization weighting processor." Notwithstanding the irrelevance of such unclaimed disclosure, such features are disclosed in great detail. See Appeal Brief at Sections V and 8.1.5, Table-1, Spec. at 25.

Claim 95 stands rejected under § 112-1 regarding unclaimed subject matter (Answer at 10-11, paragraphs 10.10 and 10.11)—"a spatial processor . . . ." Notwithstanding the irrelevance of such unclaimed disclosure, such features are disclosed in great detail. See Appeal Brief at Sections V and 8.1.5, Table-1, Spec. at 25. See the section entitled "SPATIAL FILTERING", Spec. at 15-24 and Figs. 5A-5C and 7A, and the section entitled "Weight Logic", Spec. at 162-164 and Fig. 7AH.

2.2 The Claims Of The Ancestor '032 Patent Establish That The Common Disclosure Adequately Discloses Instant Claimed Features

The instant application must be presumed to be sufficient both (a) because the law of the Federal Circuit establishes that the instant disclosure is presumptively correct (Appeal Brief at 8.1.1) and (b) because the instant disclosure is common in pertinent part with the disclosure in the '032 ancestor patent (Appeal Brief at

Section 8.1.1). However, the Examiner totally disregards the '032 patent based upon the erroneous contention that the claims in the instant application and the '032 patent are different. The similarity between the claims are discussed below.

The '032 patent is directed to a kernel processor, disclosed and claimed as a spatial filter with weighting and scaling. Although the instant claims do not expressly recite a kernel processor, the disclosure of the kernel processor that is presumptively correct in the '032 patent also supports the spatial processing in the instant application.

Many of the instant claim features objected to by the Examiner under § 112-1 are recited in the claims of the '032 ancestor patent and hence have an even stronger presumption of being legally correct and valid. For example, the following table identifies the instant claim features objected to by the Examiner under § 112-1 that are recited in the claims of the '032 ancestor patent.

INSTANT CLAIM FEATURE	'032 PATENT CLAIMS	ANSWER SECTION(S)
spatial[24]	1-3, 5-9, 11-15, 17-20, 43	10.10
weight	6, 12, 18, 28	10.16
making a product	32, 34, 40, 42	10.26, 10.27

[24] The cited claims in the '032 ancestor patent recite "spatially filtered" while the subject rejection of the Examiner in the instant application is to "a spatial processor".

It is particularly noteworthy that the terminology "making a product" that the Examiner objects to in the instant claims is expressly recited in four claims of the '032 ancestor patent (patent claims 32, 34, 40, and 42), which patent has the same disclosure in pertinent part as the instant application. Thus, the instant disclosure must be considered to provide adequate § 112-1 basis for the instant "making a product" claim recitations. For this reason alone, notwithstanding the reasons set forth in the Appeal Brief at Sections 8.1.6-8.1.7 and in Section 2.8 herein, the rejection of instant claims 153-172 for making a product terminology (Answer at Sections 10.26 and 10.27) must fall.

The Examiner, remarkably, questions the statututory presumption. Section 282 establishes that a patent is presumed valid. Thus, what is claimed in the patent must be presumed to be correct, what is disclosed in the patent must be presumed to be correctly and sufficiently disclosed, and the burden is on the Examiner to establish otherwise (see § 282). See also Appeal Brief at Section 8.1.1 for the law of the Federal Circuit regarding this issue. But the Examiner relies only on conclusory statements in rebuttal to § 282. Because all of the terms objected to by the Examiner under § 112-1 are used in the '032 patent disclosure and similarly in the instant disclosure which is common (see Table-1 in the Appeal Brief at 25), all of these terms must all be presumed to be correctly and sufficiently disclosed and the § 112-1 rejections, based only on the Examiner's conclusory statements, should be reversed.

2.3 The Issue Of Being Fully Disclosed

The Examiner stated that the instant claims are "fully disclosed in the referenced copending application" (Appeal Brief at Section 8.1.2). Because these copending applications have the same disclosure as the instant application," the instant claims are also fully disclosed in the instant application. Hence, as discussed in Section 8.1.2 of the Appeal Brief, the '112-1 rejections must fall. Now the Examiner says that his statement is not true, that the instant claims are not fully disclosed in the copending applications (Section 1.4 herein and the instant section). However, the Examiner cannot have it both ways—since the disclosure is a matter of fact, the claims cannot be fully disclosed for a Schneller double patenting rejection and then mystically converted to be insufficiently disclosed for a § 112-1 rejection. Clearly, the claims are adequately disclosed even without the Examiner's "fast and loose"[25] position regarding Schneller.

2.4 Many Of The Examiner's § 112-1 Arguments Simply Do Not Make Any Sense

The Examiner makes senseless arguments in support of the § 112-1 rejections. A few representative examples are discussed below.

Answer at 10.5

The Examiner rejects . . . [more than 100] claims for "simultaneous" writing and reading (accessing) terminology while implicitly admitting to the fact that only

---

[25] See Appeal Brief at Section 8.10—judicial estoppel is designed to preserve the integrity of the judicial process by "protecting against litigants who 'play fast and loose with the courts.'"

claims 110 and 117 actually recite "simultaneous" terminology. Even worse, the Examiner admits that claims 112 and 118 solve the "accessing" problem (although he contends that they do not solve an alleged "writing" problem), but neither claim 112 nor claim 118 recites either "writing" or "simultaneous" at all, instead they recite "sequentially accessing". And still worse, claims 112 and 118, which the Examiner expressly admits solve the alleged accessing problem and which do not recite "simultaneous" or "writing" at all, stand rejected with the group of more than 100 claims under § 112-1 for "simultaneous" terminology that claims 112 and 118 do not recite and that the Examiner admits is not recited in claims 112 and 118. And still worse, the Examiner ignores the fact that this "simultaneous" terminology finds adequate antecedent basis in the disclosure at pages 36, 45, 46, and 50 as pointed out by the Appellant.[26] And worst of all, the disclosure provides in extreme detail[27] an actually reduced-to-practice system that **simultaneously** accesses from memory and **simultaneously** writes into memory a block of 64-pixels, disclosed down to the individual IC component and individual wire level of detail.[28]

---

[26] See Appeal Brief at 25, in Table-1 under the term "simultaneous".

[27] See, e.g., Appeal Brief at 9-13 and 38-40 (Sections V and 8.2.1).

[28] See Appeal Brief at Section V. See particularly Appeal Brief at 12.

In addition, extremely detailed tables of cabling and component placement (Spec. at 138-213) and computer source programs (Spec. at 214-36) are located near the back of the specification.

2.5 The Fact That The Appellant Reduced-To-Practice An "Experimental System" Is Very Significant To § 112-1

The Appellant actually reduced to practice and disclosed in detail an "experimental system". The Examiner, however, has ignored the disclosure of this "experimental system" and therefore has failed to establish a prima facie case. For a summary of this disclosure, see Appeal Brief at 9-13, Section V entitled "SUMMARY OF THE INVENTION".

According to the Deputy Assistant Commissioner for Patent Policy, and Projects,[29] such a reduction-to-practice is particularly relevant to the issue of § 112-1.

> If a specification demonstrates actual reduction to practice by showing that the inventor constructed an embodiment or performed a process that met all the limitations of the claim and determined that the invention would work for its intended purpose, one skilled in the art would clearly recognize that the applicant was in possession of the claimed invention.

The Assistant Commissioner cites to Cooper[30] for an authority.

In view of the above, the Examiner has ignored this very important evidence and hence, for this reason alone, the § 112-1 rejections should be reversed.

---

[29] Stephen G. Kunin, "Written Description Guidelines and Utility Guidelines," Journal of the Patent and Trademark Office Society (JPTOS), Vol. 82, No. 2 at page 86 (February 2000).

[30] Cooper v. Goldfarb, 154 F.3d 1321, 1327, 47 USPQ2d 1896, 1901 (Fed. Cir. 1998).

2.6 Each And Every One Of The § 112-1 Rejections Are Based Upon Nothing But Conclusory "Boilerplate" Statements

Each and every one of the § 112-1 rejections (Answer at 4-21) are based upon nothing more than conclusory "boilerplate" statements. These rejections do not give a shred of factual information about the rejection, merely reciting uninformative cliches without any support. These rejections do not explain why the Examiner doubts the truth or accuracy of any statement in a supporting disclosure nor back up assertions "with acceptable evidence or reasoning" as required by the CCPA in Marzocchi.[31] See Appeal Brief at Section 8.1.1. Further, these conclusory statements do not properly address the Appellant's factual and legal showing in the Appeal Brief concerning the specific disclosure in the instant application.[32] For example, the Examiner states:

> 10.4 Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, and 95-172 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 1-14, 17-20, 22-25, 34-37, 42-45, 49-52, 81-85, 95-112, 117, and 118 claim a writing circuit and an accessing circuit for writing and reading a block of video pixel image data into the block memory or the

---

[31] In re Marzocchi, 439 F.2d 220, 223-24, 169 USPQ 367, 369-70 (CCPA 1967).

[32] See, e.g., Appeal Brief at Sections V, 8.1.5, and 8.2.1 and Table-1 on page 25.

> process of writing and reading a block of video pixel image data into the block memory. These claims cover simultaneous writing and reading of a block of graphic image data (note claims 110 and 117). Claims 112 or 118 solve the accessing problem but does not solve the writing. The specification does not describe this. This claimed feature was not described in the specification at the time of filing this application nor at the time of filing parent application serial no. 06/662,211. The specification describes a sequential write to and read from the block memory. Thus, applicants originally filed specification does not manifest that applicant had possession of the currently broadly claimed invention at the time of filing. In re Wilder, 222 USPQ 369, (CAFC June 20, 1984). In re Ghiron and Ulrich, 169 USPQ 723, (CCPA May 20, 1971). Vas-Cath inc. v. Mahurkar, 19 USPQ 2nd 1111, (CA FC, 6/7/91).

See Answer at 6-7.

Still further, these conclusory statements are just plain wrong. See Sections 1.4 and 2.1 herein for an analysis of the above Section 10.4 statement.

2.7 The § 112-1 Rejections Make Various Admissions About The Disclosure

The Examiner admits that he does not require a verbatim disclosure:

> In section 8.3.1 appellant argues that the examiner is requiring a verbatim recitation of the terms found not to have any support in the specification. The examiner agrees that a verbatim recitation of claim

limitations in the specification would be too stringent.

See Answer at 35. However, the Examiner does not clarify the reason that the extensive antecedent basis in the disclosure, including actual verbatim antecedent basis, is not acceptable. The Examiner provides only unsupported conclusory statements that are uninformative and of no guidance to the Board or the Appellant.

The § 112-1 rejections make various admissions about the disclosure. These admissions are excerpted below.

> 10.1 The claims of this application are directed to the portions of the specification which describe a vector memory storing vectors, reading the vectors from the vector memory, sending the read vectors to the address generators, strobing (writing) color values into image memory at the locations defined by the address generators, reading the image memory during display system readout, storing the readout values in a buffer memory, applying in parallel 9 pixels of information from the buffer memory to a spatial filter, applying the spatially filtered pixel information to a digital to analog convertor, and sending the analog signal to a monitor. . . .
>
> 10.2 . . . This specification briefly describes compressing database images and data compression. . . . The specification at page 23 lines 1-18 states "Image processing can be performed on digitized images stored in the database. A stored image can be loaded from the database into image memory for image processing online with a hardware-implemented image processor. A stored image can be

preprocessed; such as offline in the database and such as online with a preprocessor. Offline processing can be performed during database generation, such as filtering database images before storing the images in the database. Online preprocessing can be performed during system operation, such as by accessing database images and preprocessing the accessed database images with compression and filtering, prior to loading into image memory. Offline preprocessing can be performed for filtering of images, which is illustrative of other forms of offline preprocessing and is also illustrative of online preprocessing. For example, other forms of offline preprocessing includes data compression, image enhancement, and other forms of filtering. Also, other forms of online preprocessing includes data decompression, image expansion, image compression, and filtering."

. . .

10.4 . . . Claims 112 or 118 solve the accessing problem . . . . The specification describes a sequential write to and read from the block memory.

. . .

10.5 . . . Claims 112 or 118 solve the accessing problem . . . . The specification describes a sequential write to and read from the block memory.

. . .

10.16 . . . The specification at page 147 lines 12-17 and figures 6Y and 6Z teach applying addresses through multiplexers U5C and U6C to the address inputs of RAMs U5E and U6E so these RAMs may store weight addresses supplied on input lines IO0 to IO3 from address generators. The same lines of page 147 describe the line buffers U4F to U6F as

applying the intensity bits from image memory to RAMs U3E and U4E and applying the weight addresses from the address generators to RAMs U5E and U6E. Page 142 lines 13 to 29 and figure 6X describe an address counter for generating the addresses to be applied to the address lines of RAMs U3E, U4E, U5E, and U6E so these RAMs will be able to store the intensity and weight addresses at storage locations determined by the addresses. Page 149 lines 1-9 describes reading the weight addresses from RAMs U5E and U6E and applying those weight addresses on a weight bus. Page 162 lines 5-7 describes outputting the weight addresses stored in the line buffers to the weight RAMs U21E to U23E for accessing of the weights associated therewith in order for those weights to be applied to the spatial filter (spatial filter shown in figure 5A). Page 12 lines 1-6 describes using address generators for performing a vector to raster conversion by using the address generators to step through addresses and by strobing a color value into each memory location represented by each address of the generated addresses. Pages 118 to 127 and figures 6O to 6R describes address generators for generating addresses. Applicant has failed to describe an address generator which will generate weight addresses and has failed to describe an address generator which will apply the weight addresses to the inputs of RAMs U5E and U6E at the same time the intensity bits are being applied to RAMs U3E and U4E. This portion of .applicants specification is critical in supporting the claimed invention because each weight address associated with an intensity value for a pixel must select a weight value from the weight table which will per-

> form the correct filtering of a matrix of pixels in the spatial filter in order for the desired filtered image to be generated. . . .

See Answer at Sections 10.1, 10.2, 10.4, 10.5, and 10.16 (emphasis added).

2.8 **The Examiner's Rebuttal To The Appeal Brief Establishes The Impropriety Of The § 112-1 Rejections**

The Examiner's rebuttal to the Appeal Brief establishes the impropriety of the § 112-1 rejections.

The Examiner admits that Section 8.1.5 of the Appeal Brief "actually attempts to correlate questioned limitations to portions of the specification . . . . Table 1 which attempts to correlate individual words with locations in the specification." (Answer at 31). This is an unfair characterization because there is much more than an "attempt". Further, the extensive detail regarding the disclosure in the Appeal Brief at Section V has been totally ignored in the Answer. The Appeal Brief provides a discussion of the extensive disclosure, disclosure of an actual reduction-to-practice system (the importance of which is addressed in Section 2.5 herein), detailed schematic diagrams down to the component and wire level of detail with discussions thereof for the actual reduction-to-practice system, and citations to verbatim recitations of the contested terminology in the specification. However, the substance of these discussions have been ignored by the Examiner.

The Examiner unfairly and erroneously criticizes the disclosure as a "broad disclosure" (Answer at 31), whatever that is supposed to mean. There can be no question that the disclosure is extensive with "detailed schematic

diagrams", with verbatim statements of the contested claim features, and with disclosure of an actually reduced-to- practice system. In this context, what is the term "broad disclosure" supposed to mean and how does it support the § 112-1 rejections?

The Examiner unfairly and erroneously makes critical statements regarding the Appeal Brief such as "general allegations of broad disclosure for unspecified claim limitations" and "broad disclosure as supporting the claimed invention" (Answer at 31). However, these are unsupported conclusory statements that are erroneous on their face, the disclosure is extensive and detailed and the Appeal Brief fairly describes the disclosure in the context of the claimed invention. See, e.g., Table-1 at page 25 of the Appeal Brief. This appears to be an excuse for ignoring the extensive disclosure and the associated discussions in the Appeal Brief.

The Examiner takes the erroneous position that Table-1 does not address the contested limitations (Answer at 31), but Table-1 specifically addresses the terminology addressed by the Examiner in the final Action and in this Answer (e.g., "simultaneous", "graphic", "spatial", "weight", and "video").

The Examiner takes the remarkable position that the facts provided by the Appellant are "not persuasive" to him (e.g., Answer at 31). However, this is an irrelevant issue because it is this Board that must be persuaded. Such self-serving, uninformative, and conclusory statements by the Examiner do not and cannot support the rejections. Conclusory statements that the Examiner is not persuaded are not informative to the Board or to the Appellant regarding the rejections.

The Examiner erroneously criticizes notes A-F in a vacuum (Answer at 31-32), but these notes must be taken in conjunction with Table-1. See the "NOTES" column in Table-1 (Appeal Brief at 25).

The Examiner's criticism of the notes to Table-1 (Answer at 31-32) are an example of where he disregards the substance of the arguments and the disclosure and instead criticizes the form of the arguments and the disclosure.

The Examiner erroneously criticizes Note-A and with it Note-B for not being relevant to the claim limitation and the disclosure (Answer at 31). However, many of the contested limitations are related to memory technology, accessing and writing, addressing, and blocks which are the terms in Table-1 that cite to Note-A (Appeal Brief at 25). Further, the contested limitation "spatial" is the term in Table-1 that cites to Note-B (Appeal Brief at 25).

The Examiner is preoccupied with quantity of disclosure rather than quality of disclosure and then he ignores the bulk of the relevant disclosure and the skill in the art (Appeal Brief at 8.2.3). For example, the Examiner criticizes the disclosure of an FFT in the Spec. at 33-34 as being insufficient (Answer at 31) and the Examiner ignores the detailed disclosure of a computer system, the related computer interface (Spec. at 87-89 and 95-98 and Figs. 6A-6B), and the very detailed disclosure of the kernel filter system[33] (Spec. at 15-24, 159-164, and 231-236 and Figs. 5A-5C, 6AG-6AH, and 7A) and the

---

[33] An FFT (a fast-Fourier transform) is a form of a filter system using a Fourier kernel.

Examiner ignores the very well known nature of an FFT and the extensive skill in the art related thereto.

The Examiner states that "Note D alleges that the broad disclosure of a graphics processor overcomes the various graphics rejections made" (Answer at 31) and that "Note F alleges that the broad disclosure of weighting in the specification and weighting and scaling in the program FTR.ASC overcomes the various weight rejections made" (Answer at 32). However, these are unfair and erroneous statements. The graphics processor and the weighting are disclosed in extensive detail in the form of a processor system coupled to an image memory and a display system and the detailed **programs** used to provide graphics capability (Spec. at 9-14 and 214-231) and weighting capability (Spec. at 15-24, 159-164, and 231-236 and Figs. 5A-5C, 6AG-6AH, and 7A). These disclosures range from system level block diagrams down to detailed schematic diagrams and **individual computer instructions**, with annotations for an actually reduced-to-practice system. The Examiner knows this but instead chooses to ignore this, recognizing that there is extensive detail regarding a **graphics program** and a **weighting program** in the disclosure. *See* Answer at page 32, line 1 and at page 32, line 10 for statements regarding these programs.

The Examiner states:

> This allegation [the graphics processor] is incorrect since the graphics processor described in the spec and in the program are not the same as the rejected graphics.

> This allegation [the weighting processor] is incorrect since the weight described in the specification and in the program are not the same as the rejected weight.

See Answer at 31-32, bridging sentence, and at 32 lines 9-11. However, **these are remarkable statements because they are totally false and totally unsupported**. There can be no doubt that it is the disclosed graphics processor and weighting processor that are claimed, not some other. This is the epitome of an improper rejection, refusing to consider the disclosure and then alleging no disclosure. However, the Examiner has a novel twist, admitting to the relevant disclosure before refusing to consider it. The Examiner admits to extensive graphics disclosure and weight disclosure in the application and then refuses to consider these disclosures. Actually, the graphics and weight limitations are disclosed in great detail and are claimed broadly—the epitome of sufficiency of disclosure.

Possibly, the Examiner's point is that there are two disclosures of weighting, a software (program) embodiment and a hardware (circuit) embodiment. However, they both represent relevant disclosures of kernel processors with weighting and must both be considered regarding § 112-1.

The Examiner again addresses the disclosure of an address generator for loading a weight table with weight values (Answer at 32). This issue involves the unbelievable § 112-1 rejection of adequately disclosed but unclaimed subject matter, which is addressed in detail in Section 2.1 herein.

The Examiner rejects Note-E because he alleges that the disclosure "according to the Microsoft Basic

Reference Book (exhibit 3) in section 1.7 is clearly rounding and not truncation." (Answer at 32). Notwithstanding the issue presented by the Examiner regarding the "%" instruction, the "FIX" instruction has no contention because Exhibit-4 to the Appeal Brief conclusively establishes that the "FIX" instruction truncates—**"FIX(X) returns the truncated integer part of X."** See the example in the Appeal Brief at Exhibit-4, Section 3.12, page 3-7 (emphasis added). Thus, it is not clear why the Examiner has not properly addressed this "FIX" instruction because it totally resolves the "truncation" issue and it is discussed in the subject Note-E.

Further, the example for "%" in said Exhibit-4 at Section 1.7, (page 1-8) is a form of truncation:

```
10 A% = 23.42
20 PRINT A%
RUN
 23
```

Converting 23.42 to 23 is an example of truncation.

The Examiner erroneously argues "product" terminology which is addressed in the Appeal Brief at Sections 8.1.6 and 8.1.7 and the Examiner totally disregards the statutory language, the law of the Federal Circuit, the guidelines of the PTO, and the disclosure in the instant application. See Answer at 32-33.

Further, the Examiner misstates that the '032 patent does not recite product claims when in fact it does. Claims 32, 34, 40, and 42 of the '032 patent expressly recite "making a product" terminology.

The Examiner takes a remarkable position—"[w]ithout adding more detailed limitations to the product claims . . . the rejection of the product claims is maintained." See Answer at 33. First, the Examiner has no authority to require the Appellant to add more limitations to any claim. Second, it is improper for the Examiner to withhold this suggestion until the Answer because the Appellant is not permitted to amend the claims in response thereto.

Notwithstanding the above, this statement on breadth is fatal to the § 112-1 rejection of the "product" claims because it reduces this § 112-1 rejection to one of breadth. However, breadth is an improper ground of rejection. It is black-letter law that an applicant can draft the claims as broadly as the prior art will allow. Further, these product claims are dependent claims, yet the parent claims from which they depend do not have a breadth rejection. Hence, the § 112-1 breadth rejection of the product claims is improper and should be reversed.

The Examiner attempts to make a "strawman" argument—that the circuitry is made in response to the process. See Answer at 33. However, a reference to § 271(g) will clarify that the product is made in response to the process. For example, performing of the process results in a product—a memory system. Alternatively, performing of the process results in information which constitutes a product.

The Examiner responds to Section 8.1.8 of the Appeal Brief with more improper conclusory statements alleging that the previous improper conclusory statements were proper. (Answer at 33). This is the epitome of circular reasoning.

The Examiner takes another remarkable position—that the commercial documents[34] describing how to make and use the commercial products disclosed in the specification are insufficient. See Answer at 34. The Examiner does not even state that he has reviewed these documents. However, these documents are significant, they disclose what to purchase, how to construct, how to program, and how to operate the commercial equipment used in the experimental system and much more.

The Examiner again makes unsupported conclusory statements about the skill in the art but he does not cite to any analysis of the skill in the art nor specifically state why the disclosure would not describe to or enable an artisan. For example, is it the Examiner's position that an artisan would not be able to wire up the disclosed schematics, or input the disclosed program, or turn on the power?

In view of the Examiner's disputed position, that the three disparate references that form the basis of the § 103 rejection could be combined to render obvious the claimed invention, why is a disclosure that presents the software, hardware, features, etc. together insufficient? The Examiner is playing "fast and loose" with the Board. See Appeal Brief at Section 8.10.

---

[34] These documents are cited to, are incorporated-by-reference into the instant application, and copies of which were provided to the PTO under the document disclosure program.

III. DOUBLE PATENTING REJECTIONS

3.1 The Controlling Law Establishes That The Provisional Double Patenting Rejections Must Be Reversed—Affirmance Is Legally Untenable

The Examiner clutters the record with provisional double patenting "rejections" that are really only objections (see, e.g., Wetterau[35]) and that the Board must reverse as a matter of law (see, e.g., Mott) where—"[a]n affirmance . . . is legally untenable."[36]

> We have trouble understanding the PTO's stated rationale for making the double patenting rejection final at this time. Once the provisional rejection has been made, there is nothing the examiner and the applicant must do until the other application issues. We see no undue burden here. There is no question, of course, that a double patenting rejection would be proper if one of appellant's applications issues. The effect of our reversal is merely to maintain co-pendency of these claims. An affirmance under the circumstances of this case would result in the automatic abandonment of these claims upon the receipt of our mandate by the PTO since appellant has refused to cancel the corresponding claims from the '840 application, and that result is legally untenable. The rejection of claims 39, 42, 44, 46, 50, and 57 for double patenting is reversed.

Mott[37] (emphasis added).

---

[35] In re Wetterau, 356 F.2d 556, 148 USPQ 499 (CCPA 1966).

[36] In re Mott, 539 F.2d 1291, 190 USPQ 536 (CCPA 1976).

[37] In re Mott, 539 F.2d at 1291, 190 USPQ at 541.

The only law cited by the MPEP on provisional double patenting (MPEP 804) is the CCPA controlling decisions in Mott and Wetterau. The Appellant knows of no other relevant cases and the Examiner has not cited any. It is particularly noteworthy that the CCPA reversed in Mott because such provisional objections [rejections] are not suitable for appeal. "**An affirmance . . . is legally untenable.**" It is also noteworthy that the CCPA decision in Wetterau is only provisional.

All CCPA cases, including Mott, were rendered in banc and later decisions therefore took precedence over earlier decisions. Later decisions sub silentio overruled any prior decisions to the extent that a prior decision was inconsistent with a later decision. As stated by the Federal Circuit:

> To the extent that [the later decision] language is inconsistent with that in [earlier decisions], that inconsistency has already been sub silentio removed. The CCPA's later decisions control because that court always sat en banc.

Gosteli[38] Hence, Mott is the controlling CCPA decision. Further, the CCPA decisions are precedent for the Federal Circuit.

It is also noteworthy that the MPEP guides the examiners to make such provisional rejections but does not inform the examiners or the public that such rejections are "legally untenable" and must be reversed according to Mott and constitute merely a notice if the copending application were to issue as a patent according to

---

[38] In re Gosteli, 872 F.2d 1008, 1011, 10 USPQ2d 1614, 1617 (Fed. Cir. 1989).

Wetterau. Proper guidance by the MPEP would have relieved the burden placed on the Board and on the Appellant in the present appeal.

The reason that these provisional objections [rejections] must be reversed is that the prohibition against double patenting is a prohibition against an extension of a patent term on an obvious variation of the same invention. As discussed below and notwithstanding the fact that there is no double patenting, unless or until there is an issued patent, there is no patent term to extend by issuing an application as a patent. If there are two pending applications with conflicting claims (which is not the case here), there is still no double patenting because there is no patent term to extend. Only after one of the applications issues as a patent can a double patenting rejection appropriate.

A provisional double patenting objection [rejection] constitutes merely a notice that a double patenting issue may exist when the subject copending application issues as a patent with conflicting claims. But such a notice is not a rejection. In order to save the Board and the Appellant unnecessary and, in this case, overly burdensome effort, the Examiner should have served notice with an objection under 37 CFR 1.78 rather than with a final provisional rejection.

The Board has more important responsibilities than to give notices on complex issues that are not ripe for Board adjudication and that most-likely will be resolved before it is ripe for Board adjudication. For example, the Federal Circuit is likely to dismiss such a provisional objection [rejection] on the ground that such an advisory opinion was not a case or controversy ripe for consideration by the court. Alternately, the court will reverse

since an affirmance of a provisional double patenting rejection is legally untenable. See Mott. Further, the PTO may obviate the instant provisional objections [rejections] by simultaneous issuance of the instant application and the copending applications, as requested in the Appeal Brief at Section 8.4.5 and as provided by the PTO in other cases discussed in this Section 3.1.

Thus, there is no purpose for the Board to spend its time to do the Examiner's job for him when the Examiner has not even attempted to establish a prima facie case of provisional double patenting, such as with claim comparisons, and when the results of the Board's efforts would merely be advisory.

As a still further example, the Examiner implicitly withdrew most of the provisional double patenting objections [rejections] in the Answer. The Appellant in the Appeal Brief drafted claim comparisons in the form of claim charts showing the errors in the provisional double patenting rejections and the Examiner implicitly agreed in the Answer that those charted-claims did not conflict. The Examiner then identified the subset of claims that he considered to be conflicting, five instant claims and 36 copending claims. This reduced the issues by more than ten-fold. The Appellant drafted additional claim charts (Exhibit-A attached hereto) showing the significant differences between the remaining instant claims and the copending claims. The next step would be for the Board to make the mandatory reversal of the provisionary rejections as required by Mott and, if the Board chooses to spend its time on this unnecessary advisory effort, to comment on the remaining five instant claims and 36 copending claims based upon the claim comparisons in the instant Brief.

The courts decision in Wetterau at 501 made abundantly clear the **provisional** nature of the rejection when it stated that '[i]f a patent were not to issue on the [] application, the "double patenting" rejection, if here affirmed, would of necessity evaporate for the possibility of two patents would not exist.'

Since the provisional double patenting rejection is over a copending **application**, actual double patenting is an impossibility unless or until a patent issues on the copending application. As the Federal Circuit has stated, the purpose of the rule against double patenting is to prevent an inventor from effectively extending the term of exclusivity by the subsequent patenting of variations that are not patentably distinct from the first patented invention. See Applied Materials and Van Ornum[39] which make it clear that, until a patent issues, there can be no double patenting. Said differently, there can be no substantive issue of double patenting mandating action on the part of the applicant (such as a terminal disclaimer) until such time as there is a patent issued. Then and only then is there a future interest, i.e., a fixed timewise monopoly that is subject to being improperly extended.

The Examiner should not have encumbered the record by carrying such notice-type rejections to appeal and briefing of an issue which may not ever arise. If and when one of the applications issues, the provisional dou-

---

[39] Applied Materials Inc. v. Advanced Semiconductor Materials America, 98 F.3d 1563, 40 USPQ2d 1481 (Fed. Cir. 1996). See also In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982) (The rule against double patenting prevents unjustified timewise extension of the right to exclude granted by a patent no matter how the extension is brought about.).

ble patenting rejection is converted to an actual double patenting rejection if still appropriate. The Board should not have to decide a provisional issue of double patenting and certainly the Federal Circuit should not have to decide such a provisional issue. This is especially so because a decision on such a provisional issue by either tribunal is merely advisory—it simply notifies the applicant that a possible double patenting rejection may be appropriate once the other application forming the basis of the rejection issues as a patent.

The CCPA and the Federal Circuit dismissed an issue under 37 CFR 1.175(a)(4) on the ground that an advisory opinion was not a case or controversy subject to consideration by the court. See Dien.[40] Similarly, the provisional double patenting rejections are advisory opinions or notices to the effect that at some point in time if and when a patent issues, an actual double patenting rejection may be appropriate. Also, it may well be that such a rejection is no longer appropriate once the patent issues. In that sense, a provisional rejection is merely a request for the Board and/or the Federal Circuit to render an advisory opinion. Such opinions burden the Board and the court. Thus, the rendering of a decision by the Board and/or the court on a provisional double patenting rejection would not appear to be a benefit and insofar as the court is concerned, would not appear to be a case or controversy appropriate for its consideration.

The Board is sufficiently burdened with its enormous workload that it should not be further burdened with

---

[40] In re Dien, 214 USPQ 10 (CCPA 1982); see also In re Keil, 1 USPQ2d 1427 (Fed. Cir. 1987).

rendering what is essentially a useless decision. A decision regarding a provisional rejection is an opinion of what could happen if certain events take place in the future. It is not and cannot be an actual rejection until one of the applications issues as a patent. The Board should dismiss these provisional rejections as not ripe for consideration. Although couched as rejections, they are more like objections to conflicting claims in copending applications. This is actually a 37 CFR 1.78 objection cloaked in the form of a provisional rejection. There cannot be a genuine issue of double patenting without an issued patent since there is no existing monopoly subject to extension. If the Appellant attempted to cloak an objection as a rejection and appeal it to the Board, the Board would decline to render a decision on the objection. Similarly, because the Examiner has cloaked a 37 CFR 1.78 objection as a provisional rejection, the Board should also decline to render a decision on this objection. When the instant application issues as a patent, the Examiner will be able to reject the claims of the copending application based upon an actual double patenting rejection and the Appellant will be able to pursue his remedies. This would minimize the burden on the Board, on the Appellant, and even on the Examiner.

As in Mott, the Board should reverse the provisional double patenting objections [rejections] because "[a]n affirmance . . . is legally untenable."

3.2 The Examiner Admits That Appellant's Claim Charts Are Persuasive

The Examiner implicitly agrees that the Appellant's claim charts[41] establish the absence of double patenting:

> Appellant also refers to Exhibit 2 in which appellant has chosen to compare **diverse claims** rather than comparing the most similar claims.

See Answer at 37 (emphasis added). Then the Examiner lists the five instant claims (claims 22, 23, 25, 84, and 100) that he now says exhibit provisional double patenting (Answer at 37-38). Notwithstanding the fact that the Examiner's newly-identified claims (instant claims 22, 23, 25, 84, and 100) do not show double patenting (Exhibit-A attached hereto), the double patenting rejections of all of the instant claims other than the Examiner's five newly-listed claims (instant claims 22, 23, 25, 84, and 100) should be reversed for the reasons shown in the Appellant's claim charts and because of the Examiner's acquiescence related thereto.[42]

The Examiner violates this law of the present case, that the claims do not stand or fall together[43] by identifying the five claims that he considers to exhibit provisional double patenting (Answer at 37-38) and then re-

---

[41] See Exhibit-2 to the Appeal Brief.

[42] Also, the double patenting rejections of the six newly-listed instant claims (instant claims 22, 23, 25, 84, and 100) over other than the Examiner's listed copending claims should be reversed for these same reasons.

[43] See Appeal Brief at Section VII and see the Answer at 3 which states "Appellant's brief includes a statement that the claims do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8)."

jecting **all** claims in this case for provisional double patenting thereover (Answer at 23-25). This violates the clear law of the Federal Circuit.[44]

3.3 The Examiner's Refusal To Address The Claim Differences Is Fatal To The Double Patenting Rejections

The Examiner refused to address the differences between the instant claims and in the copending claims. Hence, the provisional double patenting rejections must fall.

It is undisputed that there are differences between the instant claims and the copending claims. See Appeal Brief at Section 8.4.3. Even the Examiner admits to the presence of differences.

> Although the conflicting claims are not identical . . . . The minor **differences** between the claims in these nine applications are obvious variations of the same claimed invention.

See Answer at 23-24 (emphasis added).

The minor **differences** between the claims in these nine applications are obvious variations of the same claimed invention.

See Answer at 25 (emphasis added). But the Examiner has refused to provide the required Graham and Gechter analyses even when the Appellant pointed out these requirements (see, e.g., Appeal Brief at 70-71, Section 8.5). This is because these are significant differences and the required Graham and Gechter analyses would establish

---

[44] See Appeal Brief at Section VII entitled "GROUPING OF CLAIMS".

the non-obviousness thereof. See Exhibit-2 to the Appeal Brief and Exhibit-A herein. Even the Examiner implicitly admits to this fact.

> Appellant also refers to Exhibit 2 in which appellant has chosen to compare **diverse claims** rather than comparing the most similar claims.

See Answer at 37 (emphasis added).

Further, the Examiner now appears to be limiting the double patenting issues to only "some" of the claims (Answer at 41), but he still rejects **all** of the instant claims over **all** of the claims of the eight copending applications. The Examiner is erroneously rejecting the claims all-together in violation of his concurrence that the claims do not all stand or fall together (Section 1.2 herein). Further, the Examiner appears to be improperly leaving this task for the Board to do.

The CCPA in Wetterau[45] required that the claims in the copending application be analyzed for provisional double patenting:

> In the instant case, the approach we believe proper is to determine whether the differences between the inventions claimed in the application at bar and in the copending reference application are such that the subject matter sought to be patented would have been obvious to one of ordinary skill in the art . . . . If the issue as stated is answered in the negative, the appealed claims and the reference claims define patentably distinct subject matter and the "double patenting" rejection is unsound.

---

[45] In re Wetterau, 356 F.2d 556, 148 USPQ 499, 502 (CCPA 1966) (emphasis added).

However, in the instant case, the Examiner has neither determined the differences in the instant claims, nor determined the differences in the copending claims, nor analyzed the obviousness of these differences. Hence, the Examiner has failed to make the determination required by Wetterau and thus the provisional double patenting rejections should be reversed.

If the Examiner had determined and analyzed the differences between the instant claims and the copending claims, he would have found that the instant claims are not obvious over the copending claims. This is clear from the claim-charts in Exhibit-2 to the Appeal Brief. Now, in the Answer, the Examiner asks the Board to analyze the claims that he belatedly selected (Answer at 37-38) after complaining that he does not like the "diverse claims" selected by the Appellant (Answer at 37). However, the claims selected by the Examiner also have non-obvious differences, as shown in Exhibit-A attached hereto.

The many differences between the instant claims and the copending claims are illustrated in Exhibit-2 to the Appeal Brief. While the Examiner apparently concurs that these claims do not have double patenting,[46] admitting that these claims are "diverse" and thus do not conflict (Answer at 37), he now identifies five other claims which he now says conflict and he now asks the Board to do his work to analyze these claims. However, as with the claims analyzed in Exhibit-2 to the Appeal Brief, these five newly-identified claims do not conflict. See

---

[46] It is remarkable that the Examiner, after acknowledging that the claims in the claim charts (Appeal Brief at Exhibit-2) do not conflict refuses to withdraw the provisional double patenting rejections of these claims.

Exhibit-A attached hereto for additional claim charts showing the Examiner's errors with pairs of the claims that he now selects in the Answer. There are significant differences in each of the claims, as discussed below.

In a first example, instant claim 22 is directed to the processing of a frame of image information stored in "a two dimensional frame buffer" and having "a two dimensional array of . . . blocks of pixel image information" (a "macro array") while copending claim 43 is directed to the processing of a block of information stored in "a block memory" (a "micro array").

Instant claim 22 has further differences over copending claim 43 including "a two dimensional frame buffer storing a frame of . . . a two dimensional array of rows and columns of blocks of pixel image information", an address generator, and a two dimensional processor. These elements are not recited in copending claim 43.

Copending claim 43 has still further differences over instant claim 22 including an input weight circuit, a weight memory, a weight memory writing circuit, a weight memory accessing circuit, a scale factor memory, a scale factor memory accessing circuit, a weighting and scaling processor, and a display. These elements are not recited in instant claim 22.

In a second example, instant claim 100 is directed to the processing of "a two dimensional array of blocks of pixel image information" that is stored as "a two dimensional array of rows and columns of blocks" (a "macro array") while copending claim 45 is directed to the processing of "a block of image information" stored in "a block memory" (a "micro array").

Instant claim 100 has further differences over copending claim 45 including a two dimensional pixel block memory storing "a two dimensional array of blocks" (copending claim 45 has "a block memory") storing "a two dimensional array of rows and columns of blocks of pixel image information", address generating, and spatial processing. These elements are not recited in copending claim 45.

Copending claim 45 has still further differences over instant claim 100 including a data compressed image input circuit, a data decompressed image information output circuit, a block memory writing circuit, first and second clock circuits operating at different clock rates, an input weight circuit, a weight memory, a weight memory writing circuit, a weight memory accessing circuit, a scale factor memory, a scale factor memory accessing circuit, a weighting and scaling processor, and a display. These elements are not recited in instant claim 100.

Copending claim 45 is an apparatus claim and instant claim 100 is a process claim. Copending claim 45 has apparatus-type limitations not recited in process claim 100. For example, copending claim 45 recites the type of elements and the coupling between elements not recited in copending claim 45.

In a third example, instant claim 22 is directed to the processing of a frame of image information stored in "a two dimensional frame buffer" and having "a two dimensional array of . . . blocks of pixel image information" (a "macro array") while copending claim 96 is directed to the processing of a block of video image information stored in "a block memory" (a "micro array").

Instant claim 22 has further differences over copending claim 96 including "a two dimensional frame buffer storing a frame of . . . a two dimensional array of rows and columns of blocks of pixel image information" (copending claim 96 stores "a block of video image information" in "a block memory") and an address generator generating write addresses. These elements are not recited in copending claim 96.

Instant claim 22 is an apparatus claim and copending claim 96 is a process claim. Instant claim 22 has apparatus-type limitations not recited in process claim 96. For example, instant claim 22 recites the type of elements and the coupling between elements not recited in copending claim 96.

Copending claim 96 has still further differences over instant claim 22 including generating video information, generating data compressed video image information, generating data decompressed video image information, storing a block of video image information, storing a buffered block of video image information by a buffer memory, generating two dimensional spatially processed video image information, and displaying an image. These elements are not recited in instant claim 22.

In a fourth example, instant claim 22 is directed to the processing of a frame of image information stored in "a two dimensional frame buffer" and having "a two dimensional array of . . . blocks of pixel image information" (a "macro array") while copending claim 9 is directed to "a two dimensional pixel block memory (a "micro array").

Instant claim 22 has further differences over copending claim 9 including "a two dimensional frame buffer storing a frame of . . . a two dimensional array

of rows and columns of blocks of pixel image information" and frame buffer writing and accessing circuits. These elements are not recited in copending claim 9.

Copending claim 9 has still further differences over instant claim 22 including an input circuit operating at a first word rate and an output circuit operating at a second word rate, a scanning circuit, a vector generator, a two dimensional vector processor, and a two dimensional spatial processor. These elements are not recited in instant claim 22.

All of these representative differences, and further differences that are apparent between the two claims of each claim pair, should have been identified by the Examiner, but instead were ignored. Then the Examiner should have performed a Graham analysis and a Gechter analysis regarding the differences, but he did not. Hence, in addition to the fact that the provisional double patenting objections [rejections] are not suitable for Board adjudication (Section 3.1 herein), the provisional double patenting objections [rejections] are also fatally defective because of the significant differences between the instant claims and the copending claims and because of the refusal of the Examiner to perform the required analysis of the many claim differences.

If the Board does the Examiner's job for him, the Board will undoubtedly conclude first that any double patenting determinations between copending applications are merely notices and not sustainable rejections and second that there is no double patenting between the instant claims and the copending claims because of the significant non-obvious differences therebetween. Hence, the Board's effort would be for naught.

3.4 The Nonobviousness Double Patenting Rejections Are Fatally Defective

The Examiner recites the same conclusory Schneller cliches (see Answer at 25) that were criticized in the Appeal Brief (see Section 8.6.7) without providing reasons or facts to support the conclusory cliches. The Examiner also ignores MPEP 804 which requires claim comparisons in support of a Schneller-type double patenting rejection.[47] This failure to-support the rejection is a direct result of the inability to make the Schneller cliches fit the facts of the instant application. The PTO and particularly the Board recognizes the highly fact-specific nature of Schneller, and the Schneller facts do not fit the facts in the instant application. See Section 3.5 below. Hence, for this reason alone, the nonobviousness-type (Schneller-type) double patenting rejections must fall.

An important one of the Schneller cliches is that the instant claimed invention must be disclosed in the patent, otherwise it could not possibly have been properly claimed in the patent. As discussed in Section 1.4 herein, the Examiner stated that the instant claims were "fully disclosed" in the copending applications (see Appeal Brief at Section 8.1.2), which is a requirement to maintain a Schneller nonobviousness double patenting rejection (MPEP 804). However, the Examiner now changes his mind and states that his comment concerning "fully disclosed" means something else, (Answer at 49). Hence, because the Examiner has apparently with-

---

[47] The Examiner's listing of newly-identified claims (Answer at 37-38) for the Board to do the his analysis for him and the Examiner's failure to perform Graham and Gechter analyses violate this requirement.

drawn one of the basic requirements for a Schneller rejection (MPEP 804), the Schneller rejection must fall.

MPEP 804 requires claim comparisons between the instant claims and the copending claims in order to support Schneller-type double patenting rejections. No such comparisons have been made by the Examiner. In fact, the claim comparisons made by the Appellant were persuasive to the Examiner who implicitly withdrew most of the double patenting rejections in response thereto (Sections 3.2 herein). Although the Examiner provided a limited list of claims for the Board to compare (Answer at 37-38), it is not the Board's responsibility to do the required analyses for the Examiner. Further, the Appellant's claim comparisons (Exhibit-A attached hereto) show that there is no double patenting for the Examiner's newly-identified claims just as there is no double patenting for the claims analyzed in Exhibit-2 to the Appeal Brief. Yet further, the Examiner has never even attempted to reconcile the differences between these claims (Section 3.3 herein).

The names of the rejections alone illustrate the fallacy with the current provisional double patenting rejections. They are cast as "obviousness-type" and "nonobviousness- type" double patenting rejections" (Answer at 22-24) and as "the same obvious/nonobvious invention" (Answer at 40-41). Rejections for both obviousness and nonobviousness leave nothing for the Appellant to patent. The PTO cannot condone such a concept, and certainly the courts will not. Effectively, an allegation of obviousness-type double patenting overcomes an allegation of nonobviousness-type double patenting and similarly an allegation of nonobviousness-type double patenting overcomes an allegation of obviousness-type dou-

ble patenting. The Board must preserve the intellectual integrity of patent law, and the courts will certainly do so.

The Examiner confuses the double patenting issue with arguments about the issuance of a second patent extending the term of a first patent,[48] even though no first patent (in this context) has yet issued.

3.5 The Instant Schneller-Type Double Patenting Rejections Violate PTO Policy and Recent Board Decisions

The Appellant has been informed by PTO officials, subsequent to the filing of the Appeal Brief, that the current PTO policy regarding nonobviousness-type (Schneller-type) double patenting rejections is that such rejections should not be made unless the facts in the case are much the same as the facts in the Schneller decision. No per se rule for double patenting can or should be made based upon the facts in Schneller. See Appeal Brief at Sections 8.6.1 and 8.6.2 (the table of contents of which is excerpted below):

8.6.1 The Controlling Two-Part Test For Double Patenting Has Been Established By In Re Vogel 72

8.6.2 The Board Should Not Ignore In Re Vogel By Creating A Third Test For Double Patenting 75

This current PTO policy requires that Schneller-type-double patenting rejections be viewed as fact-specific rejections and do not have wide applicability. Hence,

---

[48] See Answer at 24-25.

Schneller is not relevant to the instant application. See Appeal Brief at Sections 8.6.3 to 8.6.6 (the table of contents of which is excerpted below):

8.6.3	The Present Claims Satisfy The Overruled Schneller Inquiries For Double Patenting	76
8.6.4	Schneller Only Applies Where The Patent Claims And The Application Claims Are Directed To The Same Preferred Embodiment	76
8.6.5	The Facts In The Instant Application Are Significantly Different From The Facts Of Schneller	78
8.6.5.1	Introduction	78
8.6.5.2	Schneller's Invention Is A Unitary Device, A Single Piece Of Wire Having Five Bends	80
8.6.5.3	The Present Case Has Ample Justification For Multiple Applications	81
8.6.5.4	The Claims In The Instant Application Are Not "Covered" By The Copending Application Claims	83
8.6.5.5	It Is Contrary To Schneller To Reject The Instant Claims Over Copending Applications	84
8.6.6	Schneller Is Distinguished Pursuant	

In view of the above, the Schneller-type double patenting rejections should be reversed.

The Appellant has been further informed by PTO officials, subsequent to the filing of the Appeal Brief, that certain recent decisions by the Board of Patent Appeals and Interferences relating to Schneller-type double patenting rejections support this policy change and that such cases will be published in the near future. The Appellant hereby requests leave to provide relevant comments on these cases when they are published. The timetable for publication of these cases is, according to PTO officials, indefinite but publication is certain.

3.6 The Examiner's Rebuttal To The Appeal Brief Establishes The Impropriety Of The Double Patenting Rejections

The Examiner's, rebuttal to the Appeal Brief establishes the impropriety of the double patenting rejections.

The Examiner discards the requirements of § 121 regarding other restriction requirements and ends up with an unsupported conclusory statement—"[c]urrently these applications are claiming the same invention in an obvious variation way." See Answer at 36-37. However, this statement does not satisfy § 121.

Further, how can claims that are admitted by the Examiner to be "diverse" (Answer at 37) be obvious variations of each other? See Appeal Brief at Exhibit-2 and Section 3.2 herein. Yet further, how can claims that

are rejected for nonobvious double patenting be obvious variations of each other?

The Examiner makes a devastating admission—"Appellant also refers to Exhibit 2 in which appellant has chosen to compare **diverse claims** rather than comparing the most similar claims. See Answer at 37.

The Examiner cites a subset of five newly-selected claims (Answer at 37-38), disregarding the fact that he has rejected **all** of the claims of the instant application over **all** of the claims of the eight copending applications. However, the Examiner's subset of claims are also **diverse**. See Exhibit-A attached hereto.

The Examiner expressly refuses to compare the claims, insisting instead that the Board compare the claims for him. See Answer at 38.

The Examiner makes the remarkable comment that simultaneous issuance "cannot be done since the applications are not allowed." (Answer at 39). However, the instant double patenting rejections are then also moot since the same patent applications are not allowed. In fact, provisional double patenting rejections are improper because there is no patent term to extend (Section 3.1 herein).

The Examiner is highly inconsistent, refusing to compare claims because they are alleged to have only "minor differences" (Answer at 39) while admitting to "diverse claims" when they are compared by the Appellant (Answer at 37 and Exhibit-2 to the Appeal Brief). Nevertheless, the Examiner has absolutely refused to compare the claims and to perform the required Graham and Gechter analysis, instead asking the Board and the Appellant to do his job for him.

The Examiner alleges to be following the current PTO policy, but in fact he is violating the current PTO policy (Section 3.5 herein).

The Examiner missed the point in Section 8.6.2 of the Appeal Brief (Answer at 39- 40). Vogel is the controlling law and Vogel establishes only two types of double patenting rejections, thereby prohibiting the third Schneller-type double patenting rejection.

The Examiner inconsistently states that the copending applications claim the same referred embodiment—a memory system storing, processing, and outputting—(Answer at 40) yet the Examiner has characterized the instant claims significantly differently—a vector system—(Answer at 4, Section 10.1). Clearly, the nine copending applications claim different embodiments that are admitted by the Examiner to be "diverse" from each other (Answer at 37). However, the Examiner keeps changing his story, once again alleging that the admitted "diverse" claims "**are so close that they cannot claim anything else but the same embodiment.**" See Answer at 41 (emphasis added). What an unbelievable statement. What happened to objectivity? What happened to Graham and Gechter? What happened to the admittedly "diverse" claims?

The Examiner makes a significant admission—"at least **some of the claims** in each of the applications claim the same obvious/nonobvious invention." See Answer at 41 (emphasis added). Who is to determine if there are "some" claims and if so which claims? Not the Examiner, he has finished his work. Not the Appellant, he has established the differences (Appeal Brief at Exhibit-2 and Reply Brief at Exhibit-A). The Examiner must be relying on the Board to do his job for him.

The Examiner admits to reviewing the claims in the nine copending applications (Answer at 41) but he does not share the results of this review with the Board or the Appellant. What kind of a review could this have been? Why has the Examiner withheld the results (e.g., the multitude of other "diverse" claims and any claims that might be obvious/nonobvious)?

The Examiner alleges a side-by-side comparison between claims shows that they claim the same invention (Answer at 42). However, where is this side-by-side comparison? Surely not Exhibit-2 of the Appeal Brief, the claims that the Examiner calls "diverse" (Answer at 37).

IV. ART REJECTIONS

4.1 The Examiner's Rebuttal To The Appeal Brief Establishes The Impropriety Of The Art Rejections

The Examiner erroneously alleges that Hill's "picture matrix memory" stores "a block of video data" (Answer at 26) in support of the art rejections. However, this is simply wrong. First, the instant claims do not recite just "a block of video data", but recite arrangements of blocks of data. For example, claim 22 recites "a two dimensional array of rows and columns of blocks of pixel image information". The details of these block-related recitations are discussed in Sections 4.2 and 4.3 below. Second, Hill discloses that "picture matrix memory" as follows.

> The picture matrix memory 80 is a 1024X3 bit dynamic shift register. . . .

> The picture matrix memory 80 stores the picture data in a recirculating sequence. The picture data requires 768 locations of memory.

However, the Examiner does not explain how this anticipates "a block of video data" as alleged by the Examiner nor how Hill anticipates the other limitations of the claims. Further, these are unsupported conclusory statements that do not establish that Hill is identical for the various claim limitations as required for a § 102 rejection.

The Examiner attempts to read claim 22 on Hill (Answer at 45-46), but Hill does not support the Examiner's reading. The Examiner made this up from the Appellant's disclosure through prohibited hindsight.

For example, the Examiner relies on Hill to teach "storing an array of blocks (164)" (Answer at 46) but Hill does not support this allegation. Hill does not teach that his picture matrix RAM 164 stores blocks. The Examiner made this up from the Appellant's disclosure through prohibited hindsight. Further, even the Examiner admits that Lord does not teach the claimed block limitations (Answer at 27). Hence, the block-related limitations alone are sufficient to distinguish the references.

The Examiner erroneously alleges that Hill's MPU "generates the video image information at a first word rate and the shift registers output the video information at a second word rate" (Answer at 26). However, this is an unsupported conclusory statement and it does not establish that Hill is identical for the various claim limitations as required for a § 102 rejection.

The Examiner denies that the authorities cited by the Appellant require and element by element comparison of the claims and he refused to provide this analysis (Answer at 43). However, the Examiner indicates that he did such an analysis and alleges that "[a] comparison of the claims with the prior art shows that all of the claimed elements are taught or suggested by the prior art." (Answer at 43). However, the Examiner fails to provide this "comparison of the claims with the prior art", necessitating the Board again perform such an analysis. However, the Appellant submits that the Board cannot duplicate such an analysis, even if the Examiner did perform one, because the references do not anticipate or render obvious the claims as established in Sections 4.2 and 4.3 below.

The Examiner refuses to comply with Richardson (Section 1.3 above and Answer at 44) and the Examiner relies on inherency in support of the § 102 rejections (Answer at 44) which is fatal to the § 102 rejections.

The Examiner throws around terminology as if it has little meaning. For example, the block architecture of the system is very important and it is not even indicated much less adequately taught by the references. Further, the references do not provide any motivation for the combination, only the Examiner's hindsight, as addressed in the Appeal Brief at Section 8.9.1. Further, the Examiner has not performed a Graham analysis, as addressed in the Appeal Brief at Section 8.9.2. Instead, the Examiner relies on unsupported conclusory statements, which violates the law of the Federal Circuit.

4.2 **Distinctions Of The Claims Rejected Under § 102 Over Hill**

The Examiner has never properly established why the rejected claims are alleged to be fully anticipated by Hill. The instant claims have non-identical differences with Hill. See Appeal Brief at Sections 8.7.1, 8.7.2, 8.8.1, and 8.8.2. For example, the instant claims have differences such as blocks of image information, different input and output clocks, and particular arrangements of addressing, writing, and accessing.

The claims rejected over Hill under § 102 have novel block storage and block processing distinctions thereover. For example, Hill does not teach the claimed block memory arrangement having an array of rows and columns of blocks of pixel image information. Excerpts from the independent claims rejected under § 102 over Hill are provided below with emphasis to illustrate the distinguishing block-related limitations.

Claim 22

> . . . a two dimensional frame buffer storing a frame of image information, the frame of image information arranged in a two dimensional array of rows and columns of blocks of pixel image information; . . .
>
> a frame buffer accessing circuit coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer accessing circuit accessing blocks of pixel image information in response to the read addresses generated by the address generator;

a two dimensional processor coupled to the frame buffer accessing circuit and generating two dimensional output processed image information in response to the blocks of pixel image information accessed by the frame buffer accessing circuit; . . .

Claim 23

. . . a two dimensional pixel block memory storing a two dimensional array of blocks of pixel image information, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information; . . .

a pixel block memory writing circuit coupled to the image input circuit, coupled to the two dimensional pixel block memory and coupled to the address generator, the pixel block memory writing circuit writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory in response to the input image information generated by the image input circuit and in response to the write addresses generated by the address generator;

a pixel block memory accessing circuit coupled to the two dimensional pixel block memory and coupled to the address generator, the pixel block memory accessing circuit accessing blocks of pixel image information in response to the read addresses generated by the address generator;

a two dimensional processor coupled to the pixel block memory accessing circuit and generating two dimensional output processed image information in

response to the blocks of pixel image information accessed by the pixel block memory accessing circuit; . . .

Claim 82

. . . storing a two dimensional array of blocks of pixel image information by a two dimensional pixel block memory, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information; . . .

writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory in response to the input image information and in response to the write addresses; . . .

accessing blocks of pixel image information from the two dimensional frame buffer in response to the read addresses, wherein the accessing of blocks of pixel image information from the two dimensional frame buffer is at a first information rate in response to the first clock signal; . . .

Claim 83

. . . storing a frame of image information by a two dimensional frame buffer, the frame of image information arranged in a two dimensional array of rows and columns of blocks of pixel image information; . . .

accessing blocks of pixel image information from the two dimensional frame buffer in response to the read addresses;

generating two dimensional processed image information in response to the accessed blocks of pixel image information; . . .

Claim 84

. . . storing a two dimensional array of blocks of pixel image information hy a two dimensional pixel block memory the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information; . . .

writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory in response to the input image information and in response to the write addresses;

accessing blocks of pixel image information from the two dimensional pixel block memory in response to the read addresses;

generating two dimensional processed image information in response to the accessed blocks of pixel image information; . . .

Claim 95

. . . storing a two dimensional array of blocks of pixel image information in a two dimensional pixel block image memory in response to the input image information, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information; . . .

accessing blocks of pixel image information from the two dimensional pixel block image memory, in response to the read addresses;

generating output image information in response to the accessed blocks of pixel image information; . . .

Claim 99

. . . storing a two dimensional array of blocks of pixel image information in a two dimensional pixel block memory in response to the input image information, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information; . . .

accessing blocks of pixel image information in response to the read addresses;

generating output processed image information in response to the accessed blocks of pixel image information;

The claims rejected over Hill under § 102 have novel addressing, writing, accessing, clocking, and output buffer limitations distinguishing over Hill. These limitations are particularly distinguishing when considered in the block storage and processing arrangement discussed above. Excerpts from the independent claims rejected under § 102 over Hill are provided below with emphasis to illustrate the distinguishing addressing, writing, accessing, and clocking limitations.

Claim 22

. . . an address generator generating write addresses and generating read addresses;

a frame buffer writing circuit coupled to the image input circuit, coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer writing circuit writing the frame of image information into the two dimensional frame buffer in response to the input image information generated by the image input circuit and in response to the write addresses generated by the address generator;

a frame buffer accessing circuit coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer accessing circuit accessing blocks of pixel image information in response to the read addresses generated by the address generator;

Claim 23

. . . an address generator generating write addresses and generating read addresses;

a pixel block memory writing circuit coupled to the image input circuit, coupled to the two dimensional pixel block memory and coupled to the address generator, the pixel block memory writing circuit writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory in response to the input image information generated by the image input circuit and in response to the write addresses generated by the address generator;

a pixel block memory accessing circuit coupled to the two dimensional pixel block memory and coupled to the address generator, the pixel block memory

accessing circuit accessing blocks of pixel image information in response to the read addresses generated by the address generator; . . .

Claim 82

. . . generating write addresses and generating read addresses;

writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory in response to the input image information and in response to the write addresses;

generating a first clock signal having a first clock rate;

accessing blocks of pixel image information from the two dimensional frame buffer in response to the read addresses, wherein the accessing of blocks of pixel image information from the two dimensional frame buffer is at a first information rate in response to the first clock signal; . . .

generating a second clock signal having a second clock rate that is different than the first clock rate of the first clock signal;

generating output image information in response to the two dimensional processed image information, wherein the generation of the output image information is at a different information rate than the first information rate in response to the second clock signal.

Claim 83

. . . generating write addresses and generating read addresses;

writing the frame of image information into the two dimensional frame buffer in response to the input image information and in response to the write addresses;

accessing blocks of pixel image information from the two dimensional frame buffer in response to the read addresses;

Claim 84

. . . generating write addresses and generating read addresses;

writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory in response to the input image information and in response to the write addresses;

accessing blocks of pixel image information from the two dimensional pixel block memory in response to the read addresses; . . .

Claim 95

. . . generating read addresses;

accessing blocks of pixel image information from the two dimensional pixel block image memory in response to the read addresses; . . .

storing buffered output image information by a buffer memory in response to the output image information.

Claim 99

. . . generating input image information at a first information rate; . . .

generating read addresses;

accessing blocks of pixel image information in response to the read addresses; . . .

outputting the output image information at a second information rate that is greater than the first information rate.

4.3 Distinctions Of The Claims Rejected Under § 103 Over Hill, Lord, And Lelke

The Examiner has never properly established why the rejected claims are alleged to be rendered obvious by Hill, Lord, and Lelke. These claims have non-obvious differences with these references and the references are improperly combined together. See Appeal Brief at Sections 8.7.2 and 8.9.3. For example, the instant claims have differences such as blocks of image information, different input and output clocks, and particular arrangements of addressing, writing, and accessing. Further, the references are disparate and cannot be combined together. See Appeal Brief at Sections 8.7.2 and 8.9.1.

Claims 19, 25, 96, 100, and 101 are limited to a spatial processing arrangement. The Examiner relies on Lord's element 21 as a spatial processor. However, Lord calls element 21 a "line interpolator" (see the Abstract) and the Examiner does not describe how he reads the instant spatial processor in a block arrangement on this

"line interpolator" nor how it can be combined with Hill and Lelke.

The claims rejected over Hill, Lord, and Lelke under § 103 have novel block storage and block processing distinctions thereover. For example, these references do not teach the claimed block memory arrangement having an array of rows and columns of blocks of pixel image information. Excerpts from the independent claims rejected under § 103 over these references are provided below with emphasis to illustrate the distinguishing block-related limitations.

Claim 19

. . . a two dimensional frame buffer storing a frame of image information, the frame of image information arranged in a two dimensional array of rows and columns of blocks of pixel image information; . . .

a frame buffer accessing circuit coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer accessing circuit accessing blocks of pixel image information in response to the read addresses generated by the address generator;

a two dimensional spatial processor coupled to the frame buffer accessing circuit and generating two dimensional spatially processed image information in response to the blocks of pixel image information accessed by the frame buffer accessing circuit; . . .

Claim 25

. . . a two dimensional pixel block memory storing a two dimensional array of blocks of pixel image information, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information; . . .

a pixel block memory writing circuit coupled to the image input circuit, coupled to the two dimensional pixel block memory and coupled to the address generator, the pixel block memory writing circuit writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory in response to the input image information generated by the image input circuit and in response to the write addresses generated by the address generator; . . .

a pixel block memory accessing circuit coupled to the two dimensional pixel block memory, coupled to the first clock circuit and coupled to the address generator, the pixel block memory accessing circuit accessing blocks of pixel image information in response to the read addresses generated by the address generator, wherein the accessing of blocks of pixel image information from the two dimensional pixel block memory by the pixel block memory accessing circuit is at a first information rate in response to the first clock signal;

a two dimensional spatial processor coupled to the pixel block memory accessing circuit and generating two dimensional spatially processed image information in response to the blocks of pixel image informa-

tion accessed by the pixel block memory accessing circuit; . . .

Claim 96

. . . storing a two dimensional array of blocks of pixel image information in a two dimensional pixel block image memory in response to the input image information, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information; . . .

accessing blocks of pixel image information from the two dimensional pixel block image memory in response to the read addresses;

generating two dimensional spatially processed image information in response to the accessed blocks of pixel image information; . . .

Claim 100

. . . storing a two dimensional array of blocks of pixel image information in a two dimensional pixel block memory in response to the input image information, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information; . . .

accessing blocks of pixel image information in response to the read addresses;

generating two dimensional spatially processed image information in response to the accessed blocks of pixel image information; . . .

Claim 101

. . . storing a two dimensional array of blocks of pixel image information in a two dimensional pixel block memory in response to the input image information, the two dimensional array of blocks of pixel image information arranged in a two dimensional array of rows and columns of blocks of pixel image information; . . .

generating two dimensional spatially processed image information in response to the accessed blocks of pixel image information; . . .

The claims rejected over Hill, Lord, and Lelke under § 103 have novel addressing, writing, accessing, clocking, and output buffer limitations distinguishing over these references. These limitations are particularly distinguishing when considered in the block storage and processing arrangement discussed above. Excerpts from the independent claims rejected under § 103 are provided below with emphasis to illustrate the distinguishing addressing, writing, accessing, and clocking limitations.

Claim 19

. . . an address generator generating write addresses and generating read addresses;

a frame buffer writing circuit coupled to the image input circuit, coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer writing circuit writing the frame of image information into the two dimensional frame buffer in response to the input image information generated by the image input circuit and in response

to the write addresses generated the address generator;

a frame buffer accessing circuit coupled to the two dimensional frame buffer and coupled to the address generator, the frame buffer accessing circuit accessing blocks of pixel image information in response to the read addresses generated by the address generator; . . .

Claim 25

. . . an address generator generating write addresses and generating read addresses;

a pixel block memory writing circuit coupled to the image input circuit, coupled to the two dimensional pixel block memory and coupled to the address generator, the pixel block memory writing circuit writing the two dimensional array of blocks of pixel image information into the two dimensional pixel block memory in response to the input image information generated by the image input circuit and in response to the write addresses generated by the address generator;

a first clock circuit generating a first clock signal having a first clock rate;

a pixel block memory accessing circuit coupled to the two dimensional pixel block memory, coupled to the first clock circuit and coupled to the address generator, the pixel block memory accessing circuit accessing blocks of pixel image information in response to the read addresses generated by the address generator, wherein the accessing of blocks of pixel image information from the two dimensional pixel block

memory by the pixel block memory accessing circuit is at a first information rate in response to the first clock signal; . . .

a second clock circuit generating a second clock signal having a second clock rate that is different than the first rate of the first clock signal;

an output circuit coupled to the two dimensional spatial processor and coupled to the second clock circuit, the output circuit generating output image information in response to the two dimensional spatially processed image information generated by the two dimensional spatial processor, wherein the generation of the output image information by the output circuit is at a different information rate than the first information rate in response to the second clock signal.

Claim 96

. . . generating read addresses;

accessing blocks of pixel image information from the two dimensional pixel block image memory in response to the read addresses; . . .

storing buffered two dimensional spatially processed image information in a buffer memory in response to the two dimensional spatially processed image information.

Claim 100

. . . generating input image information at a first information rate; . . .

generating read addresses;

accessing blocks of pixel image information in response to the read addresses; . . .

outputting the output image information at a second information rate that is greater than the first information rate.

Claim 101

. . . generating input image information at a first information rate; . . .

outputting the output image information at a second information rate that is greater than the first information rate.

V. ORAL HEARING

The Appellant requested an ORAL HEARING in accordance with 37 CFR 1.192 and 37 CFR 1.194 with the Appeal Brief filed on September 2, 1998.

The Appellant respectfully requests extra time for the hearing because of the number and complexity of the issues in this appeal.

VI. CONCLUSION

The Appellant has established that the disclosure is adequate and meets the requirements of 35 USC 112-1. The Appellant has further established that the rejections under 35 USC 112-1 do not establish a prima facie case, violate the law of the Federal Circuit, and are based upon erroneous and unsupported allegations. For

each of these reasons, the Appellant respectfully requests that the 35 USC 112-1 rejections be reversed.

The Appellant has established that the claims of the instant application patentably distinguish over and are independent or distinct relative to the claims of the eight copending applications. The Appellant has further established that the double patenting rejections do not establish a prima facie case, violate the law of the Federal Circuit, and are based upon erroneous and unsupported allegations. For each of these reasons, the Appellant respectfully requests that the double patenting rejections be reversed.

The Appellant has established that the claims of the instant application patentably distinguish over the prior art references. The Appellant has further established that the art rejections do not establish a prima facie case and violate the law of the Federal Circuit. For each of these reasons, the Appellant respectfully requests that the art rejections be reversed.

Because the Examiner has failed to, and in fact cannot,[49] establish a prima facie case, the Appellant is entitled to a patent.[50]

---

[49] The Examiner cannot establish a prima facie case because the claims find ample antecedent basis in the disclosure, there is no double patenting, and the prior art references do not anticipate the claims nor render the claims obvious.

[50] In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992).

CERTIFICATE OF MAILING BY EXPRESS MAIL: I hereby certify that this correspondence is being deposited with the United States Postal Service with Express Mail post office to addressee service under 37 CFR 1.10, postage prepaid, in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231 with the express mail label number EL112070942 on July 31, 2000.

Respectfully submitted,

Date: July 31, 2000 /s/ GILBERT P. HYATT
GILBERT P. HYATT
Registration No. 27,647
[address and phone number omitted]

UNITED STATES PATENT AND
TRADEMARK OFFICE BEFORE THE BOARD OF
PATENT APPEALS AND INTERFERENCES

Docket No. 516
Serial No. 08/471,702
Group Art Unit: 2672
Examiner: Jeffery Brier

IN RE APPLICATION OF GILBERT P. HYATT

Filed: June 6, 1995
[Received: Dec. 6, 2005]

REQUEST FOR REHEARING

For: A DATA COMPRESSION SYSTEM

Hon. Commissioner For Patents
and Trademarks
Washington, D.C. 20231

ATTENTION: Board of Patent Appeals and
Interferences

May It Please The Honorable Board:

This is a Request for Rehearing from the Decision of the Board affirming the rejections of certain claims on

appeal under 35 USC 112-1 for lack of written description and for lack of enablement.[1] This Request for Rehearing involves points of law and fact which the Appellant believes were misapprehended or overlooked in rendering the decision.

The following Table of Contents is the equivalent of an Executive Summary of the issues treated in this Request For Rehearing.

[1] The 35 USC 112-1 rejection for lack of enablement was held by the Board to stand or fall with the USC 112-1 rejection for lack of written description. In reliance thereon, the Appellant did not further address this enablement rejection herein.

TABLE OF CONTENTS

AND EXECUTIVE SUMMARY

Page

I. IMPORTANT INTRODUCTORY COMMENTS 1

1.1 THE APPELLANT APPRECIATES THE SIGNIFICANT EFFORT THAT THE BOARD EXPENDED TO ANALYZE THE DISCLOSURE 1

1.2 THE REJECTION OF OTHER CLAIMS SHOULD BE REVERSED BASED UPON UNCLAIMED SUBJECT MATTER 1

II. SHORT RESPONSE 2

2.1 IT IS UNDISPUTED THAT THE INDIVIDUAL CLAIM ELEMENTS BY THEMSELVES SATISFY § 112-1—THE PRIMARY ISSUE IS WHETHER THE FILTER PROCESSOR AND VECTOR PROCESSOR FUNCTIONS ARE PERFORMED AFTER ACCESSING IMAGE MEMORY 2

2.2 MOST OF THE REJECTIONS MUST FALL BECAUSE THE FILTER PROCESSING AND VECTOR PROCESSING FUNCTIONS ARE EXPRESSLY DISCLOSED AS BEING PERFORMED AFTER ACCESSING IMAGE MEMORY 5

2.2.1 The Filter Processor Function Is Expressly Disclosed As Being Performed After Accessing Image Memory 5

2.2.2 The Filter Processor Rejections Must Fall Because The CCPA And The Federal Circuit Condone Substitution Of Functions .. 7

2.2.3 The Vector Processor Function Is Expressly Disclosed As Being Performed After Accessing Image Memory 9

2.4 SHORT RESPONSE REGARDING DISCLOSURE OF QUANTIZATION WEIGHTING 11

2.5 SHORT RESPONSE REGARDING THE CONFORMANCE OF "MAKING A PRODUCT" CLAIMS TO 35 USC 271(G) 13

III. MORE DETAILED RESPONSE 14

3.1 MORE DETAILED RESPONSE REGARDING THE FTR.ASC FILTER PROCESSOR BEING IMPLEMENTED AFTER ACCESSING IMAGE MEMORY 14

3.2 MORE DETAILED RESPONSE REGARDING DISCLOSURE OF FREQUENCY DOMAIN AND DATA COMPRESSED INFORMATION TO BLOCKS OF INFORMATION 18

3.3 MORE DETAILED RESPONSE REGARDING BLOCK BOUNDARY SMOOTHING . 19

3.4 MORE DETAILED RESPONSE REGARDING DISCLOSURE OF RESPONSIVENESS TO PIXEL INFORMATION AND VECTOR INFORMATION 21

3.8 MORE DETAILED RESPONSE REGARDING THE CONFORMANCE OF "MAKING A PRODUCT" CLAIMS TO 35 USC 271(G) 27

IV. MUCH MORE DETAILED RESPONSE 29

4.1 MUCH MORE DETAILED RESPONSE REGARDING THE FTR.ASC FILTER PROCESSOR BEING IMPLEMENTED **AFTER** ACCESSING IMAGE MEMORY 31

4.2 MUCH MORE DETAILED RESPONSE REGARDING DISCLOSURE OF RESPONSIVENESS TO PIXEL INFORMATION AND VECTOR INFORMATION 31

4.3 MORE DETAILED RESPONSE REGARDING THE CONFORMANCE OF "MAKING A PRODUCT" CLAIMS TO 35 USC 271(G) 35

V. DISCUSSION OF THE STATEMENTS IN THE DECISION 40

5.1 THE BOARD'S COMMENTS ON TABLE-1 IN THE APPEAL BRIEF 40

5.2 THE EXAMINER AND THE BOARD DISREGARDED THE FACT THAT THE DISCLOSURE IS, IN LARGE PART, DIRECTED TO AN ACTUALLY REDUCED-TO-PRACTICE "EXPERIMENTAL SYSTEM" 41

5.3 AN ARTISAN WOULD EXPECT A COMPUTER SYSTEM TO BE DOCUMENTED IN THE FUNCTIONAL FORMAT OF THE INSTANT DISCLOSURE AND THE CCPA CONDONES SUCH A DISCLOSURE 43

VI. THE LAW OF WRITTEN DESCRIPTION .. 46

6.1 THE CCPA IN BANC DECISION IN ANGSTAD THAT WRITTEN DESCRIPTION IS "RELATIVELY SIMPLE TO COMPLY WITH" SHOULD BE DISPOSITIVE OF THE WRITTEN DESCRIPTION REJECTION 46

6.2 THE ISSUES IN EX PARTE RICHARDS COMPEL A SIMILAR REVERSAL OF THE § 112-1 REJECTION BASED UPON DISCLOSURE OF "INTERCONNECTIONS" AND FAILURE OF THE EXAMINER TO ESTABLISH A PRIMA FACIE CASE 47

EXHIBIT-5

COLOR PHOTOGRAPHS SHOWING OVERLAID VECTORS AND IMAGES ON A COLORED BACKGROUND

EXHIBIT-6

DISCLOSURE DOCUMENT RETENTION LABELS

EXHIBIT-7

USER MANUAL, VIEWPOINT/3A PLUS OPERATOR MANUAL

EXHIBIT-8

EMULATION REFERENCES

EXHIBIT-9

EXCERPTS FROM THE REPLY BRIEF DATED MARCH 28, 2002 IN COPENDING APPLICATION SERIAL NO. 08/433,786

IV. § 112-1 REJECTION 9-1

4.3 The Description More Than Meets The Law On Written Description 9-1

4.4 The Federal Circuit Analyzes Written Description On An Individual Limitation-By-Limitation Basis In Simple Tabular Form 9-10

4.12 The Fact That The Appellant Reduced-To-Practice An "Experimental System" Is Very Significant to § 112-1 9-12

4.15 The Skill In The Computer Art 9-13

4.15.1 The Electronics And Programming Arts Are Very Predictable 9-13

4.15.2 Routine Software Development 9-15

4.15.3 The Federal Circuit Held That Software Does Not Have To Be Disclosed If It Is Apparent Or Implicit In The Disclosure .. 9-23

4.15.4 Routine Electronic Hardware Development 9-26

I. IMPORTANT INTRODUCTORY COMMENTS

1.1 THE APPELLANT APPRECIATES THE SIGNIFICANT EFFORT THAT THE BOARD EXPENDED TO ANALYZE THE DISCLOSURE

The Appellant appreciates the significant effort that the Board expended to analyze the disclosure.

The discussions herein provide guidance to the Board as to where in the disclosure the features questioned by the Board can be found.

1.2 THE REJECTION OF OTHER CLAIMS SHOULD BE REVERSED BASED UPON UNCLAIMED SUBJECT MATTER

The Board reversed most of the rejections that were based upon unclaimed subject matter (e.g., Decision at 13, 21-22, and 32-33). However, claims 85 and 157 still stand rejected based upon unclaimed subject matter.

Claims 85 and 157 stand rejected regarding data compression (Decision at 27-28, Section 5) even though the claims do not recite data compression. Thus, the Section 5 rejection thereof should be reversed.

II. SHORT RESPONSE

2.1 IT IS UNDISPUTED THAT THE INDIVIDUAL CLAIM ELEMENTS BY THEMSELVES SATISFY § 112-1—THE PRIMARY ISSUE IS WHETHER THE FILTER PROCESSOR AND VECTOR PROCESSOR FUNCTIONS ARE PERFORMED AFTER ACCESSING IMAGE MEMORY

The Board recognizes that all but two ("frequency domain" and "quantization") of the individual claimed elements or functions by themselves are literally disclosed. See the Board's discussions regarding Table-1 (Appeal Brief at 25).[2]

The Board recognizes that claimed elements or functions relating to "frequency domain" and "quantization" are adequately disclosed even though these limitations are not literally disclosed (Decision at 30-31 and 37, respectively):

> We agree that one of ordinary skill in the art would recognize an FFT as a two dimensional frequency domain transform, so an FFT processor would generate frequency domain image information.
>
> We agree that changing floating point numbers to integers in the three ways described in Exhibit 4 to the brief constitutes "quantization."

The written description issue is whether two functions (LD.ASC-type vector processing and FTR.ASC-

---

[2] See also the Board's other comments about Table-1 (Decision at 12-13, 14, 19-20, 25, 26-27, 28, 29-30, 32, 34, 35, 35-36, and 38-39).

type filter processing) are performed in response to accessing of the image memory. The Board has held that the FTR.ASC-type filter processing discloses both data compression and quantization. The issue of whether such functions are performed after accessing the image memory is based upon the claim limitation of operating in response to the accessed blocks of image information from the block image memory (e.g., Decision at 26, 27, 29, and 37; respectively (emphasis added)):

> The only compression mentioned in the specification is concerned with compression and decompression offline or online prior to loading into the image memory or in connection with an emulation program, not after it is stored in the **block image memory**.
>
> However, as discussed in the preceding section 4, we find no disclosure of a processor "generating data compressed video image information" o: data anytime **after** it is **stored in the block image memory**. Nor do we find any disclosure of compression of data taken from the buffer memory. The specification discloses compression and decompression of data prior to loading into the image memory (spec, at 23), but this does not teach compression elsewhere in the circuitry.
>
> As discussed in sections 4 and 5, there is no written description support for any data compression by a processor **after** information is **stored in the image memory**.
>
> The claim limitation is directed to quantization *after* the pixel image information is accessed (read) from

> the **block memory**. Thus, the program LD.ASC (spec. at 217- 230), which deals with loading a file to the image memory (spec. at 91), and the program FTR.ASC (spec. at 231-236), which deals with prefiltering the database image (spec. at 18-24), do not appear relevant to the quantization written description issue.

However, the disclosure expressly teaches that the LD.ASC-type vector generation and the FTR.ASC-type filter processing are performed **after** the image memory, in response to the accessed image information from the image memory as claimed (Sections 2.2.1, 2.2.3, III, and IV herein).

Despite the express disclosure of the FTR.ASC filter processor and the LD.ASC vector processor being located **after** the block image memory and operating in response to blocks of image information accessed from the block image memory (Sections 2.2, III, and IV herein), the law of the Federal Circuit is that disclosure of the claim elements alone is adequate to satisfy written description. See Union Oil[3] holding that a claim limitation found only in an original claim that was not even recited in the patent was sufficient to satisfy § 112-1 for that claim limitation and holding that a table of elements (such as Table-1 in the Appeal grief) is adequate to show written description. See also Angstadt[4] holding that the written description requirement is "relatively

---

[3] Union Oil Co. of California v. Atlantic Richfield, 208 F.3d 989, 54 USPQ2d 1227 (Fed. Cir. 2000).

[4] In re Angstadt and Griffin, 537 F.2d 498, 190 USPQ 214, 217 (CCPA 1976) (emphasis added).

simple to comply with" and Richards[5] (Richards at 3-4 (emphasis added)):

> From our review of the examiner['s] rejection, the examiner maintains that the programming and specific **interconnection** of the functional units "must" be disclosed in the specification. . . . **We disagree** with the examiner. The examiner provides no reasoned analysis of why these would be needed or required.

Although such details are not required according to Richards, the instant disclosure provides extensive details of the claimed interconnections (Sections 2.2, III, and IV herein).

Angstadt and Richards are discussed in more detail in Sections 6.1 and 6.2, respectively, herein and Union Oil is discussed in more detail in Exhibit-9 herein at Sections 4.3-4.4 therein.

2.2 MOST OF THE REJECTIONS MUST FALL BECAUSE THE FILTER PROCESSING AND VECTOR PROCESSING FUNCTIONS ARE EXPRESSLY DISCLOSED AS BEING PERFORMED AFTER ACCESSING IMAGE MEMORY

2.2.1 The Filter Processor Function Is Expressly Disclosed As Being Performed After Accessing Image Memory

---

[5] Ex parte Richards, Appeal No. 1999-1847 (Bd. Pat. App. & Int.) (unpublished opinion), *at* http://www.uspto.gov/web/offices/dcom/bpai/decisions/fd991847.pdf. See also U.S. Patent No. 6,382,101 (issued May 7, 2002 to Richards).

The FTR.ASC filter processor is disclosed as being implemented **after** the image memory and disclosed as operating in response to blocks of image information accessed from the image memory.

Fig. 5A (discussed below) shows the filter processor expressly disclosed as being coupled to the output of the image memory (which is a block memory). This filter processor is also expressly disclosed as being implemented with both the disclosed hardware-implemented filter processor and the disclosed software-implemented filter processor. This software filter processor is implemented in great detail with the disclosed computer program FTR.ASC and satisfies the claim limitations for data compression and for quantization.

Fig. 5A shows the output 520H from the block "image memory" 520B coupled to the sum-of-the-products (9-pixel kernel) filter processor 520J and 520F which in turn is coupled to the "DAC" (digital to analog converter) 520G and from there to the CRT display monitor (Spec. at 16, 18, and 23; respectively (emphasis added)):

> A spatial filter arrangement will now be discussed with reference to Figs 5A to 5C.
>
> Fig 5A shows an arrangement of a display system. Address generator 520A generates pixel addresses **to access** a plurality of pixels, such as a 9-pixel kernel 520H, **from image memory** 520B . . . .
>
> Product signals 520J are summed together with summer 520F to generated a weighted and mixed pixel

intensity, which is converted to analog signal form with DAC 520G to excite a CRT display.

A filter processor can be emulated **in software** to illustrate operation of **a hardware configuration**. One filter processor configuration is shown in the BASIC PROGRAM LISTING **FTR.ASC** provided herewith and is shown in flow diagram form in Fig 7A.

Image processing can be performed on digitized images stored in the database. A stored image can be loaded from the database **into image memory** for image processing online with a **hardware-implemented image processor**.

This is confirmed by the Board (Decision at 15-16 (emphasis added)):

> Spatial filtering, as illustrated in figure 5A, . . . the pixels are read out **from the image memory** 520B, each pixel intensity is multiplied by a weight . . . and the sum may be converted to analog form in digital to analog converter (DAC) 520G for display (spec. at 16-17).

The filter processor shown in Fig. 5A can be implemented with the disclosed software filter processor (LD.ASC) or with the disclosed hardware filter processor (Figs. 6AG-6AH)—all three disclose a 9-pixel kernel filter processor.

Moreover, the CCPA and the Federal Circuit establish that an artisan would recognize substitutions of alternative configurations even if the substitution was not

expressly disclosed as it is in this case (Section 2.2.2 herein).

As discussed above, the CCPA in Angstadt established that the written description requirement is "relatively simple to comply with" and the Federal Circuit in Union Oil established that a table of elements is adequate to show written description. This despite the extensive relevant disclosure in the instant application.

There should be no question that an artisan would have been convinced that, in 1984, the Appellant was in **possession** of the FTR.ASC filter processor operating in response to blocks of image information accessed from the image memory. The Federal Circuit requires no more than possession.

In view of the above, the rejection of claims 1-14, 110-114, 116, and 119-132 should be reversed.

2.2.2 The Filter Processor Rejections Must Fall Because The CCPA And The Federal Circuit Condone Substitution Of Functions

In the instant disclosure, there is an express teaching of alternative software and hardware filter processor alternatives. However, the Federal Circuit and the CCPA establish that this express teaching is not necessary, an artisan would not have to be told to select disclosed alternatives.

The CCPA in Byrne[6] established that disclosure of the functions that an artisan might reasonably combine **is sufficient** in the absence of an apparent reason "why a substitution . . . would not be operable":

---

[6] Byrne v. Trifillis, 442 F.2d 1390, 170 USPQ 32, 34 (CCPA 1971) (emphasis added).

Recalling appellants' explicit statement that the jet turbine of Figure 1 may be substituted for the rewind motor shown in Figure 2, it is apparent that the only material respect in which the embodiment of Figure 2 resulting from that modification fails to support count 4 is in the use of friction brakes instead of fluid brakes for the reel. The board found as a fact that appellants' "description does not *explicitly* state anywhere that the water brake of the embodiment shown in Figs. 12 and 13 may be substituted for the friction brakes * * * in the combinations as shown in any of the other figures of the drawing." (Emphasis ours). While such finding is undeniably correct, **we think the board's position puts entirely too restricted an interpretation on the language of the application**, and particularly on the aforementioned reference to figures 13 and 14 as illustrating an embodiment "in which we employ the principles of a water brake for the same purposes as set forth and described heretofore with respect to the embodiments of Figures 2 and 7." **No reason being apparent why a substitution of the water brake would not be operable, we think this statement constitutes a clear and unequivocal disclosure of that substitution to person of ordinary skill [1] in the art.** The issue is not, as might be inferred from the board's opinion, whether one following appellants' specification would necessarily "produce" or select the particular combination of the counts for his own use. **Rather, it is whether he would necessarily recognize that such a combination was *disclosed* as a construction which might be selected if desired.** The present application clearly discloses an alternative construction em-

> bodying the combination of count 4. Consequently, it supports that count and also the less limited combinations of counts 3 and 5.

The Board in Nelson followed the law articulated in Byrne:[7]

> Bowler argues . . . that there is no specific teaching in Nelson to modify Example 5 to obtain the compounds of the counts. Thus, Bowler urges that although Nelson discloses in the list of substituents the required meta substituents of the counts, Nelson also disclosed the ortho and para substituents, among others, and there is no indication of preference for the substituents of the counts and therefore there is no reason to single out the required meta substituents. **In our view, however, the issue is not** whether one following the Nelson disclosure would necessarily produce the compounds or prefer the particular disclosed substituents (m-chloro or m-trifluoromethyl) required to prepare the compounds of the counts; **rather, it is whether he would necessarily recognize that such a combination was disclosed as a construction which might be selected if desired.** *Byrne v. Trifillis*, 442 F.2d 1390, 170 USPQ 32, 34 (CCPA 1971). We believe that one following the Nelson disclosure would necessarily recognize that the compounds of the counts were disclosed as a combination that might be selected if desired, i.e., the message would be conveyed that Nelson invented the compounds of the counts.

---

[7] Nelson v. Bowler, 1 USPQ2d 2076 at 2079 (Bd. Pat. App. & Int. 1986) (emphasis added).

Even if there was not an express teaching in the instant disclosure, the Federal Circuit clearly established that the disclosed software and hardware filter processors can be "transformed" therebetween:

> "[it is a] fundamental and well understood tenet of the computing art [that] . . .' **[a]ny software process can be transformed into an equivalent hardware process, and any hardware process can be transformed into an equivalent software process**." *See* Ed Klingler, *Microprocessor Systems Design* 5 (1977). Dr. Rhyne stated that this "dualistic transformation," known as the "hardware/software" tradeoff, effectively means that the selection of a software pointer for a microprocessor versus a hardware switch to control a microprocessor-based system is, simply a matter of design choice. This record evidence shows, that one of skill in the art would recognize these alternative systems as interchangeable substitutes.

Overhead Door.[8]

In view of the above, the rejection of claims 1-14, 110-114, 116, and 119-132 should be reversed.

2.2.3 The Vector Processor Function Is Expressly Disclosed As Being Performed After Accessing Image Memory

The disclosure teaches overlaying a background image with graphic vectors in the image memory. The

---

[8] Overhead Door v. Chamberlain, 194 F.3d 1261, 52 USPQ2d 1321, 1326 (Fed. Cir. 1999) (emphasis added).

Board recognizes this fact but bases the affirmation of the rejection on the contention that the claim limitation requires overlaying after accessed blocks of information. However, this is what the disclosure expressly teaches (discussed below). Hence, the rejection of claims 1, 2, 5, 9, 10, 12, 17, 18, 20, 81, 85, 98, 110-114, 119, 120, 123, 127, 128, 130, 133, 134, 136, 153, 157, and 161 should be reversed.

Two different methods of reading the subject claim limitation on the disclosure will now be provided. A simpler method is that the image memory is a block memory storing blocks of image information and in addition stores vector information. Hence, there should be no question that the resultant image information is generated in response to (1) blocks of image information and (2) vector information both stored in the image memory and both accessed from the image memory. A more detailed method is discussed below.

In this embodiment, the vector generator can be read on the computer executing the LD.ASC program and loading the vector information into the address generators. The vector processor can be read on the accessing of blacks of image information from the image memory with the address generators re-addressing the image memory and then the the overlaying of the vectors onto the accessed blocks and writing the overlaid information into the image memory. Then, the overlaid information in image memory is output and displayed by the GRAPH.ASC software processor or alternatively is output and displayed through the filter processor (Fig. 5A).

The vectors are written into image memory in response to blocks of image information accessed from the image memory. The Board recognizes that the writing

cycle involves first addressing image memory with the readdressing part of the memory address and then scanning in or strobing in the vector. Upon readdressing, the address propagates through the memory chips (Mitsubishi SRAM chips, not the now-common DRAMs) and the readdressed block appears at the outputs of the 64 SRAM chips. Then a sequence of write strobes write a sequence of individual pixel bytes (representing a vector) into the SRAM chips, changing (or being overlayed upon) the accessed block. Hence, the sequence of readdressing and scan-in of a vector results in the sequence of accessing a block and modifying the accessed block.

The above discussion effectively implements the well known read-modify-write memory cycle. This also effectively implements a block-access function (read), a pixel-modify function, and a write function.

Thus, because the vector generation function first accesses a block of image information from image memory and then overlays the block with the vector, the image information written into the image memory is generated in response to both (1) accessed blocks of image information and (2) vector information.

See Section 3.4 for a more detailed discussion of the above discussion.

As discussed above, the CCPA in Angstadt established that the written description requirement is "relatively simple to comply with" and the Federal Circuit in Union Oil established that a table of elements is adequate to show written description. This despite the extensive relevant disclosure in the instant application.

There should be no question that an artisan would have been convinced that, in 1984, the Appellant was in

possession of the claimed processor operating in response to blocks of image information accessed from the image memory and in response to the vector information. The Federal Circuit requires no more than possession.

2.4 SHORT RESPONSE REGARDING DISCLOSURE OF QUANTIZATION WEIGHTING

The Board questions the written description of quantization weighting claim limitations (Decision at 35-37, Section 11). However, this claim limitation finds clear antecedent basis in the disclosure. The Board recognized that the disclosure teaches quantization (Decision at 37):

> We agree that changing floating point numbers to integers in the three ways described in Exhibit 4 to the brief constitutes "quantization."

The real issue is (Decision at 37):

> The claim limitation is directed to quantization after the pixel image information is accessed read) from the block memory. Thus, the program LD.ASC (spec. at 217-230), which deals with loading a file to the image memory (spec. at 91), and the program FTR.ASC (spec. at 231-236), which deals with prefiltering the database image (spec. at 18-24), do not appear relevant to the quantization written description issue.

However, the FTR.ASC filter program does quantize "after the pixel image information is accessed (read) from the block memory." It is undisputed that quanti-

zation is adequately described in the FTR.ASC filter program and that this program is described as being implemented after the image memory. See, e.g., Fig. 5A as discussed in Sections 2.2.1 and 2.2.2 above and in Sections 3.1 and 4.1 below.

The Board suggests that the GRAPH.ASC program may be suitable to show quantization but concludes that it is not suitable (Decision at 37):

> The program GRAPH.ASC (spec. at 214-216), which deals with refreshing a CRT monitor from memory (spec. at 91), could be relevant. However, the GRAPH.ASC apparently simply accesses (reads) pixel information out of memory (and it is very cryptic how it does that) and does not perform any frequency domain processing, does not control the weight memory accessing circuit, and does not perform any quantization weighting of weighted frequency domain information. Thus, we fail to see how the program GRAPH.ASC, or the other programs LD.ASC or FTR.ASC, provide written description support for the limitation at issue. This basis for the rejection of claim 116 is sustained.

However, the FTR.ASC and GRAPH.ASC programs are both suitable. The FTR.ASC program is suitable for the reasons discussed above and the GRAPH.ASC program is suitable for the reasons discussed below.

The above quoted issues will be taken in sequence.

The GRAPH.ASC program does not simply access (read) pixel information out of memory. First and foremost it is a computer program executed in a stored program computer. It performs the relatively complicated functions of calculating of row and pixel addresses to

generate a two field interlaced scan in response to field identification. It detects and synchronizes with the field sync pulses, and much more.

The GRAPH.ASC program does process frequency domain information in that it controls the output of the image memory and the Board has held that storing of frequency domain information in image memory is adequately disclosed.

The GRAPH.ASC program does operate in response to quantized weight information in that it controls the output of the image memory and the Board has held that storing of such weighted information in image memory is adequately disclosed.

In sum, to the extent that image memory stores a type of information, the computer executes the GRAPH.ASC program to access that type of information from image memory.

2.5 SHORT RESPONSE REGARDING THE CONFORMANCE OF "MAKING A PRODUCT" CLAIMS TO 35 USC 271(G)

The Board questions the written description of "making a product" claim limitations (claims 153-172) (Decision at 39-42, Section 13). However, this claim limitation represents the statutory mandate of 35 USC 271(g):

> a product which is made by a process

This statutory phrase establishes that every process claim has a product associated with it and that every process claim covers such a product without the process claim even reciting the product made by the process.

Thus, a product is implicit in every claimed process. Hence, the Appellant must certainly be able to make explicit that which is made implicit in the process claim by the statute. See also the discussions in Sections 3.8 and 4.3 below.

III. MORE DETAILED RESPONSE

3.1 MORE DETAILED RESPONSE REGARDING THE FTR.ASC FILTER PROCESSOR BEING IMPLEMENTED AFTER ACCESSING IMAGE MEMORY

The Board questions the written description of responsiveness of data compressed video information to blocks of information claim limitations (Decision at 26-27 and 38-39, Sections 4 and 12). However, these claim limitations find clear antecedent basis in the disclosure. In brief, the disclosure teaches data compression in conjunction with the FTR.ASC filtering program and Fig. 5A expressly teaches filter processing after the image memory in response to blocks of image information accessed from image memory (Section 2.2 herein).

The Board states in affirming the rejection (Decision at 26):

> While a processor is coupled to the accessing circuit comprising the block memory of figures 6E to 6N and the raster scan address generator of figures 6O and 6P, we find no disclosure of the processor "generating data compressed video image information," as claimed. The only compression mentioned in the specification is concerned with compression and decompression offline or online prior to loading into the image memory or in connection with an emu-

lation program, not after it is stored in the block image memory.

However, see Sections 2.1 and 2.3 above.

The reading of the FTR.ASC software-implemented filter processor on Fig. 5A (Section 2.2.1 herein) should be dispositive of the instant issue. However, if the Board needs more, a foundation for the discussion is laid below to further clarify the issue followed by a technical description. See also Section 4.1 herein.

The filter processor function is expressly disclosed as being performed after accessing image memory.

First, it is undisputed that the disclosure expressly teaches both a software-implemented filter processor (Fig. 7A) and a hardware-implemented filter processor (Figs. 6AG- 6AH).

Second, it is undisputed that the disclosure teaches a filter processor implemented after the image memory (Fig. 5A).

Third, it is undisputed that the software-implemented filter processor expressly teaches the subject data compression and quantization.

Fourth, the instant disclosure expressly teaches emulating the hardware-implemented filter processor with the software-implemented filter processor.

Fifth, the CCPA and the Federal Circuit condone substituting of alternative features without an express disclosure thereof despite the fact that the instant disclosure expressly teaches emulating the

hardware-implemented filter processor with the software-implemented filter processor.

The FTR.ASC software-implemented filter processor is disclosed as operating both before and **after** accessing image memory. It is disclosed as operating before accessing image memory as a preprocessor (Spec. at 23) and it is disclosed as operating **after** accessing image memory in response to the image information accessed from image memory (Fig. 5A, this Section 2.2.1, and Sections 3.1 and 4.1 herein). Thus, the disclosure satisfies the written description requirement set forth by the Board for the rejections that are based upon filter processing after assessing of the image memory (Decision at 17, 17-18, 26, 27, and 37; respectively):

Both the CCPA and the Federal Circuit condone "substitution" (Section 2.2.2 herein) and the disclosure clearly teaches that the software filter processor FTR.ASC and the "hardware configuration" can be substituted there between—emulation is a type of substitution (Spec. at 18 (emphasis added)):

Description of Fig. 7A and the FTR-ASC Listing

> A **filter processor** can be **emulated** in **software** to illustrate operation of a **hardware** configuration. One filter processor configuration is shown in the BASIC PROGRAM LISTING FTR.ASC provided herewith and is shown in flow diagram form in Fig 7A.

The filter processor is disclosed as being implemented **after** the "image memory" (discussed above). See Fig. 5A where the input to the filter processor is the information accessed from the image memory. The Board asks

for no more for the filter processor claims (Decision at 26 and 37, respectively (emphasis added)):

> The only compression mentioned in the specification is concerned with compression and decompression offline or online prior to loading into the image memory or in connection with an emulation program, not after it is stored in the **block image memory**.
>
> The claim limitation is directed to quantization after the pixel image information is accessed (read) from the **block memory**. Thus, the program LD.ASC (spec. at 217 230), which deals with loading a file to the image memory (spec. at 91), and the program FTR.ASC (spec. at 231-236), which deals with prefiltering the database image (spec. at 18-24), do not appear relevant to the quantization written description issue.

In view of the above, an artisan would have been convinced that, in 1984, the Appellant was in **possession** of both the software-implemented filter processor LD.ASC and the hardware-implemented filter processor each operating in response to the image information accessed from the image memory (Fig. 5A).

Even without this express teaching in the disclosure, an artisan would recognize that the teachings of the software filter processor and the hardware filter processor were interchangeable. For example, both configurations filter a frame of image information with a 9-pixel kernel arrangement using a kernel weight arrangement.

The CCPA in Honn[9] stated:

---

[9] In re Honn, 364 F.2d 454, 150 USPQ 652, 657 (CCPA 1966) (emphasis added).

> It is well settled that an applicant need not expressly set forth in his specification that which would be understood by persons skilled in the art. See In re Bosy, 53 CCPA 1231, 360 F.2d 972, 149 USPQ 789; In re Chilowsky, 43 CCPA 775, 229 F.2d 457, 108 USPQ 321, and cases cited therein.

Thus, the express teachings in the instant disclosure are not needed, an artisan would readily recognize that the features of the software-implemented filter processor LD.ASC are equally applicable to the hardware-implemented filter processor (Fig. 5A) and which are alternatively implemented **after** the block image memory.

The disclosure expressly teaches two uses for the software-implemented filter processor (FTR.ASC), a pre-processor[10] function and a post-processor function. The pre-processor function was recognized by the Board (e.g., Decision at 17), but the post-processor function (discussed above in Section 2.2 and 3.1 and discussed in more detail in Section 4.1 below) was overlooked by the Board. There should be no question that an artisan would understand from the disclosure that the software-implemented filter processor (FTR.ASC) can be used both as a pre-processor and as a post-processor and can be software-implemented or hardware-implemented in either location.

There should be no question that an artisan would have been convinced that, in 1984, the Appellant was in possession of the FTR.ASC filter processor operating in

---

[10] The disclosure recites "preprocessor" without a dash. However, a dash ("pre-processor") may be used herein for ease of distinguishing the terminology "pre-processor" from the terminology "post-processor".

response to blocks of image information accessed from the image memory. The Federal Circuit requires no more than possession.

3.2 MORE DETAILED RESPONSE REGARDING DISCLOSURE OF FREQUENCY DOMAIN AND DATA COMPRESSED INFORMATION IN RESPONSE TO BLOCKS OF INFORMATION

The Board questions the written description of "frequency domain transform processor generating data compressed video image information or generating frequency domain image information" claim limitations (Decision at 29-31, Section 6). However, these claim limitations find clear antecedent basis in the disclosure. In brief, the disclosure teaches a data compression processor and a frequency domain processor operating in response to blocks of image information accessed from image memory.

The Board affirmed the rejection regarding the disclosure of the data compression processor operating in response to blocks of image information accessed from image memory. This is confirmed by the Board (Decision at 29):

> Independent claims 6-9, 13, and 14 all contain the limitation of "generating data compressed video image information." As discussed in sections 4 and 5, there is no written description support for any data compression by a processor after information is stored in the image memory. This rejection is cumulative to the rejection of section 12 as to claims 6-9, 13, 14, 124-127, 131, and 132.

This is the same issue addressed in Sections 2.2 and 3.1 above and Section 4.1 below and the Appellant relies on the discussions therein. In effect, Fig. 5A and the discussions related thereto disclose the filter processor (which includes data compression processing (FTR.ASC)) operating in response to the output from image memory.

In contrast to the treatment of data compression responsiveness, the Board concurs that the disclosure adequately teaches a frequency domain processor operating in response to blocks of image information accessed from image memory and the Board reversed the rejection of the claims related thereto (Decision at 30-31).

3.3 MORE DETAILED RESPONSE REGARDING DISCLOSURE OF BLOCK BOUNDARY SMOOTHING

The Board questions the written description of the block boundary smoothing claim limitations (Decision at 33-34, Section 9):

> A "block" is disclosed to be an array of 64 pixels arranged in 8 rows and 8 columns having a single address (or "re-address") of 11 bits. Pixels are selected within this block by a "scanout" address comprising the 3 least significant bits of the X and Y address. A "block boundary" occurs going from one block (one 11-bit address) to another block (another 11-bit address) during "re-addressing." We find nothing in the specification that describes "smoothing" or "block boundary smoothing." While the word "smoothing" occurs in the program FTR2.ACS (spec.

at 232, program line 110), this refers to "SMOOTHING PRINTOUTS" without explanation. In any case, the program FTR2.ASC is for -prefiltering the database image by taking an image from a file in conventional computer memory, filtering the kernel of 9 pixels using one of three sets of weights (program lines 170-210), and storing the image back into a file: as we understand it, it does not use a memory having blocks or block boundaries and so is not relevant to the issue of block boundary smoothing.

However, these claim limitations find clear antecedent basis in the disclosure. In brief, the disclosure teaches a smoothing (filtering) program (Spec. at 231-236) that expressly smooths across boundaries.

The FTR.ASC program is expressly stated as performing smoothing (Spec. at 232 (emphasis added)):

```
10  LPRINT "FTR2.ASC" '8/15/84 REV.8/22/4
      09:30"
20  'PREFILTER THE DATABASE IMAGE
30    OPEN "R", #1, "PRESENT.BIN", 128
40        FIELD 1,128 AS IA$ . . .
100   F%=66   INPUT "NUMBER OF LINES TO
      BE FILTERED";F5%
110   ' INPUT "ENABLE SMOOTHING PRINT
            OUTS; 'Y' OR 'N'"; A15$
```

Also, an artisan would readily recognize that two of the three selectable filter kernels (selections 1 and 2) are low pass filter kernels that smooth image information (Spec. at 232):

```
170 ' PRINT " SELECT, " 1 ", " 2 ", " 3 ": PRINT
180 ' PRINT "          , "2 4 2", "4 6 4," "8 8 8"
190 ' PRINT            , "4 8 4", "6 8 6", "8 8 8"
200 ' PRINT            , "2 4 2"; "4 6 4", "8 8 8"
210  A1%=3  'PRINT: INPUT "SELECT
                  WEIGHTS '1', '2', OR '3'"; A1%
220    ON A1% GOTO 260, 290, 320
```

The image to be smoothed is segmented into eight stripes. Each stripe is smoothed with the selected smoothing kernel except for the boundary pixels. The boundary pixels are smoothed by overlapping the kernel over the two adjacent stripes, the present stripe and the prior stripe at the top stripe boundary and the present stripe and the next stripe at the bottom stripe boundary (Spec. at 24 and 233; respectively (emphasis added)):

> The image is divided into 8-subimages; where each subimage contains 64-lines in a stripe. The stripes are identified as stripe-0 to stripe-7. For example, the lake image has the topmost stripe stored as the LAKE50.BIN file, the next lower stripe stored as the LAKB51.BIN file, the other stripes stored in the ascending LAKE5n.BIN files and the lowest stripe stored in the LAKE57.BIN file. The filter program accesses each stripe in sequence, filters the stripe, buffers the stripe as the FILTERED.BIN file, and stores the stripe as the FLAKE5n.BIN file. The filtering operation accesses a kernel of pixels surrounding the center pixel and consequently **overlaps stripes for the first line and the last line in a stripe**. Therefore, filtering of each stripe is imple-

mented by accessing the particular stripe as the **PRESENT.BIN** file, accessing **the previous stripe** as the **PRIOR.BIN** file, and accessing **the subsequent stripe** as the **NEXT.BIN** file.

```
670  OPEN "R",#1, "PRESENT.BIN",128 'RE-
     OPEN PRESENT FILE IF ANOTHER
680  FIELD 1,128 AS IA$ ' FILE WAS USED
690  TOGL$="F"
700  GOTO 860
710  IF RC < 5 THEN 720 ELSE 790
720  'GET RECORD FROM PREVIOUS FILE
730  CLOSE #1
740  OPEN "R",#1,"PRIOR.BIN",128
750  FIELD 1,128 AS IA$
760  TOGL$ = "T"      'FILE MUST BE OPEN
                      FOR INNER LOOP
770  RC=252+RC        'SET RC TO LAST LINE
                      IN PRIOR FILE
780  GOTO 860         'GET RECORD FROM
                      FILE
790  'ELSE
800  'GET RECORD FROM NEXT FILE
810  CLOSE #1
820  OPEN "R",#1,"NEXT.BIN",128
830  FIELD 1,128 AS IA$
840  TOGL$ = "T" 'FILE MUST BE OPEN FOR
     INNER LOOP
```

```
850   RC=RC-260 'SET RC TO FIRST LINE IN
      NEXT ;FILE
860   GET #1,RC
```

3.4 MORE DETAILED RESPONSE REGARDING DISCLOSURE OF RESPONSIVENESS TO PIXEL INFORMATION AND VECTOR INFORMATION

The Board questions the written description of claim limitations that are responsive to pixel information and vector information (Decision at 23-25, 27-28, and 31-32, Sections 3, 5, and 7). However, these claim limitations find clear antecedent basis in the disclosure. In brief, the disclosure teaches loading pixel image information (e.g., a background) into the image memory and then overlaying graphic vector information onto the pixel image information in the image memory. Hence, the output of the image memory is in response to both pixel image information and graphic vector information.

A more detailed discussion of the embodiment addressed in Section 2.2.3 will now be provided.

The vectors are written into image memory in response to blocks of image information accessed from the image memory in the following manner. The writing cycle involves first addressing image memory with the readdressing part of the memory address and then scanning in or strobing in the vector (Decision at 21-22 and 33-34, respectively):

> Initially, it is noted that the term "accessing" is used in two different ways. One meaning is sending an address to the memory circuits to select a particular address within all 64 memory circuits arranged in

an 8x8 array on a board ("re-addressing") (see claim 110 which requires "simultaneously accessing the 64 pixels arranged as eight rows and eight columns of pixel information") or selecting a particular memory circuit within the 8x8 array on the selected board to read out the pixel data ("scanout") (see spec. at 47: "The access time from the address select is significantly greater than the access time from the chip select or the output enable select. Therefore, accessing with the chip select and output enable signals can proceed at a significantly faster rate than accessing with the address select."). That is, all 64 memory circuits may be accessed simultaneously by readdressing, as in claim 110, but only 1 of the 64 pixels is accessed to be read out sequentially by scanout (spec. at 49). However, the general meaning from the specification is "reading" from the memory, which includes sequential "re-addressing" and "scanout" steps. Although it would be better to use different words for different functions to prevent confusion, the terminology is consistent with the specification and the particular meaning is clear in context.

A "block" is disclosed to be an array of 64 pixel arranged in 8 rows and 8 columns having a single address (or "re-address") of 11 bits. Pixels are selected within this block by a "scanout" address comprising the 3 least significant bits of the X and Y address. A "block boundary" occurs going from one block (one 11-bit address) to another block. (another 11-bit address) during "readdressing."

Upon readdressing, the address propagates through the memory chips (Mitsubishi SRAM chips, not the now-common DRAMs) and the readdressed block appears at the outputs of the 64 SRAM chips (Spec. at 35, 37, 40, and 46-47; respectively):

> Memory architectural features pertaining to high speed scanout in conjunction with re-addressing can provide speed enhancement, such as a 3-fold improvement in speed. These feature are particularly pertinent to RAMs having multiple tristate control signals; such as the Mitsubishi Electric M58725P RAMs. RAMs having a single tristate control signal can also be used with this configuration . . . .
>
> Higher speed scanout can be used in conjunction with slower speed addressing of the RAMs to provide an average access rate that is significantly higher than the addressing rate. For example, the Mitsubishi Electric M58725P RAMs have a 200-ns address period and a 100-ns scanout period.

The Mitsubishi RAMs have 2K-words by 8-bits per word. Therefore, 128-RAMs are used to provide 262,144-pixels. For efficiency of implementation, the RAMs are arranged in two 2-dimensional boards each having a binary quantity. (i.e., 8) RAMs for each dimension. Consequently, the 128-RAMs are arranged on 2-boards each having 64-RAMs, arranged in an 8-by-8 block of RAMs per board.

Typical circuits are the TMS-4016 RAM from Texas Instruments Inc. and the M58725P static RAM from Mitsubishi Electric. These circuits are configured in

> the form of a 2K-word by 8-bit static RAM having an 11-bit address, a tristate chip select, and a tristate output enable. Conventionally, the chip select and output enable are used to provide output bussing and to reduce the need for an output register. In the present configuration, the chip select and output enable signals are used to provide 2-additional dimensions of memory addressing. For example, the 11-address lines are used to select a block of 64-pixels out of 262,144-pixels; the chip select signal is used to select a column of 8-pixels out of the selected block of 64-pixels; and the output enable signal is used to select a row of 8-pixels out of the selected block of 64-pixels. The selection of a column of 8-pixels and a row of 8-pixels with the chip select signal and the output enable signal selects a single pixel at the intersection of that column and row from the selected block of 64-pixels. Consequently, a 3-dimensional architecture having address selection of a 64-pixel block, chip selection of an 8-pixel column in that block, and output enable selection of an 8-pixel row in that block uniquely selects a single pixel out of 262,144-pixels.

Then a sequence of write strobes write a sequence of individual pixel bytes (representing a vector) into the SRAM chips, changing (or being overlayed upon) the accessed block (e.g.; Spec. at 88, 90, 101, and 174):

> Signal DOA5 controls loading in sequential and random access form. Sequential loading is selected when DOA5 is high and random access loading is selected when DOA5 is low. When DOA5 is high, an output strobe on DOA7 causes the pixel address registers to be updated with the related slope parame-

ters on the falling edge of the strobe. This insures compatibility with the DOA7 strobe used as a write-bar signal to write the previous pixel information into the previously addressed pixel in image memory.

Loading of image memory with the supervisory processor is performed with a 3-port output arrangement having 8-bits per port. The first port, Port-A, communicates control signals between the supervisory processor and the display processor. The second port, Port-B, communicates address and data information to be loaded into the display processor between the supervisory processor and the display processor. The third port, Port-C, selects the register or memory in the display processor for loading. The protocol involves outputting of the destination address on Port-C, outputting of information to be loaded into the display processor on Port-B, and then outputting of a data strobe on Port-A. The data strobe loads the output information into the selected destination.

Gate U22C-11 is an OR-gate that is enabled with the address of the memory U19B-11 to load data into the memory for steering of the computer strobe U22B-3 to generate a write strobe to load the computer generated parameter into memory.

SEQUENTIAL CONTROL OF IMAGE LOADING

(1) RESET DOA5
(2) LOAD X+Y START ADDRESSES, (PIXEL ADDRESS TIMES 8)

(3) LOAD SLOPES TIMES 256

(4) SET DOA5

(5) GENERATE A SEQUENCE OF STROBED DATA OUTPUTS ALONG LINE

(6) ADDRESS COUNTER WILL AUTOMATICALLY ADVANCE

(7) DOA5 must be set before strobing data into memory independent of whether one or a sequence of strobes is to be generated.

Hence, the sequence of readdressing and scan-in of a vector results in the sequence of accessing a block and modifying the accessed block.

Thus, because the vector generation function first accesses a block of image information from image memory and then overlays the block with the vector, the image information in the image memory is generated in response to both (1) accessed blocks of image information and (2) vector information.

In addition to the antecedent basis discussed in this Section 3.4 above, the disclosure has additional teachings regarding this vector and block information arrangement. It is important to note that the image memory is a block memory (as recognized by the Board in the Decision) and the image memory central to these display processing operations. Thus there should be no question that there is significant interaction between the generated vectors and the blocks accessed from the image memory.

The filter program FTR.ASC teaches accessing of the disk database information into the computer, image processing (e.g., filtering) of the disk database image information, and writing of the processed image information back into the disk database from the computer (Spec. at 18). The Image Load section (Spec. at 90) teaches this loading of image information into the image memory. The disclosure expressly teaches in detail the computer interface circuitry and software for this loading of the image information into image memory (e.g., Spec. at 88-90, 101, 104-06, 111-112, and 174). The graphic vector software LD.ASC (e.g, Spec. at 9-14 and 217-30) teaches the overlaying of graphic vectors onto this image information that was loaded into image memory. This is expressly taught as overlaying graphic vectors onto a "background" image in image memory (Spec. at 217-221):

```
120  PRINT "SELECT OVERLAY FOR LOAD-
     ING INTO IMAGE MEMORY ... 1"

                * * *

171  PRINT "SELECT OVERLAY FOR LOAD-
     ING INTO IMAGE MEMORY"

                * * *

632  'SUBROUTINE TO OVERLAY A RECTAN-
     GLE

                * * *

2020 RETURN          'RETURN TO OVERLAY
     MENU
```

The display refresh software GRAPH.ASC (Spec. at 214-216) displays the overlaid image by refreshing the

display device in response to the overlaid image stored in image memory.

The Appellant actually reduced-to-practice and disclosed in detail the "Experimental System" which included vector generation and overlaying in the LD.ASC computer program (Spec. at 10-11 and 86, respectively):

> An experimental system has been constructed to demonstrate operation of the graphics display capability. The arrangement shown in Fig 1 has been implemented in hardware for refreshing the display in real time. A program, such as the BASIC PROGRAM LISTING GRAPH.ASC, can be used to control that experimental hardware for refreshing the display. In this experimental system, the graphics vectors are loaded in an offline manner with the LD.ASC Basic program set forth in the BASIC PROGRAM LISTING LD.ASC herein; emulating hardware loading of graphics vectors in an online manner. In this experimental system, graphics operation is initiated each frame with supervisory processor 115A and hardware refresh is performed with address generators 115B and image memory 115C.
>
> Operation of hardware and software in the experimental system discussed herein in conjunction with a color monitor demonstrates operation of the system, meeting of system objectives, and providing actual reduction to practice. For example, information has been loaded into image memory and has been display processed and displayed to demonstrate operation.

The Appellant presented at oral argument color photocopies of overlaid images that were displayed with the disclosed actually reduced-to-practice "Experimental System". These photocopies were excerpted from video tapes filed with the PTO and retained by the PTO under the disclosure document program. See Exhibit-5 herein for color photocopies of the type that were presented at oral argument and see Exhibit-6 herein for the disclosure document retention labels. These photocopies show the graphic vectors and images overlayed together on a colored background with the LD.ASC program.

The disclosure of responsiveness to pixel information and vector information is discussed above and should be dispositive of this rejection. However, if the Board wants more, the disclosure of responsiveness to pixel information and vector information is discussed in greater detail in Section 4.2 below.

There should be no question that an artisan would have been convinced that, in 1984, the Appellant was in **possession** of the LD.ASC vector processor operating in response to blocks of image information accessed from the image memory and in response to the vector information. The Federal Circuit requires no more than possession.

3.4 MORE DETAILED RESPONSE REGARDING DISCLOSURE OF DATA COMPRESSED VIDEO INFORMATION IN RESPONSE TO VIDEO PIXEL INFORMATION AND VICTOR PROCESSED INFORMATION

The Board questions the written description of data compressed video information in response to video pixel information and vector processed information claim limi-

tations (Decision at 27-28, Sections 5 and 10). However, these claim limitations find clear antecedent basis in the disclosure. In brief, the disclosure teaches data compression in conjunction with the FTR.ASC filtering program which is a software implementation of the filtering arrangement shown in Fig. 5A (Sections 2.2.1, 3.1, and 4.1 herein). Moreover, the disclosure teaches the video information generated in response to video pixel information and vector processed information claim limitations (Sections 2.2.3, 3.4, and 4.2. herein).

3.8 MORE DETAILED RESPONSE REGARDING THE CONFORMANCE OF "MAKING A PRODUCT" CLAIMS TO 35 USC 271(G)

As discussed in Section 2.5 above, the Board questions the written description of "making a product" claim limitations (claims 153-172) (Decision at 39-42, Section 13). However, this claim limitation represents the statutory mandate of 35 USC 271(g):

> a product which is made by a process

This statutory phrase establishes that every process claim has a product associated with it and that every process claim covers such a product without the process claim even reciting the product made by the process. Thus, a product is implicit in every claimed process. Hence, the Appellant must certainly be able to make explicit that which is made implicit in the process claim by the statute. See also the discussion in Section 4.3 below.

It is not clear from the record if the rejection is based upon:

(a) a position that a product is not implicit in a process claim,

(b) a position that the Appellant cannot make explicit in a claim that which is made implicit by the statute,

(c) a position that a patent application disclosure does not represent a product (e.g., the disclosed actually reduced-to-practice "Experimental System" does not represent a product),

(d) a position that the wording of claims 153-172 does not reflect the statutory mandate, and/or

(e) some other position.

Hence, clarification of the Board's affirmation regarding the "making a product" claims is respectfully requested.

If the Board's position is (d) above (that the wording of claims 153-172 does not reflect the statutory mandate), then the Appellant respectfully requests guidance of the Board on the proper wording and the Appellant respectfully requests leave under 37 CFR 1.196(c) to implement the Board's guidance by amending claims 153-172 in conformance with the Board's guidance.

The Board's holdings regarding the "making a product" claims (Decision at 39-42) are further discussed in Section 4.3 herein.

IV. MUCH MORE DETAILED RESPONSE

4.1 MUCH MORE DETAILED RESPONSE REGARDING THE FTR.ASC FILTER PROCESSOR BEING IMPLEMENTED AFTER ACCESSING IMAGE MEMORY

The FTR.ASC filter processor is disclosed as being implemented **after** the image memory and as operating in response to blocks of image information accessed from the image memory (Sections 2.2 and 3.1 above).

The disclosed **emulation** teaches an artisan to use the software-implemented filter processor in substitution for the software-implemented filter processor (Section 2.2 herein).

The disclosure expressly teaches the software-implemented filter processor FTR.ASC as emulating the hardware-implemented filter processor (Spec. at 18 (emphasis added)):

> Description of Fig 7A and the FTR.ASC Listing
>
> A filter processor can be **emulated** in software to illustrate operation of a hardware configuration. One filter processor configuration is shown in the BASIC PROGRAM LISTING FTR.ASC provided herewith and is shown in flow diagram form in Fig 7A.

Software emulation of hardware is used elsewhere in the disclosure. The disclosure even teaches that the software graphics vector generator (included in the LD.ASC program) emulates a hardware implementation thereof (Spec. at 11 (emphasis added)):

> In a hardware configuration, graphics vector generation can be performed in real time using the **software emulated vector generation capability implemented in hardware form**.

Thus, an artisan would recognize that the Appellant was in **possession** of the disclosed software features as being emulations of hardware features.

The Board uses "emulator" and "emulation" terminology with approval (Decision at 17-18, 20, and 26, respectively).

> As in the disclosed actually reduced-to-practice "Experimental System", in the art of the time, emulation was used to "experiment on tradeoffs between software and hardware" which were known to be alternative or "substitute" implementations:[11]
>
> EMULATION
>
> * * *
>
> Lately there has been a great deal of interest in moving certain portions of software systems into microprogrammed control portion of the machine to effect increased speed. This has created the opportunity **to experiment on tradeoffs between software and hardware** and between software and microcode.

---

[11] ENCYCLOPEDIA OF COMPUTER SCIENCE AND ENGINEERING at 602-603, Van Nostrand Reinhold Company (1983) (emphasis added). See Exhibit-8 herein.

The meaning of emulation today is consistent with the meaning of emulation in the early 1980s:[12]

> Emulation
>
> > The process by which a device is built to work like another. . . . The emulator can be hardware, software or both.
>
> The VEEP [Visual Equipment Emulation Program] emulated equipment can be operated almost identically with the real equipment. . . .

4.2 MUCH MORE DETAILED REPONSE REGARDING DISCLOSURE OF RESPONSIVENESS TO PIXEL INFORMATION AND VECTOR INFORMATION

The disclosure of responsiveness to pixel information and vector information is discussed in Sections 2.2.3 and 3.4 above and is discussed in more detail below.

As discussed in Sections 2.2.3 and 3.4 above, the disclosed actually reduced-to-practice "Experimental System" discloses generating the processed image information in response to two types of information—the frame of pixel information loaded into the image memory by the processor and the vector information overlaid onto the frame of pixel information that is in the image memory. The Image Load section (Spec. at 90) loads the frame of pixel information into the image memory with the processor and the graphics vector generation software over-

---

[12] http://www.synopsys.com/news/pr_kit/eda_glossary.html (09/27/2002) and http://www.cemtekenglish/electronics.htm (09/27/2002); respectively. See Exhibit-8 herein.

lays the vector information onto the frame of pixel information in the image memory.

The Image Loading section teaches in detail the writing of a frame of image information from the computer into the image memory. It teaches the loading of image memory with image information accessed by the computer, such as for use as a background for overlaying of graphic vectors, and teaches the loading of graphic vectors (Spec. at 90 (bold emphasis added, underlining in original)):

Image Loading

Loading of an image into memory is performed by loading the XP and YP-address registers with the address of each pixel to be loaded, then outputting the pixel information to be loaded with Port-B, and then strobing the pixel information into image memory with the DOA7 signal. A sequential load feature is provided under control of the DOA5 signal. When the DOA5 signal is high, a vector can be loaded; where the previously loaded pixel address is incremented with the related delta parameter to obtain the next pixel address to reduce software overhead and thereby speedup loading of image memory.

Loading of image memory with the supervisory processor is performed with a 3-port output arrangement having 8-bits per port. The first port, Port-A, communicates control signals between the supervisory processor and the display processor. The second port, Port-B, communicates address and data information to be loaded into the display processor between the supervisory processor and the display processor. The

third port, Port-C, selects the register or memory in the display processor for loading. The protocol involves outputting of the destination address on Port-C, outputting of information to be loaded into the display processor on Port-B, and then outputting of a data strobe on Port-A. The data strobe loads the output information into the selected destination.

A program to load vectors into memory is provided herein as the BASIC PROGRAM LISTING LD.ASC and is briefly discussed in the section entitled Software herein.

Details of the hardware and software for loading the frame of image information from the computer into the image memory are further discussed in detail.

The overlaying of graphic vectors onto a background image, which background image may be loaded from the database by the computer (discussed above) or can be loaded by the computer executing the LD.ASC program (discussed below), is taught in detail (Spec. at 218-223 (emphasis added)):

```
114 PRINT " SELECT OPERATION"
116 PRINT "**********************": PRINT
118 PRINT "RETURN TO OPERATING
    SYSTEM ..............................  0"
120 PRINT "SELECT OVERLAY FOR
    LOADING INTO IMAGE MEMORY ..... 1"
122 PRINT "SELECT IMAGE TO BE
    LOADED INTO IMAGE MEMORY"
```

```
124 PRINT "     CONCENTRIC SQUARE
                FRAMES .... ..... 2"
126 PRINT "     RECTANGLES AND
                LINES ..... 3"
128 PRINT "     SPIRALS ..... 4"
130 PRINT "     VIEWPORT COORDINATE
                SYMBOLS ..... 5"
132 PRINT "     PATTERN #6 ..... 6"
134 PRINT "     PATTERN #7 ..... 7"
136 PRINT "     SQUARE PATTERN ..... 8"
138 PRINT "     SQUARE FRAMES ..... 9"
140 PRINT "     PERIPHERAL SQUARES 10"
141 PRINT "     PERIPHERAL
                TRIANGLES ..... 11"
142 PRINT "     HOUSE ..... 12"
151 INPUT "     SELECT OPERATION NUM-
                BER"; A20%
152 IF A20%<13 THEN 155
153 PRINT "  *  *  *" : PRINT "IMPROPER
    SELECTION": PRINT "**********"
154 GOTO 112
155 IF A2 Q.%>0 THEN 158
156 SYSTEM
158 ON A20% GOSUB 170, 4400, 4530, 5500, 4500,
    7500, 8500, 9000, 9040, 9180,
159 GOTO 112
170 PRINT: PRINT "**********"
```

```
171 PRINT " SELECT OVERLAY FOR LOADING INTO IMAGE MEMORY"
172 PRINT "************": PRINT
173 PRINT "     RETURN TO MAIN MENU  0"
174 PRINT "     SELECT RECTANGULAR IMAGE MEMORY PATTERN"
180 PRINT "     HORIZONTAL BARS"
200 PRINT "     3-2-2  WIDTH BARS, INTENSITY VARATIONS .... 1"
220 PRINT "     1-1-1 WIDTH BARS, MAXIMUM INTENSITY ..... 2"
240 PRINT "     LINEAR COUNT, ALL COLOR COMBINATIONS ..... 8"
260 PRINT "     SOLID SINGLE COLORED IMAGES"
265 PRINT "     RECTANGLE ..... 3"
270 PRINT "     BACKGROUND .....4"
400 PRINT "     CHECKERBOARD"
420 PRINT "          4-COLORS ..... 6"
440 PRINT "          2-COLORS ..... 7"
442 PRINT "     VARIABLE SINGLE COLORS"
443 PRINT "     GREEN SAWTOOTH ..... 10"
460 PRINT "     CENTER ELEMENT"
480 PRINT "     9-PIXEL SQUARE ..... 11"
482 PRINT "     SELECT SLOPING LINE . 12"
484 INPUT "     SELECT PATTERN NUMBER";A5%
```

```
486  IF A5%>0 THEN 502
500  RETURN
502  IF A5%<13 THEN 520
503  PRINT "**********": PRINT "IMPROPER
     SELECTION": PRINT "**********
504  GOTO 170
520  IF A5%=3 OR A5%=4 OR A5%=12 THEN 523
     ELSE 535
523  PRINT " COLOR CODE"
524  PRINT "      BLACK ..... 0"
526  PRINT "      GREEN ..... 1 TO 7"
527  PRINT "      RED ..... 8, 16, 24"
528  PRINT "      BLUE ..... 32, 64, 96"
529  INPUT "      SELECT COLOR CODE
               SUM"; INT1%
530  IF INT1%<128 THEN 535
531  PRINT:PRINT "**********"
532  PRINT "IMPROPER COLOR CODE; ENTER
     COLOR CODE AGAIN"
533  PRINT "**********": PRINT
534  GOTO 523
535  IF A5%=11 THEN 2040
540  IF A5%=6 OR A5%=7 GOTO 560 ELSE 570
560  INPUT "CHECKERBOARD RESOLUTION,
     PIXELS PER SIDE";A.6%
570  IF A5%=4 THEN 575 ELSE 580
```

```
575  A5%=3:  XB%=0:  YB%=0: XE%=511:
     YE%=511: GOTO 623
580  INPUT " START PIXEL COORDINATE";
     XB%,YB%
620  INPUT " STOP PIXEL COORDINATE";
     XE%,YE%
623  GOSUB 630
624  GOTO 170
630  "**********************************
632  'SUBROUTINE TO OVERLAY A RECTAN-
     GLE
635  XB%=(XB%+1)*8: YB%=(YB%+1)*8
640  XE%=(XE%+1)*8: YE%=(YE%+1)*8
642' IF XB%=>8 AND XB%<XE% AND XE%=>8
     AND XB%=<512*8 AND XE%<512*8 THEN
     643
643' IF YB%=>8 AND YB%<YE% AND YE%=>8
     AND YB%=<512*8 AND YE%=<512*8 THEN
     660
656' PRINT:PRINT "***************"
657' PRINT "IMPROPER PIXEL COORDINATES,
     ENTER PIXEL COORDINATES AGAIN"
658  PRINT * * *  * * *  * *  * * * *"PRINT
659' GOTO 580
660' PRINT: PRINT  "***************"
665' PRINT " IMAGE  MEMORY IS BEING
     LOADED"  'PRINT "ROW", "COLOR I
666' PRINT "***************" : PRINT
```

```
667  IF A5%=12 THEN 4200
690  XPS%=256: YPS%=0: XRP%=XB%-8
695  GOSUB 3000
700  FOR OUTLP1%=YB% TO YE% STEP 8
     'ROW LOOP
710  YRP%=OUTLP1%-8   'UPDATE TO NEXT
     ROW
711  XRP%=XB%-8
712  GOSUB 3000 'LOAD IMP REGISTERS
948  OUT 236,32  'SET SEQUENTIAL LOAD
     COMMAND
1230      'DETERMINE INTENSITY (INT1%)
1240      ON A5% GOTO 1260, 1460, 1720, 1250,
          1250, 1920, 1980, 1800, 1250, 1820
1250      PRINT "*******************"; PRINT
          "SELECT A DIFFERENT IMAGE* :
          PRINT "*********************
1260      IF D%<8 THEN 1340   'IMAGE PAT-
          TERN 1
1280      IF D%<32 THEN 1380   '|-64-32-|-16-08-
          |-04-02-01-|
1300      IF D%<128 THEN /420   '|BLUE|RED
          |GREEN|
1320      INT1%=0: Dt=0: GOTO 1980
1340      INT1% = D% AND 7
1360      D%=D%+1: GOTO 1980
1380      INT1%=D% AND 24
1400      D%=D%+8:GOTO 1980
```

```
1420    INT1%=D% AND 96
1440    D%= D%+32: GOTO 1980
1460    A3%=FIX ((OUTLP1%-8)/8)    'IMAGE
        PATTERN 2
1480    GOSUB 1520
1500    GOTO 1980
1520    '******* SUBROUTINE, MAXIMUM
        COLOR ************************
1540    A4%=A3% AND 3
1560    A7%=A4%+1
1580    ON 7% GOTO 1600,1620,1640,1660
1600    INT1%=0: GOTO 1680
1620    INT1%=7: GOTO 1680
1640    INT1%=24: GOTO 1680
1660    INT1%=96
1680    RETURN
1700    '************************
1720    INT1%=INT1%; GOTO 1980
        'PATTERN-3, SOLID COLOR
1800    K2%=(OUTLP1%-8)/8:   INT1%=K2%
        AND 127: GOTO 1980 'PATTERN 8, LIN
1820    INT1%=K8%: K10%=K9% AND 1
1840    IF K10%=0 THEN 1920
1860    K8%=K8%+1       'UPCOUNT, ADD
1880    IF K8%<8 THEN 1980
1900    K9%=K9%+1-1: K8%=6: GOTO 1980
        'CHANGE COUNT DIRECTIO
```

```
1920    K8%=K8%-1    'DOWNCOUNT, SUBT.
1940    IF K8%>0 THEN 1980
1960    K9% = K9%+1: K8%=2: GOTO 1980
1980    SP1%=INIT1% AND 1: SP2%= INIT1% AND3: SP3%=INT1% AND 7: SP4%=INT1% AND AND 63: SP7%=INT1% AND 127
1985    OUT 238, 252: OUT 237, SP1%: OUT 237, SP2%: OUT 237, SP3%: OUT 237, SP4% 237, SP7%: OUT 237, INT1% 'DATA TO LOAD IN IMAGE MEMORY
1991    ON A5% GOTO 1994, 1994, 1994, 1994, 1994, 1992, 1993, 1994 ,1994, 1994
1992    A3% = FIX((2*OUTLP1%+INLP1%)/A6%): GOSUB 1520: GOTO 1994
1993    A3%=FIX((2*OUTLP1%+2*INLP1%)/A6%): GOSUB 1520: GOTO 1994
1994    FOR INLP1%=XB% TO XE% STEP 8 'PIXEL LOOP
1995    OUT 236,160: OUT 236,32
1996    NEXT INLP1%
1997    OUT 237, SP7%: OUT 237, SP6%: OUT 237, SPS%: OUT 237, SP4%: OUT 237,SP3%: 237,0 'DATA TO LOAD IN IMAGE MEMORY
1999    IF K200$="M" THEN
2000    A8%=INP (93): A8%=A8% AND 2: IF A8%=0 THEN 2009    'OPERATOR RESE
```

```
2001    A8%=INP(92): GOTO 2006
2002    A8%=INP (1): A8%=A8% AND 2: IF
        A8%=0 THEN 2009      'OPERATOR
        RESE
2003    A8%=INP (0)
2006    ,A9%=A8% XOR 155: IF A9%=0 THEN
        100  -'ESCAPE TO MENU
2007    A9%=A8% XOR 127: IF A9%=0 THEN
        2008 ELSE 2009 'DELETE TO SYSTEM
2008    SYSTEM
2009    NEXT OUTLP1%
2010    PRINT CHR$(7); :PRINT "MEMORY
        LOAD COMPLETE"
2020    RETURN          'RETURN TO' OVER-
        LAY MENU
4510    'BLACK BACKGROUND WITH COOR-
        DINATE SYMBOLS
```

4.3 MORE DETAILED RESPONSE REGARDING THE CONFORMANCE OF "MAKING A PRODUCT" CLAIMS TO 35 USC 271(G)

As discussed in Section 3.8 above, the statutory phrase "a product which is made by a process" establishes that a process claim has a product associated with it and the process claim covers such a product without the process claim even reciting the product made by the process. Thus, following the rationale of the rejection of claims 153-172, the parent process claims from which the "making a product" claims 153-172 depend should also be rejected for reciting (implicitly) such a limitation. Be-

cause those parent process claims are not thus rejected, the "making a product" claims depending therefrom should not be thus rejected for the same reasons that the parent process claims and not thus rejected.

In effect, because an implicit "product" process claim limitation is adequate to satisfy the written description requirement, making this implicit "product" process claim limitation explicit with a recitation in a dependent claim must certainly also be adequate to satisfy the written description requirement.

Satisfying the enablement requirement also satisfies the written description rejection for the "making a product" claims. This is because enablement confirms that the disclosure teaches the making and using of the claimed invention and "making and using" implies "making a product". Certainly enabled claims teach the making of the invention and the invention is a product.

The Board recognizes that "product" terminology is statutory terminology (Decision at 39):

> Appellant argues that "product" terminology is statutory language under 35 U.S.C. § 271(g) (Br29 § 8.1.6).
>
> The issue is not whether "product" is statutory language, but whether there is written description support for the step of making a product in response to certain information.

However, the statute clearly establishes that a product is always associated with a process claim. Thus, any explicit product claim depending from a process claim inherently satisfies the written description requirement.

Moreover, products are expressly disclosed see below).

The rejection is erroneously based upon equating "product" to "signal", but a signal product is not the issue. The Board states (Decision at 39-41):

> Appellant argues that products include "machines" and "manufactures" and that clearly the disclosed apparatuses constitute "machines" and "manufactures" and, hence, products (Br29-30 § 8.1.6). Therefore, the disclosed signals constitute "manufactures" (and hence "products") because the signals are physical things made by the disclosed circuits (Br30).
>
> The terminology "producing [sic, making] a product" finds no written description support in the specification. Appellant's position is that the "products" can be a signal. We disagree. First, the claims recite "making a product in response to ... image information," where the "image information" is the signal and the "product" must be something else, which is not disclosed.
>
> Second, the three product classes (machine, manufacture, and composition of matter) have traditionally required physical structure or matter and a signal, while physical, does not have a tangible physical structure. A "composition of matter" "covers all compositions of two or more substances and includes all composite articles, whether they be results of chemical union, or of mechanical mixture, or whether they be gases, fluids, powders or solids." . . . A signal is not matter, but is a form of energy, and therefore is not a composition of matter.

> "The term machine includes every mechanical device or combination of mechanical device or combination of mechanical powers and devices to perform some function and produce a certain effect or result." Corning v. Burden, 56 U.S. (15 How.) 252, 267 (1854); see also Burr v. Duryee, 68 U.S. (1 Wall.,) 531, 570 (1863) (a machine is a concrete thing, consisting of parts or of certain devices and combinations of devices). A modern definition of machine no doubt includes electronic devices which perform functions. Indeed, devices such as flip-flops and computers are referred to in computer science as sequential machines. A signal, while physical, has no concrete tangible physical structure, and does not itself perform any useful, concrete and tangible result; thus, a signal does not fit within the definition of a machine (or product).
>
> The Supreme Court has read the term "manufacture" in accordance with its dictionary definition to mean "the production of articles for use from raw or prepared materials by giving to these materials new forms, qualities, properties, or combinations, whether by hand-labor or by machinery." . . . . These definitions require physical substance, which a signal does not have. Accordingly, we conclude that a signal is not a product.

However, the Appellant's "signal" statement was an "[a]lso" statement, the primary statement was directed to "the disclosed apparatuses" (Appeal Brief at 30 (emphasis added)):

> Clearly, **the disclosed apparatuses** (e.g., circuits) constitute "machines" and "manufactures" and hence "products". Also, the disclosed signals constitute

> "Manufactures" (and fence "products") because the signals are physical things[13] that are made, for example, by the disclosed circuits.

Hence, the Board should reverse the written description rejections of 153-172 because it appears undisputed that apparatuses are products. Further, it is undisputed that many of the apparatuses are adequately disclosed—the application has allowable claims[14] and, the Decision articulates portions of the disclosure that are adequate (e.g., Decision at 14-18).

The Decision states (Decision at 42):

> Appellant argues that the disclosure recites ample product related terminology, such as "constructed," "manufactured," "implemented," "interconnected," etc. (Br32-33 § 8.1.7).
>
> These terms deal with the apparatus and have not been shown to be relevant to the claimed process limitation of "producing (sic, making] a product."

However, the claimed process is disclosed as being implemented with the disclosed apparatuses (e.g., the disclosed actually reduced-to-practice "Experimental System") and the disclosed apparatuses is an embodiment of the product that is made with the process.

---

[13] Signals are "necessarily physical." Arrhythmia Research Technology Inc. v. Corazonix Corp., 22 USPQ2d 1033, 1038 (Fed. Cir. 1992). See also In re Taner et. al., 214 USPQ 678, (CCPA 1982); In re Sherwood, 613 F.2d 809, 204 USPQ 537, 545 FN 8 (CCPA 1980); and In re Johnson, 589 F.2d 1070, 200 USPQ 199 (CCPA 1978).

[14] Those claims having all rejections reversed.

For example, the "making a product" claim 154 depends from the allowable process claim 82, and operates "in response to the output image information". Moreover, the disclosed CRT display operates "in response to the output image information". It should be indisputable that the disclosed actually reduced-to-practice "Experimental System" provides a display system product. Thus, the apparatus terms in the disclosure establish that an apparatus product is disclosed and this apparatus product is disclosed as being made with the process of an allowable parent claim.

V. DISCUSSION OF THE STATEMENTS IN THE DECISION

5.1 THE BOARD'S COMMENTS ON TABLE-1 IN THE APPEAL BRIEF

The Board makes various statements about Table-1 in the Appeal Brief at 25 (Decision at 19):[15]

> Appellant argues that there is literal support for the limitation because the individual words of the limitation are found somewhere in the specification, referring to Table 1 (Br 25) for a listing of occurrences of the terminology "compress" (4 occurrences on page 23), "data compressed" (1 occurrence on page 23), "decompressed" (1 occurrence on page 23), "information" (>100 occurrences throughout the specification), "input" (>200 occurrences throughout the specification), and "video" (8 occurrences on pages 77, 166, 168-171).

---

[15] See also the Board's other comments about Table-1 (Decision at 12-13, 14, 25, 26-27, 28, 29-30, 32, 34, 35, 35-36, and 38-39).

> Merely pointing to individual words of the limitation scattered throughout the specification is totally unpersuasive of possession of the invention because words in isolation do not describe the structure, functions, and interconnections among elements defined by the words when combined together in the limitation.

However, the Examiner did not construe the claims nor consider the claims as a whole nor establish a prima facie case, as required by the Federal Circuit, and the Examiner did not address the disclosed actually reduced-to-practice "Experimental System". The Examiner should have considered the citations to the disclosure and responded thereto, but he did not do so, and the Examiner should have at least considered the block diagrams (Figs. 1, 2, and 6A) relative to Table-1, but he did not do so. Further, as discussed above, the Federal Circuit in Union Oil established that such a table by itself can satisfy written description.

5.2 THE EXAMINER AND THE BOARD DISREGARDED THE FACT THAT THE DISCLOSURE IS, IN LARGE PART, DIRECTED TO AN ACTUALLY REDUCED-TO-PRACTICE "EXPERIMENTAL SYSTEM"

The Examiner and the Board misapprehend the fact that the disclosure is, in large part, directed to an actually reduced-to-practice "Experimental System". It is unfair to cast this significant disclosure as "isolated words scattered throughout the specification", "a dictionary", "isolated words of the limitation spread out over

the specification", and "'[p]icking and choosing" terms to assemble limitations':[16]

> The merits of the disclosure are addressed in connection with the individual rejections. We agree with the examiner that merely pointing to isolated words scattered throughout the specification does not describe the invention claimed as a combination of elements, functions, and interconnections, anymore than a dictionary provides written description support for a book where words are used in combination to provide a certain meaning.
>
> The examiner does not require in haec verba (verbatim) support for the claimed subject matter at issue. The examiner properly requires appellant to show written description support for the claim limitation as a whole and not just for isolated words of the limitation spread out over the specification.
>
> * * *
>
> Appellant merely provides a Table 1 (Br25) that lists occurrences of words in the limitations somewhere in the specification. "Picking and choosing" terms to assemble limitations without ever disclosing the combination in one location does not establish possession of the claimed limitations pointed out by the examiner as being without support.

In the instant application, the Appellant designed, constructed, and operated the disclosed actually reduced-to-practice "Experimental System". This establishes an

[16] Decision at 13 and 14, respectively (emphasis in original).

extensive disclosure, much more than is required by § 112-1. Yet this disclosed actually reduced-to-practice "Experimental System" embodiment was ignored by the Examiner.

Listing of the disputed claim limitations and citing to the disclosure is not like "a dictionary", nor "isolated words", nor "[p]icking and choosing ... without-ever disclosing the combination in one location" does not fairly characterize the disclosure. This is an integrated disclosure, arranged in a top-down end-to-end format (Appeal Brief at Section V) and in a functional manner that an artisan in 1984 would expect to find (Section 1.3 herein)

The CCPA, in Honn stated:[17]

> While addition to the disclosure of a more detailed specific embodiment of the *process* of preparing the copolymers . . . might have been helpful, the information that is in the disclosure, considered as a whole, would clearly teach those skilled in the art what the invention is and how to practice it.

Thus, in the instant application, the very detailed disclosed actually reduced-to-practice "Experimental System" embodiment is much more than adequate.

---

[17] In re Honn, 364 F.2d 454, 150 USPQ 652, 657 (CCPA 1966) (emphasis in original)

5.3 AN ARTISAN WOULD EXPECT A COMPUTER SYSTEM TO BE DOCUMENTED IN THE FUNCTIONAL FORMAT OF THE INSTANT DISCLOSURE AND THE CCPA CONDONES SUCH A DISCLOSURE

The instant disclosure is arranged in a functional format that an artisan would expect to see.[18] Such a functional format is illustrated by a representative prior art user's manual Exhibit-7 herein).[19] See also the functional formats of the technical manuals and user's manuals for the computer boards, for the computer peripherals, and for the other commercially available products that were used in the disclosed actually reduced-to-practice "Experimental System" embodiment.[20]

---

[18] See the Table of Contents, Appeal Brief at Exhibit-1.

[19] See the table of contents in the operator terminal User's Manual for the Viewpoint/3A Plus at pages v-viii therein (Exhibit-7 herein). This is the operator terminal used in the disclosed actually reduced-to-practice "Experimental System" (Spec. at 95, 97, and 237). A copy of this Users Manual was filed in the PTO under the PTO disclosure document program and was incorporated-by-reference in the instant application as filed (Spec. at 237). This disclosure document (No. 131,747) was permanently "retained" by the PTO. See the official PTO "RETENTION LABEL" in Exhibit-6 herein.

[20] See the tables of contents in the manuals for the commercially available products used in the disclosed actually reduced-to-practice "Experimental System" (Spec. at 95-98 and 237-238). Copies of these manuals were filed in the PTO under the PTO disclosure document program and were incorporated-by-reference in the instant application as filed (Spec. at 237). This disclosure document (No. 131,747) was permanently "retained" by the PTO. See the official PTO "RETENTION LABEL" in Exhibit-6 herein. Copies of this PTO Disclosure Document will be provided to the Board upon request.

The functions for the major elements are shown coupled together in block diagram form in Figs. 1, 2, 5A, 5D, and 6A. Then, with this roadmap, an artisan can refer to the specific functional sections[21] to find out which additional elements are contained in the blocks and the details of implementation of the blocks. For example, the "SUPERVISORY PROCESSOR" block (e.g., block 610A in Fig. 6A) is disclosed as including various internal computer boards, computer software, and computer peripherals with detailed interconnections (e.g., computer backplane and peripheral input/output cards) and clearly stated functions. See the section entitled "S-100 Bus System" (Spec. at 95-98). Similarly, the "ADDRESS GENERATORS" block (e.g., block 610C in Fig. 6A) is disclosed as including two dimensional address circuitry, update circuitry, and angle scanout circuitry.

The CCPA in Honn established that the PTO must consider the disclosure as a whole rather that restricting it to a paragraph and label:[22]

> A specific embodiment of the invention may be found in the disclosure considered as a whole, and need not of necessity be restricted to a paragraph labeled 'example'.

In view of the above, the instant disclosure provides what an artisan would have expected to find, what an artisan would need to understand the technology, and an artisan would have been convinced that the Appellant was in possession of the claimed invention (Decision at 18):

---

[21] See the Table of Contents, Exhibit-1 of the Appeal Brief.

[22] In re Honn, 364 F.2d 454, 150 USPQ 652, 656 (CCPA 1966 (emphasis added)).

> The specification discloses a software program LD.ASC for loading vectors into memory and a software program GRAPH.ASC for refreshing a CRT monitor from memory (spec. at 91, last para.; LD.ASC described at 10-14 and listing at 217-230; GRAPH.ASC mentioned at 10 and listing at 214-216). A processor is clearly required to perform these functions. The relevant program to the claimed processors is the program GRAPH.ASC which reads data from memory. The operation of the program is not described except in the cryptic comments to the program. However, insofar as we can tell, the program only reads data from memory and does not perform any kind of processing on the data.

However, the GRAPH.ASC does far more than read data from memory, for example, it processes such as by calculating the addresses, synchronizing with the field sync pulse, and other such functions.

The Board is requested to take notice of what appears to be an inadvertent typo (the bolded "not" quoted below) (Decision at 24 (emphasis added)):

> That is, the processor may be thought of as a processor for writing information into the block memory and a processor for accessing (reading) information from block memory and controlling further operations, such as the spatial processing of figure AG and 6AH, although the drawings, such as figure 1, **do not** illustrate a processor block connected to the memory, buffer, and output device. **Thus, there is support for a processor "coupled to the accessing circuit and coupled to the vector generator."**

VI. THE LAW OF WRITTEN DESCRIPTION

See the excerpts regarding written description from the Reply Brief dated March 28, 2002 in copending application Serial No. 08/433,786 (Docket No. 602) set forth in Exhibit-9 herein and incorporated-by-reference.

6.1 THE CCPA IN BANC DECISION IN ANGSTADT, THAT WRITTEN DESCRIPTION IS "RELATIVELY SIMPLE TO COMPLY WITH" SHOULD BE DISPOSIVE OF THE WRITTEN DESCRIPTION REJECTION

It is established that the instant disclosure is fully enabling and that the elements are literally disclosed. Hence, the holding in Angstadt should be dispositive of the written description rejection.

The CCPA in Angstadt held that the written description requirement is relatively simple to comply with:[23]

> Two of the first paragraph requirements indicated above, i.e. , the **"description of the invention"** and the **"best mode" requirements, are relatively simple to comply with and thus will ordinarily demand minimal concern on the part of the Patent Office** * * * What is of maximum concern in any analysis of whether a particular claim is supported by the disclosure in an application is whether that disclosure contains sufficient teaching regarding the subject matter of the claims as to enable one skilled in the pertinent art to make and use the claimed invention.

---

[23] In re Angstadt and Griffin, 537 F.2d 498, 190 USPQ 214, 217 (CCPA 1976) (emphasis added).

Even though the CCPA has told the PTO that the written description requirement is "relatively simple to comply with and thus will ordinarily demand minimal concern on the part of the Patent Office" (see Angstadt), the Examiner disregards this legal directive—simplicity of compliance.

6.2 THE ISSUES IN EX PARTE RICHARDS COMPEL A SIMILAR REVERSAL OF THE § 112-1 REJECTION BASED UPON DISCLOSURE OF "INTERCONNECTIONS" AND FAILURE OF THE EXAMINER TO ESTABLISH A PRIMA FACIE CASE

Judge Smith, Judge Fleming, and Judge Dixon in Richards[24] found that an apparently sparse disclosure of "standard components" and the failure of the Examiner to establish a prima facie case warranted reversal of an enablement rejection. These issues are very similar to the issues in the instant appeal which is based upon an issue of "interconnections" and involves an extensively briefed issue of the failure of the Examiner to establish a prima facie case.[25] While the appellant in Richards merely relies on parts of three pages of disclosure for an example, the present Appellant, in significant contrast thereto, relies on extensive detailed disclosure of an actually reduced-to-practice "Experimental System" embodiment and much more. Further, the appellant in Richards

---

[24] *Ex parte* Richards, Appeal No. 1999-1847 (Bd. Pat. App. & Int.) (unpublished opinion), at http://www.uspto.gov/web/offices/dcom/bpai/decisions/fd991847.pdf. See also U.S. Patent No. 6,382,101 (issued May 7, 2002 to Richards).

[25] The Appeal Brief and the Reply Brief discuss at length the failure of the Examiner to establish a prima facie case .

failed to argue a prima facie case issue, yet the board therein still held that "the examiner has not met his burden" (Richards at 4). In significant contrast thereto, the present Appellant argued the prima facie case issue extensively in the briefs, yet the Board held that the Examiner had met his burden (Decision at 7).

The Board is requested to treat the issues of "interconnections" and the Examiner's failure to establish a prima facie case in the instant application in the same manner that the Board treated these issues in Richards at 3-4:

OPINION . . .

> The examiner maintains that the structural connections, circuitry and cooperation are not sufficiently disclosed . . . We find that the examiner has not attempted to establish why the supporting specification in combination with the relevant prior art fails to enable the claims which is the examiner's initial burden. In re Marzoccbi, 439 F.2d 220, 223, 169 USPQ 367, 369 (CCPA 1971). From our review of the examiner['s] rejection, the examiner maintains that the programming and specific interconnection of the functional units "must" be disclosed in the specification. . . . We disagree with the examiner. The examiner provides no reasoned analysis of why these would be needed or required. . . . The examiner carries the initial burden to establish a case. Here, the examiner has not met his burden, and we will not sustain the rejection of claims 7-12 under 35 U.S.C. § 112, first paragraph.

However, appellant has not argued that the examiner failed to establish a *prima facie* case, but merely

that the specification is enabling to those skilled in the art. . . .

It is worth repeating (Richards at 3-4):

> From our review of the examiner['s] rejection, the examiner maintains that the programming and specific interconnection of the functional units "must" be disclosed in the specification. . . . We disagree with the examiner. The examiner provides no reasoned analysis of why these would be needed or required.

If "the programming and specific interconnection of the functional units" need not be disclosed in Richards, then it seems inconsistent to affirm the § 112-1 rejection in the instant application which has extensive disclosure of "programming and specific interconnection of the functional units". As in Richards, the instant claimed invention makes extensive use of such "standard components which are connected by standard electrical connections". See Section 6.2 herein.

In Richards, the Board found that "a basic example of the operation of the invention" on parts of three pages of the specification was sufficient (Richards at 4):

> However, appellant has not argued that the examiner failed to establish a *prima facie* case, but merely that the specification is enabling to those skilled in the art. . . . Furthermore, appellant relies on a basic example of the operation of the invention at pages 5 and 6 of the brief. Appellant cites to only specific portions of pages 5, 6, and 7 of the specification to support the example.

If this was sufficient to support a finding in Richards that the specification is enabling, then certainly the instant disclosure with more than 20 figures (e.g., Figs. 1, 2, and 6A-6V) and more than 100 pages of very detailed written disclosure (e.g., Spec. at 291-405) specifically directed to the disclosed actually reduced-to-practice "Experimental System" embodiment (in addition to extensive additional disclosure) must be sufficient.

The instant disclosed actually reduced-to-practice "Experimental System" embodiment with its extensive use of "standard components which are connected by standard electrical connections" (e.g., commercially available products) must certainly be sufficient in view of the Board's finding in Richards that "standard components . . . connected by standard electrical connections" are sufficient (Richards at 4):

> Appellant argues that the devices in the specification and claims are standard components which are connected by standard electrical connections and that one skilled in the art would be able to make and use the invention without undue experimentation. We agree with appellant.

In view of the Board's holding in Richards, the instant disclosed actually reduced-to-practice "Experimental System" embodiment having significantly greater disclosure than the applied references must certainly be sufficient. In Richards, the Board reached its decision regarding the sufficiency of Richards' disclosure by noting that the Wuhrl reference "contains a similar level of description as the instant description with respect to the interconnection of standard elements and does not provide any of the specifics for programming these standard functional units" (Richards at 4-5):

> Specifically, the prior art to Wuhrl applied against the claims is indicative of the level of skill in the relevant art. Wuhrl contains a similar level of description as the instant description with respect to the interconnection of standard elements and does not provide any of the specifics for programming these standard functional units. Similarly, we find that from the basic functional description of these standard components, it would have been obvious to one of ordinary skill in the art at the time of the invention to program and interface these components together to make and use the system to aid in the selection of ink fountains for adjustment by an operator.

Just as in Richards, the applied references in the instant application have much less disclosure than the instant application but are still presumed to be sufficiently disclosed. For example, Beaulier is the lead reference for one of the § 103 rejections. Beaulier has only a single figure, a low detail block diagram, and has less than three columns total of detailed description (col. 2:60 - col. 5:5). In significant contrast, the instant disclosure has more than 20 figures (e.g., Figs. 1, 2, and 6A-6V) and more than 100 pages of very detailed written disclosure (e.g., Spec. at 291-405) specifically directed to the disclosed actually reduced-to-practice "Experimental System" embodiment (in addition to extensive additional disclosure).

In Richards, the Board commented that it would have been obvious for an artisan to program and interface the standard components "from the basic functional description of these standard components" (Richards at 5):

> Similarly, we find that from the basic functional description of these standard components it would have been obvious to one of ordinary skill in the art at the time of the invention to **program and interface** these components together to make and use the system to aid in the selection of ink fountains for adjustment by an operator.

However, the instant application discloses far more than a "basic functional description of . . . standard components". It discloses commercially available operating system software and source code for custom computer programs (e.g.; Spec. at 303-305 and 389-405) and it discloses commercially available computer interface boards (e.g., two Compupro Interfacer-II board and one Compupro System Support board (e.g., Spec. at 294, 301, 303, and 304; respectively (emphasis added)). See Spec. at 303 (emphasis added):

> The computer is implemented with various S-100 boards manufactured by CompuPro including the 8085-8088 CPU board, RAM 16 and RAM 17 memory boards, **a System Support board**, and a **pair of Interfacer 2 boards**. One Interfacer 2 board is used **to interface to the terminal and printers**. The other Interfacer 2 board provides **the 3-channel parallel interface** to the control logic. These boards are described in detail in the referenced manuals.

And this disclosure is in the highly predictable electronics art where one skilled in the art would know how to program and interface standard components. This notwithstanding the fact that the instant application has extensive programming and interfacing disclosure.

Please charge any fees associated with the papers transmitted herewith to Deposit Account No. 08-3626.

CERTIFICATION OF MAILING BY EXPRESS MAIL: I hereby certify that this correspondence is being deposited with the United States Postal Service with Express Mail post office to addressee service under 37 CFR 1.10, postage prepaid, in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231 with the express mail label number EV 069541615 September 30, 2002.

Respectfully submitted,

Date: Sept. 30, 2002 /s/ GILBERT P. HYATT

GILBERT P. HYATT
Registration No. 27,647
[address and phone
number omitted]

PETITIONER'S BRIEF

No. 10-1219

In the Supreme Court of the United States

DAVID J. KAPPOS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR, UNITED STATES PATENT AND TRADEMARK OFFICE, PETITIONER

v.

GILBERT P. HYATT

ON WRIT OF CERTIORARI TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

BRIEF FOR THE PETITIONER

DONALD B. VERRILLI, JR.
Solicitor General
Counsel of Record

TONY WEST
Assistant Attorney General

MALCOLM L. STEWART
Deputy Solicitor General

BETH S. BRINKMANN
Deputy Assistant Attorney General

GINGER D. ANDERS
Assistant to the Solicitor General

SCOTT R. MCINTOSH
Attorney

Department of Justice
Washington, D.C. 20530-0001
SupremeCtBriefs@usdoj.gov
(202) 514-2217

BERNARD J. KNIGHT, JR.
General Counsel

RAYMOND T. CHEN
Solicitor and Deputy General Counsel

ROBERT J. MCMANUS
THOMAS W. KRAUSE
Associate Solicitors
U.S. Patent and Trademark Office
Alexandria, VA 22313

QUESTIONS PRESENTED

When the United States Patent and Trademark Office (PTO) denies an application for a patent, the applicant may seek judicial review of the agency's final action through either of two avenues. The applicant may obtain direct review of the agency's determination in the Federal Circuit under 35 U.S.C. 141. Alternatively, the applicant may commence a civil action against the Director of the PTO in federal district court under 35 U.S.C. 145. In a Section 145 action, the applicant may in certain circumstances introduce evidence of patentability that was not presented to the agency. The questions presented are as follows:

1. Whether the plaintiff in a Section 145 action may introduce new evidence that could have been presented to the agency in the first instance.

2. Whether, when new evidence is introduced under Section 145, the district court may decide de novo the factual questions to which the evidence pertains, without giving deference to the prior decision of the PTO.

TABLE OF CONTENTS

Page

Opinions below 1
Jurisdiction 1
Statutory provision involved 2
Statement 2
Summary of argument 11
Argument:
I. Consistent with established principles of administrative law, 35 U.S.C. 145 is properly construed to limit evidence not presented to the PTO and provide for deferential review 14
A. A Section 145 suit is a proceeding for judicial review that is governed by traditional administrative-law principles 14
1. Section 145 authorizes judicial review of the PTO's decision 14
2. Traditional administrative-law principles govern the admissibility of new evidence and the standard of review in Section 145 proceedings 18
B. Evidence that reasonably could have been presented to the PTO should not be admissible in Section 145 suits, and the PTO's decision should be reviewed deferentially in all cases 21
1. Permitting introduction of new evidence that could have been presented to the agency conflicts with administrative-exhaustion principles 21
2. Permitting de novo review of issues involving new evidence conflicts with long-standing principles of deference to agency authority and expertise 25

Table of Contents—Continued: Page

II. Congress's reenactment of Section 145 in the Patent Act of 1952 should be understood to incorporate the prevailing judicial practice of limiting the introduction of new evidence and applying a deferential standard of review 30
A. This court's analysis of R.S. 4915 in *Morgan* supports limitations on new evidence and deferential review of the PTO's factfindings 31
B. Under R.S. 4915, the prevailing judicial practice following *Morgan* was to exclude evidence that the plaintiff had failed without cause to present to the PTO 34
C. When Congress reenacted R.S. 4915 as Section 145, it adopted the prevailing judicial understanding of R.S. 4915 38
III. New evidence should be admitted in a Section 145 suit only if its proponent had no reasonable opportunity to present it to the PTO, and the court should overturn the PTO's decision only if the evidence clearly establishes that the agency erred 42
Conclusion 47

TABLE OF AUTHORITIES

Cases:

Abbott v. *Shepherd*, 135 F.2d 769 (D.C. Cir. 1942) 37
American Hoist & Derrick Co. v. *Sowa & Sons, Inc.*, 725 F.2d 1350 (Fed. Cir.), cert. denied, 469 U.S. 821 (1984) 26, 27
Ashwander v. *TVA*, 297 U.S. 288 (1936) 35
Barrett v. *Failing*, 111 U.S. 523 (1884) 31

Cases—Continued: Page

Barrett Co. v. *Koppers Co.*, 22 F.2d 395 (3d Cir. 1927) 35
Beard v. *Burts*, 95 U.S. 434 (1877) 12, 32
Boucher Inventions, Ltd. v. *Sola Elec. Co.*, 131 F.2d 225 (D.C. Cir. 1942), cert. denied, 318 U.S. 770 (1943) 34
Bryan v. *United States*, 524 U.S. 184 (1998) 39
Butterworth v. *United States*, 112 U.S. 50 (1884) 33
Cabinet Mountains Wilderness v. *Peterson*, 685 F.2d 678 (D.C. Cir. 1982) 20
California Research Corp. v. *Ladd*, 356 F.2d 815 (D.C. Cir. 1966) 38
Chandler v. *Roudebush*, 425 U.S. 840 (1976) 9, 20, 31
Citizens to Preserve Overton Park, Inc. v. *Volpe*, 401 U.S. 402 (1971) 22
Consolo v. *Federal Mar. Comm'n*, 383 U.S. 607 (1966) 18, 25
Cordis Corp. v. *Boston Scientific Corp.*, 561 F.3d 1319 (Fed. Cir.), cert. denied, 130 S. Ct. 748, and 130 S. Ct. 749 (2009) 28
DeSeversky v. *Brenner*, 424 F.2d 857 (D.C. Cir. 1970) 38, 40
Dickinson v. *Zurko*, 527 U.S. 150 (1999) ..... *passim*
Dowling v. *Jones*, 67 F.2d 537 (2d Cir. 1933) 37
Etten v. *Kauffman*, 32 F. Supp. 186 (W.D. Pa. 1940), aff'd, 121 F.2d 137 (3d Cir. 1941) 36
Fisher, In re, 448 F.2d 1406 (C.C.P.A. 1971) 16
Florida Power & Light Co. v. *Lorion*, 470 U.S. 729 (1985) 22, 25, 44

Cases—Continued: Page

Forest Grove Sch. Dist. v. *T.A.*, 129 S. Ct. 2484 (2009) ... 38
Gandy v. *Marble*, 122 U.S. 432 (1887) 34
Globe-Union, Inc. v. *Chicago Tel. Supply Co.*, 103 F.2d 722 (7th Cir. 1939) 36, 37, 40
Gold v. *Newton*, 254 F. 824 (2d Cir. 1918), cert. denied, 249 U.S. 608 (1919) 37
Gould, In re, 673 F.2d 1385 (C.C.P.A. 1982) 16
Gould v. *Quigg*, 822 F.2d 1074 (Fed. Cir. 1987) 15
Graham v. *John Deere Co.*, 383 U.S. 1 (1966) 3, 15
Greene v. *Beidler*, 58 F.2d 207 (2d Cir. 1932) 36
Hien, In re, 166 U.S. 432 (1897) 33
Hoover Co. v. *Coe*, 325 U.S. 79 (1945) 4, 5, 15, 16, 33
INS v. *Orlando Ventura*, 537 U.S. 12 (2002) 25, 26
Interstate Commerce Comm'n v. *Union Pac. R.R.*, 222 U.S. 541 (1912) 25
Kelly v. *Robinson*, 479 U.S. 36 (1986) 39
Knutson v. *Gallsworthy*, 164 F.2d 497 (D.C. Cir. 1947) .. 36
Kronig, In re, 539 F.2d 1300 (C.C.P.A. 1976) 43
Lorillard v. *Pons*, 434 U.S. 575 (1978) 38
McCarthy v. *Madigan*, 503 U.S. 140 (1992) 22
McKart v. *United States*, 395 U.S. 185 (1969) 22, 44
Microsoft Corp. v. *i4i Ltd. P'ship*, 131 S. Ct. 2238 (2011) ..... *passim*
Minnesota Mining & Mfg. Co. v. *Carborundum Co.*, 155 F.2d 746 (3d Cir. 1946) 35, 37
Morgan v. *Daniels*, 153 U.S. 120 (1894) ..... *passim*
Nichols v. *Minnesota Mining & Mfg. Co.*, 109 F.2d 162 (4th Cir. 1940) 37

Cases—Continued: Page

O'Donnell v. *United Shoe Mach. Corp.*, 2 F. Supp. 178 (D. Mass. 1933) 36
Pintarelli v. *Brogan*, 65 F. Supp. 281 (D.R.I. 1946) 41
Putman v. *Dudas*, 539 F. Supp. 2d 414 (D.D.C. 2008) ... 44
Radio Corp. of Am. v. *Radio Eng'g Labs., Inc.*, 293 U.S. 1 (1934) 27
S. & S. Corrugated Paper Mach. Co. v. *George W. Swift, Jr., Inc.*, 176 F.2d 358 (3d Cir. 1949) 37
Schering Corp. v. *Marzall*, 101 F. Supp. 571 (D.D.C. 1951) 36
Schilling v. *Schwitzer-Cummins Co.*, 142 F.2d 82 (D.C. Cir. 1944) 35, 37
Scotten v. *Littlefield*, 235 U.S. 407 (1914) 32
Southard v. *Russell*, 57 U.S. (16 How.) 547 (1854) 32
Squire, In re, 22 F. Cas. 1015 (C.C.E.D. Mo. 1877) 33
Tagg Bros. & Moorhead v. *United States*, 280 U.S. 420 (1930) 22
United States v. *Carlo Bianchi & Co.*, 373 U.S. 709 (1963) 18, 20, 23
Wainwright v. *Sykes*, 433 U.S. 72 (1977) 28
Woodford v. *Ngo*, 548 U.S. 81 (2006) 24

Statutes, regulations and rule:

Act of July 4, 1836, ch. 357, § 16, 5 Stat. 123 ..... 4, 5
Act of Mar. 3, 1839, ch. 88, § 10, 5 Stat. 354 ..... 4, 5
Act of Mar. 2, 1927, ch. 273, 44 Stat. 1335:
§ 8, 44 Stat. 1336 5
§ 11, 44 Stat. 1336 5

Statutes, regulations and rule: Page

Administrative Procedure Act, 5 U.S.C. 701 *et seq.* 3
5 U.S.C. 702 20
5 U.S.C. 704 39
5 U.S.C. 706 ..... 20, 25, 39
Civil Rights Act of 1964, 42 U.S.C. 2000e *et seq.* (Tit. VII) 20, 21
Contract Disputes Act of 1978, 41 U.S.C. 609(a)(3) 19
Endangered Species Act of 1973, 16 U.S.C. 1540(g)(1) (1976) 20
Food Stamp Act of 1977, 7 U.S.C. 2023(a)(15) 19
Freedom of Information Act, 5 U.S.C. 552(a)(4)(B) 19
Patent Act of 1870, ch. 230, § 52, 16 Stat. 205 5
Patent Act of 1952, 35 U.S.C. 1 *et seq.*:
35 U.S.C. 2(a) 15
35 U.S.C. 2(a)(1) 2
35 U.S.C. 6 (2006 & Supp. III 2009) 3
35 U.S.C. 6(a) (Supp. III 2009) 3
35 U.S.C. 101 2
35 U.S.C. 102 2
35 U.S.C. 103(a) 2
35 U.S.C. 112 ..... 2, 6
35 U.S.C. 120 3
35 U.S.C. 131 2
35 U.S.C. 131-132 42
35 U.S.C. 132(a) 6
35 U.S.C. 134 3
35 U.S.C. 135 4

Statutes, regulations and rule—Continued: Page

35 U.S.C. 141 ..... 3, 15, 18, 19
35 U.S.C. 141-145 3
35 U.S.C. 141-146 (Chap. 13) 15
35 U.S.C. 144 ..... 3, 18
35 U.S.C. 145 ..... *passim*
35 U.S.C. 146 5
35 U.S.C. 282 26
Rev. Stat. (1878):
§ 4911 ..... 33, 40
§§ 4911-4914 5
§ 4915 ..... *passim*
18 U.S.C. 923(f)(3) 19
28 U.S.C. 2640(a) 19
37 C.F.R.:
Section 1.2 44
Section 1.53(b) 3, 24
Section 1.105 42
Section 1.105(a)(1) 6
Section 1.113 42
Section 1.114 ..... 3, 24
Section 1.130 42
Section 1.131 42
Section 1.192(a) (1992) 8
Section 41.33 43
Section 41.33(d)(1) 24
Section 41.37(c)(1)(vii) 8, 24
Section 41.39(b)(1) 24

Regulations and rule—Continued: Page

Section 41.50(a)(2)(i) 24
Section 41.50(b) 43
Section 41.50(b)(1) 24
Section 41.52 3
Section 41.52(a)(1) 43
Fed. R. Civ. P. 2 20

Miscellaneous:

2 Anthony William Deller, *Walker on Patents: Deller's Edition* (1937) 36
Procedure in the Patent Office: Hearing on H.R. 7563 and H.R. 13487 Before the House Comm. on Patents, 69th Cong., 2d Sess. (1926) 41
S. Rep. No. 1979, 82d Cong., 2d Sess. (1952) 6, 30, 38
Benjamin J. Shipman, *Handbook of the Law of Equity Pleading* (1897) 5, 31, 32
2 Thomas Atkins Street, *Federal Equity Practice* (1909) 32
To Amend Section 52 of the Judicial Code and Other Statutes Affecting Procedure in Patent Office: Hearing on H.R. 6252 and H.R. 7087 Before the House Comm. on Patents, 69th Cong., 1st Sess. (1926) 41
U.S. Patent & Trademark Office, U.S. Dep't of Commerce, *Manual of Patent Examining Procedure* (8th ed. Rev. 8, July 2010) 2

In the Supreme Court of the United States

No. 10-1219

DAVID J. KAPPOS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR, UNITED STATES PATENT AND TRADEMARK OFFICE, PETITIONER

v.

GILBERT P. HYATT

ON WRIT OF CERTIORARI TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

BRIEF FOR THE PETITIONER

OPINIONS BELOW

The opinion of the en banc court of appeals (Pet. App. 1a-80a) is reported at 625 F.3d 1320. The opinion of the court of appeals panel (Pet. App. 81a-172a) is reported at 576 F.3d 1246. The opinion of the district court (Pet. App. 173a-199a) is unreported. The order of the Board of Patent Appeals and Interferences (Pet. App. 200a-254a) is unreported.

JURISDICTION

The judgment of the court of appeals was entered on November 8, 2010. On January 26, 2011, the Chief Justice extended the time in which to file a petition for a

writ of certiorari to and including March 8, 2011. On February 25, 2011, the Chief Justice further extended the time to and including April 7, 2011, and the petition was filed on that date. The petition for a writ of certiorari was granted on June 27, 2011. The jurisdiction of this Court rests on 28 U.S.C. 1254(1).

STATUTORY PROVISION INVOLVED

Section 145 of Title 35 of the United States Code is reproduced in the appendix to the petition for a writ of certiorari (Pet. App. 280a).

STATEMENT

1. a. The United States Patent and Trademark Office (PTO) is "responsible for the granting and issuing of patents." 35 U.S.C. 2(a)(1). When an applicant seeks a patent, the PTO undertakes an examination process to determine whether a patent should issue. 35 U.S.C. 131. An examiner with expertise in the relevant technological fields analyzes the application and the invention it describes, as well as the prior art in the field, to determine whether the statutory requirements for patentability are satisfied. *Ibid.*; PTO, U.S. Dep't of Commerce, *Manual of Patent Examining Procedure* §§ 704-706, 903.08(e), 904-904.02 (8th ed. Rev. 8, July 2010).

A number of statutory prerequisites must be satisfied before a patent may issue. An invention must consist of patent-eligible subject matter, 35 U.S.C. 101, and it must be novel, 35 U.S.C. 102, and non-obvious, 35 U.S.C. 103(a). The patent's specification must contain a written description of the invention "and of the manner and process of making and using it," and it must enable a person of ordinary skill in the art to "make and use the same." 35 U.S.C. 112. In applying those requirements, the PTO may make a number of factual determinations

regarding, *inter alia*, the nature of the invention's advancement over existing technology, the level of ordinary skill in the art, and the way in which a person of ordinary skill would understand the patent's specification. See, *e.g.*, *Graham* v. *John Deere Co.*, 383 U.S. 1, 17 (1966).

If the examiner denies a patent application, the applicant may appeal the decision to the PTO's Board of Patent Appeals and Interferences (Board). See 35 U.S.C. 6 (2006 & Supp. III 2009); 35 U.S.C. 134. The Board is composed of "administrative patent judges" who possess "competent legal knowledge and scientific ability." 35 U.S.C. 6(a) (Supp. III 2009). An applicant who believes the Board's decision is erroneous may file a request for Board rehearing. 37 C.F.R. 41.52. Alternatively, an applicant who wishes to overcome the Board's decision by introducing new evidence of patentability before the PTO may file a request for continued examination, 37 C.F.R. 1.114, or a continuation application, 37 C.F.R. 1.53(b); see 35 U.S.C. 120. In either case, the examiner considers the application in light of the new evidence, and the applicant may appeal the examiner's decision to the Board.

b. An applicant aggrieved by the Board's final determination may obtain judicial review through either of two avenues. 35 U.S.C. 141-145. The applicant may directly "appeal the decision to the United States Court of Appeals for the Federal Circuit," 35 U.S.C. 141, which "review[s] the [Board's] decision * * * on the record before the [PTO]," 35 U.S.C. 144. In Section 141 proceedings, the Federal Circuit reviews the PTO's decision under the deferential standards that govern judicial review of final agency action under the Administrative

Procedure Act (APA), 5 U.S.C. 701 *et seq.* See *Dickinson* v. *Zurko*, 527 U.S. 150, 154-165 (1999).

Alternatively, an unsuccessful applicant may "have remedy by civil action against the Director" of the PTO in the District Court for the District of Columbia. 35 U.S.C. 145. In a Section 145 action, the "court may adjudge that such applicant is entitled to receive a patent for his invention, as specified in any of his claims involved in the decision of the [Board], as the facts in the case may appear." *Ibid.* This Court observed in *Zurko* that Section 145 sometimes "permits the disappointed applicant to present to the court evidence that the applicant did not present to the PTO," which "makes a factfinder of the district judge." *Zurko*, 527 U.S. at 164. Neither in *Zurko* nor in any other decision, however, has this Court addressed the circumstances in which evidence that was not presented to the PTO may be admitted in a Section 145 suit. See *ibid.*

c. Section 145 is the current embodiment of a statutory provision that has authorized judicial review of the decisions of the PTO (or its predecessor, the Patent Office) in district court since 1836, when Congress first created an agency responsible for the examination of patents. See Act of July 4, 1836 (Patent Act of 1836), ch. 357, § 16, 5 Stat. 123; see generally *Hoover Co.* v. *Coe*, 325 U.S. 79, 84-87 (1945). Eventually codified as Rev. Stat. § 4915 (1878) (R.S. 4915), the provision authorized disappointed patent applicants to file a "bill in equity" to obtain judicial review in "all cases where patents are refused for any reason whatever," Act of Mar. 3, 1839 (Patent Act of 1839), ch. 88, § 10, 5 Stat. 354, including both patent denials and priority determinations made after "interference" proceedings, see 35 U.S.C.

135.[1] Although Congress amended various aspects of R.S. 4915 during the 19th and early 20th centuries, the language defining the proceeding remained essentially unchanged, providing that an unsuccessful patent applicant may "have remedy" through an original action in which the court "may adjudge that such applicant is entitled, according to law, to receive a patent * * * as the facts in the case may appear." Patent Act of 1870, ch. 230, § 52, 16 Stat. 205; see Act of Mar. 2, 1927 (1927 Act), ch. 273, § 11, 44 Stat. 1336; Patent Act of 1836 § 16, 5 Stat. 123 (cited by the Patent Act of 1839 § 10, 5 Stat. 354). Each version of the statute provided that the court's decision in favor of the applicant "shall authorize the Commissioner to issue such patent." *Id.* § 16, 5 Stat. 124.

Originally, an unsuccessful patent applicant could file a bill in equity in district court under R.S. 4915 only after obtaining initial judicial review in the courts of the District of Columbia. See Rev. Stat. §§ 4911-4914 (1878); *Hoover Co.*, 325 U.S. at 85-86; Pet. App. 97a-101a. In 1927, Congress amended the statutory scheme to permit a disappointed applicant to "have the decision of the Patent Office reviewed either by the court of appeals or by filing a bill in equity, but not both." *Hoover Co.*, 325 U.S. at 87 (citation omitted); see 1927 Act § 8, 44 Stat. 1336. In the Patent Act of 1952, Congress divided R.S. 4915 into two sections: Section 145, governing ex parte proceedings, and Section 146, governing interferences. The Senate Report accompanying the relevant bill indicated that "no fundamental change" was in-

---

[1] A "bill in equity" was the initial pleading in proceedings invoking the equity jurisdiction of the courts, equivalent to the complaint in actions at law. See, *e.g.*, Benjamin J. Shipman, *Handbook of the Law of Equity Pleading* § 101, at 168 (1897).

tended "in the various appeals and other review of Patent Office action." S. Rep. No. 1979, 82d Cong., 2d Sess. 7 (1952) (*Senate Report*).

2. a. Respondent is the named inventor of the invention disclosed in the patent application at issue in this case, known as the '702 application. Pet. App. 3a. The invention relates generally to a computerized display system for processing image information. *Ibid.*

Respondent filed the '702 application in 1995. He asserted priority of invention dating back to 1975 through a chain of previous applications. Gov't C.A. Br. 2-3. After a series of amendments, he cancelled the original claims in the application and presented 117 new claims for examination. Pet. App. 83a; C.A. App. A11009-A11087; see J.A. 263-364. Concerned that the amendment was not supported by the original application, see 35 U.S.C. 132(a) (barring amendments introducing "new matter"), and thus did not comply with the written-description requirement, the PTO examiner directed respondent to "point out where in the specification support may be found" for the new claims. C.A. App. A10493; Pet. App. 85a; cf. 37 C.F.R. 1.105(a)(1). Respondent then submitted further amendments to the specification and a list of page ranges that purportedly contained support for the claims. Pet. App. 85a-86a. Respondent also referred the examiner to the specification's "Table of Contents (see the Preliminary Amendments) for additional antecedent basis." *Id.* at 86a. Finding respondent's submission insufficiently specific, the examiner rejected all 117 claims under 35 U.S.C. 112 for lack of an adequate written description. Pet. App. 4a; 86a-88a.

b. Respondent appealed to the Board. To demonstrate support for the claims in the specification, respon-

dent provided a table (Table-1) listing "representative terminology," the number of times each term appeared in the specification, and representative pages on which each term appeared. Pet. App. 89a-90a. For example, the table showed that the term "input" appeared more than 200 times "throughout" the 238-page specification. *Id.* at 89a.

Addressing respondent's submission, the Board observed that respondent's only effort to identify support in the specification for the rejected claims consisted of Table-1. See Pet. App. 213a, 218a-219a; see also *id.* at 260a. Stating that "merely pointing to isolated words scattered throughout the specification does not describe the invention claimed as a combination of elements, functions, and interconnections, any more than a dictionary provides written description support for a book where words are used in combination to provide a certain meaning," the Board concluded that respondent had failed to refute the examiner's findings under Section 112. *Id.* at 213a. The Board nevertheless conducted its own search of the specification for supporting disclosures. *Id.* at 219a-240a; see *id.* at 257a ("This panel spent three weeks considering the 238 page specification, the 42 drawing figures, the 128 page appeal brief, and the 64 page reply brief as applied to 54 independent claims and 63 dependent claims in writing our original decision."). The Board ultimately found adequate support for 38 claims, but affirmed the examiner's rejection of the other 79 claims for lack of written description.[2] *Id.* at 252a-253a.

---

[2] The Board reversed the examiner's rejections based on obviousness, anticipation, and other grounds not at issue here. Pet. App. 5a.

Respondent filed a request for rehearing before the Board and offered, for the first time, claim-by-claim responses to the examiner's written-description rejections. See Pet. App. 257a; J.A. 670-745. The Board denied reconsideration, explaining that, under PTO rules, respondent had forfeited his new written-description arguments by failing to present them in his briefing on appeal to the Board. Pet. App. 256a; see 37 C.F.R. 1.192(a) (2002) (arguments not presented to the Board in appeal briefs are waived); cf. 37 C.F.R. 41.37(c)(1)(vii) (same).

3. Respondent sought judicial review of the PTO's decision in district court under 35 U.S.C. 145. Pet. App. 6a. The Director moved for summary judgment, arguing that the Board's findings on the written-description issue were supported by substantial evidence in the record. *Ibid.* Respondent then submitted his own written declaration, in which he identified portions of the specification that, in his view, supported the claims held unpatentable by the Board. *Ibid.*; see *id.* at 261a-279a. The Director urged the district court not to consider the declaration because respondent had failed without reasonable excuse to provide the same information to the agency. *Id.* at 6a.

The district court excluded respondent's declaration, holding that Section 145 does not permit a plaintiff to introduce, for the first time in district court, evidence that he had a reasonable opportunity to present to the PTO during the administrative process. Pet. App. 173a-189a. Finding no basis in the administrative record for disturbing the Board's findings, the court granted summary judgment to the Director. *Id.* at 190a-199a.

4. A panel of the court of appeals affirmed. Pet. App. 81a-172a. The panel explained that Congress could not reasonably be thought to have intended "to allow a

patent applicant in a § 145 action to introduce new evidence with no regard whatsoever as to his conduct before the PTO." *Id.* at 146a. The panel emphasized that "it has been the general practice of federal courts for over eighty years in certain circumstances to exclude evidence which a party could and should have introduced before the Patent Office but did not despite an obligation to do so." *Id.* at 121a. Judge Moore dissented. *Id.* at 149a-172a.

5. a. The court of appeals granted rehearing en banc and vacated the district court's grant of summary judgment. Pet. App. 1a-80a. The en banc court held that Section 145 permits patent applicants to challenge the Board's determination based on any evidence admissible under the Federal Rules of Evidence, even if the applicant had no justification for failing to provide the evidence to the agency. *Id.* at 21a. The court stated that Section 145 "provides no indication that this civil action is somehow different from a customary civil action," *id.* at 11a-12a, and that "[w]here [a] statute permits a 'civil action' in relation to agency actions, the Supreme Court has held that this amounts to a trial de novo," *id.* at 30a (citing *Chandler* v. *Roudebush*, 425 U.S. 840 (1976)). The court also relied on testimony during congressional hearings preceding the 1927 revisions to the Patent Act, in which certain witnesses characterized R.S. 4915 as permitting a "de novo" proceeding in district court in which the administrative record could be supplemented by additional evidence. See Pet. App. 14a-17a. The court viewed that testimony as indicating that Congress understood R.S. 4915 to "allow[] an applicant to introduce new evidence in district court, regardless of whether that evidence had been provided to the Patent Office in earlier proceedings." *Id.* at 17a.

The court of appeals further held that "once an applicant introduces new evidence on an issue, the district court reviews that issue de novo," Pet. App. 2a, and makes "de novo fact findings if the evidence conflicts with any related [PTO] finding," *id.* at 32a. In the court's view, permitting de novo review when new evidence is introduced does not conflict with "principles of deference to agency fact finding" because a deferential "court/agency standard of review" applies when the applicant does not offer new evidence. *Id.* at 31a; see *id.* at 30a. The court also noted that a district court may consider "the proceedings before and findings of the Patent Office in deciding what weight to afford an applicant's newly-admitted evidence." *Id.* at 28a. The en banc court accordingly vacated the district court's grant of summary judgment to the PTO and remanded for further proceedings. *Id.* at 34a-35a.

b. Judge Newman concurred in part and dissented in part. Pet. App. 36a-43a. She agreed with the majority that Section 145 authorizes the admission of new evidence without regard to the applicant's conduct before the PTO. *Id.* at 38a. She would have held, however, that Section 145 authorizes de novo review even when the applicant does not introduce new evidence. *Ibid.*

c. Judge Dyk, joined by Judge Gajarsa, dissented. Pet. App. 44a-80a. The dissenting judges described the en banc court's decision as "a remarkable departure from settled principles of administrative law" and "yet another misguided effort to craft special rules for patent cases that the Supreme Court in other cases has held to be impermissible." *Id.* at 44a, 46a (citing *Zurko*, 527 U.S. at 152). They emphasized that courts historically had limited the admissibility of new evidence in Section 145 proceedings, and that Congress has often provided

for deferential review in civil actions brought in district court. *Id.* at 53a-78a. They would have held that Section 145 does not permit a disappointed patent applicant to introduce new evidence that could have been submitted to the PTO. *Id.* at 51a-52a. In the dissenting judges' view, "[t]he majority opinion invites applicants to deliberately withhold evidence from the PTO in favor of a more hospitable district court forum," *id.* at 46a, particularly "in those circumstances where an expert agency would reject the evidence but a non-expert district court might be convinced to accept it," *id.* at 80a.

SUMMARY OF ARGUMENT

Under Section 145, a patent applicant "dissatisfied with the decision" of the PTO may seek judicial review by filing a "civil action against the Director" in district court. 35 U.S.C. 145. If the plaintiff prevails in his challenge to the PTO's decision, the district court's "adjudication shall authorize the Director to issue [a] patent on compliance with the requirements of law." *Ibid.* More than a century ago, this Court held that actions under Section 145's statutory predecessor, R.S. 4915, involved judicial review of agency determinations. *Morgan* v. *Daniels*, 153 U.S. 120, 124 (1894). That new evidence is sometimes admissible in Section 145 actions reflects a limited departure from ordinary on-the-record review of agency action, but it does not alter the fundamental nature of the proceeding as one to "set aside" the PTO's decision. *Ibid.*

The extent to which new evidence is admissible in a Section 145 suit, and the standard of review under which the PTO's decision is evaluated, therefore should be determined in light of the background principles that govern judicial review of agency action. The established

general rule that a litigant must exhaust administrative remedies counsels that Section 145 should be construed to permit the introduction of new evidence only when a disappointed patent applicant had no reasonable opportunity to present that evidence to the PTO. Permitting applicants to withhold available evidence from the PTO in order to present it to a reviewing court would deprive the agency of the opportunity to apply its specialized expertise to the full body of relevant information, and it would deprive the court of the benefit of the agency's judgment. When new evidence is admitted, the court should apply the same deferential standard that otherwise governs review of the PTO's conclusions, but the court may accord greater weight to evidence that the PTO did not consider. Cf. *Microsoft Corp.* v. *i4i Ltd. P'ship*, 131 S. Ct. 2238 (2011) (*Microsoft*).

This construction of Section 145 finds support in the judicial understanding of R.S. 4915 that prevailed when Congress reenacted the provision in the Patent Act of 1952. In establishing the administrative-review character of R.S. 4915, the Court in *Morgan* described the proceeding as "something in the nature of a suit to set aside a judgment." 153 U.S. at 124. That analogy is revealing, since a nineteenth-century court presented with an equitable proceeding to attack a prior judgment would not have considered evidence that could have been produced during the earlier proceeding, and it would not have overturned the prior judgment absent compelling proof of error. See *Beard* v. *Burts*, 95 U.S. 434, 436 (1877). Early twentieth-century courts regularly excluded evidence that could have been presented to the PTO, and they applied a deferential standard of review even when new evidence was admitted. Congress's 1952 reenactment of R.S. 4915 without material alterations should

therefore be understood to adopt the settled judicial practice.

This interpretation of Section 145 comports with generally-applicable principles of administrative law, and it produces an appropriate symmetry between judicial review of patent grants and review of patent denials. Limiting the admission of new evidence in Section 145 cases simply requires patent applicants to abide by the same exhaustion principles that govern parties who appear before other federal agencies. In *Microsoft*, the Court held that the presumption of validity that attaches to a granted patent can be overcome only by clear and convincing evidence, even when the party contesting the patent submits evidence that was not before the PTO. 131 S. Ct. at 2251. The Court explained that, although "new evidence supporting an invalidity defense may 'carry more weight' in an infringement action than evidence previously considered by the PTO," the standard of proof remains the same. *Ibid.* Because a challenge to the PTO's denial of a patent is "closely" related to a challenge to the validity of a granted patent, *Morgan*, 153 U.S. at 123, a Section 145 court's review of evidence not considered by the PTO should be governed by the same principles.

ARGUMENT

I. CONSISTENT WITH ESTABLISHED PRINCIPLES OF ADMINISTRATIVE LAW, 35 U.S.C. 145 IS PROPERLY CONSTRUED TO LIMIT EVIDENCE NOT PRESENTED TO THE PTO AND PROVIDE FOR DEFERENTIAL REVIEW

A. A Section 145 Suit Is A Proceeding For Judicial Review That Is Governed By Traditional Administrative-Law Principles

Under Section 145, a patent applicant "dissatisfied with the decision of the Board of Patent Appeals and Interferences * * * may * * * have remedy by civil action" against the Director of the PTO in the District Court for the District of Columbia, and the court "may adjudge that such applicant is entitled to receive a patent * * * as the facts of the case may appear." 35 U.S.C. 145. This Court has recognized that, unlike in appeals under Section 141, evidence outside the administrative record sometimes may be introduced in Section 145 proceedings. That limited deviation from usual administrative-law principles, however, does not change the fundamental character of a Section 145 proceeding as a suit for judicial review of agency action, and it does not justify wholesale abandonment of the background rules that govern admissibility of new evidence and the appropriate standard of review.

1. Section 145 authorizes judicial review of the PTO's decision

Contrary to respondent's contention, a proceeding under Section 145 is an action for judicial review of the PTO's denial of a patent, rather than a freestanding

"civil action *to obtain a patent*" (Br. in Opp. 12) from the district court.

a. Congress has authorized the PTO to decide whether to grant or deny a patent. See 35 U.S.C. 2(a) (The PTO is "responsible for the granting and issuing of patents."); *Graham* v. *John Deere Co.*, 383 U.S. 1, 18 (1966). When the PTO denies a patent, Chapter 13 of the Patent Act of 1952, entitled "Review of Patent and Trademark Office Decisions," provides the disappointed applicant two potential avenues by which to challenge the PTO's decision. The applicant may pursue a direct appeal under Section 141, in which the Federal Circuit reviews the patent denial in accordance with the APA. Alternatively, the applicant may file a civil action under Section 145. See generally *Dickinson* v. *Zurko*, 527 U.S. 150, 154-165 (1999); *Hoover Co.* v. *Coe*, 325 U.S. 79, 83 (1945) ("It is evident that alternative rights of review are accorded an applicant.").

Like Section 141, Section 145 applies to a patent applicant who is "dissatisfied with the decision" of the PTO, and it permits the applicant to seek a "remedy by civil action against the Director." 35 U.S.C. 145. A Section 145 action thus challenges the PTO's decision to deny a patent, and the potential "remedy" (if the plaintiff prevails) is a district court determination that "such applicant is entitled to receive a patent." *Ibid.* In adjudicating the action, the court is limited to the "correction of erroneous adverse rulings" contained within the PTO's rejection, such that "the effect of adjudication * * * [is] the same as that of decision on appeal." *Hoover Co.*, 325 U.S. at 87-88.

Section 145 does not authorize the court to issue the patent itself, or even to "direct the issuance of a patent." *Gould* v. *Quigg*, 822 F.2d 1074, 1079 (Fed. Cir. 1987).

Rather, if the district court "adjudge[s] that [the] applicant is entitled to receive a patent for his invention," the court's "adjudication shall authorize the Director to issue such patent on compliance with the requirements of law." 35 U.S.C. 145. A decision in favor of the plaintiff in a Section 145 action thus has the effect of a remand, returning the application to the PTO to determine in the first instance whether the patent should issue, or whether there is some other ground on which the patent should be denied. See *Hoover Co.*, 325 U.S. at 89 ("where an applicant has succeeded in a bill filed under R.S. 4915, the courts have not questioned the power of the Patent Office subsequently to disallow the claims" for other reasons); *In re Gould*, 673 F.2d 1385, 1386 (C.C.P.A. 1982) (per curiam); *In re Fisher*, 448 F.2d 1406, 1407 (C.C.P.A. 1971) (per curiam) (In a Section 145 action, "our mandates amount to remands."). The court's role is thus to review the PTO's conclusions and to set them aside if they are erroneous, rather than to determine in the first instance whether a patent should issue.

b. In *Morgan* v. *Daniels*, 153 U.S. 120 (1894), this Court characterized an R.S. 4915 action as "an application to the court to set aside the action of one of the executive departments of the government." *Id.* at 124. The Court explained that, because the decision to deny a patent or award priority is made by "[t]he one charged with the administration of the patent system" after "finish[ing] its investigations and ma[king] its determination," *ibid.*, the agency's determination should be overturned only if its error "is established by testimony which in character and amount carries thorough conviction." *Id.* at 125. When the evidence is "doubtful[,] the decision of the Patent Office must control." *Ibid.* The

Court thus has long viewed the proceeding established in R.S. 4915 and reenacted in Section 145 as a suit for judicial review of agency action.

The court of appeals discounted *Morgan* as simply "a case about what standard of review ought to apply when the district court decides whether an applicant is entitled to a patent on exactly the same record that was before the Patent Office." Pet. App. 23a; see Br. in Opp. 18. But the *Morgan* Court did not announce any such limits on its description of R.S. 4915 as authorizing an action "in the nature of a suit to set aside a judgment." 153 U.S. at 124. The *Morgan* plaintiff's failure to proffer new evidence in federal court "make[s] no appearance" in the Court's discussion of the nature of judicial proceedings under R.S. 4915. *Microsoft Corp.* v. *i4i Ltd. P'ship*, 131 S. Ct. 2238, 2247-2248 (2011) (rejecting a similar attempt to read "unstated limitations" into this Court's precedents regarding deferential review of administrative patent determinations). Instead, the Court's characterization of R.S. 4915 as "something in the nature of a suit to set aside a judgment," *Morgan*, 153 U.S. at 124, and the Court's associated endorsement of a deferential standard of judicial review, were offered "without qualification." *Microsoft*, 131 S. Ct. at 2247.

In any event, there is no sound logical basis for the distinction the court of appeals drew. *Morgan* makes clear that Section 145 functions as a judicial-review provision ("an application to the court to set aside the action of one of the executive departments of the government," 153 U.S. at 124) when the plaintiff does not introduce new evidence. When a Section 145 plaintiff is permitted to introduce new evidence in court (see pp. 44-45, *infra*), the plaintiff's prior inability to present the materials to the PTO may affect the *weight*

the evidence should be given, but it cannot alter the fundamental character of the proceeding as one for judicial review of agency action. Whether or not new evidence is introduced, the ultimate question for the court in a Section 145 suit is whether the PTO's decision should stand. Cf. *Microsoft*, 131 S. Ct. at 2251 (recognizing that a challenge to the validity of a granted patent attacks the PTO's "considered judgment" even when the challenge is based on evidence not considered by the agency).

2. Traditional administrative-law principles govern the admissibility of new evidence and the standard of review in Section 145 proceedings

The express statutory requirement that review in a Section 141 appeal be "on the record before the [PTO]," 35 U.S.C. 144, combined with the absence of similar language in Section 145, indicates that Section 145 plaintiffs are not wholly foreclosed from introducing evidence that was not before the agency. The Court in *Zurko* accordingly observed that Section 145 "permits the disappointed applicant to present to the court evidence that the applicant did not present to the PTO." 527 U.S. at 164. Neither Section 145 nor any adjacent Patent Act provision, however, addresses the *circumstances* under which new evidence should be admissible, or the standard of review the court should apply in determining whether the PTO's decision should be set aside. "[W]here Congress has simply provided for review, without setting forth the standards to be used or the procedures to be followed," review is governed by established background principles that reflect deference to agency authority and expertise. *United States* v. *Carlo Bianchi & Co.*, 373 U.S. 709, 715 (1963); *Consolo* v. *Fed-*

eral Mar. Comm'n, 383 U.S. 607, 619 n.17 (1966) ("[I]n the absence of specific statutory authorization, a *de novo* review is generally not to be presumed.").[3]

Respondent suggests (Br. in Opp. 14-15) that, if Section 145 is construed to incorporate background administrative-law principles, Congress's creation of alternative modes of judicial review (see 35 U.S.C. 141, 145) will somehow be subverted. That argument lacks merit. The approach advocated by the government and by the dissenters below, under which the plaintiff in a Section 145 action may introduce evidence that he had no reasonable opportunity to present to the PTO, preserves distinct roles for Sections 141 and 145 while respecting usual rules of agency exhaustion. See pp. 42-44, *infra*.

Respondent also argues (Br. in Opp. 11-13) that Section 145's use of the term "civil action" reflects Congress's intent to authorize "*de novo* proceeding[s]." But neither Congress's use of that terminology, nor its decision to entrust judicial review to the district court in the

---

[3] In contrast to Section 145, some federal statutes expressly authorize a court to conduct de novo review of agency action. See, *e.g.*, 18 U.S.C. 923(f)(3) (revocation of firearms licenses) (authorizing "de novo judicial review" and providing that "the court may consider any evidence submitted by the parties to the proceeding whether or not such evidence was considered at the [administrative] hearing"); 7 U.S.C. 2023(a)(15) (Food Stamp Act of 1977) (stipulating that the suit "shall be a trial de novo by the court"); 5 U.S.C. 552(a)(4)(B) (Freedom of Information Act) (the district court "shall determine the matter de novo"); 41 U.S.C. 609(a)(3) (Contract Disputes Act of 1978) (suits for breach of contract "shall proceed de novo in accordance with the rules of the appropriate court"); cf. 28 U.S.C. 2640(a) (customs matters) (instructing that the Court of International Trade "shall make its determinations on the basis of the record made before the court" in specified types of civil actions).

first instance, renders ordinary principles of administrative law inapplicable. This Court has recognized that "the function of reviewing an administrative decision can be and frequently is performed by a court of original jurisdiction as well as by an appellate tribunal." *Carlo Bianchi & Co.*, 373 U.S. at 715. And denominating the proceeding a "civil action" implies nothing about the contours of the proceeding, for *all* civil proceedings in district court are civil actions. See Fed. R. Civ. P. 2 ("There is one form of action—the civil action."); cf. *Cabinet Mountains Wilderness* v. *Peterson*, 685 F.2d 678, 685 & n.3 (D.C. Cir. 1982) (explaining that the Endangered Species Act of 1973's citizen-suit provision, which authorizes a plaintiff to "commence a civil suit on his own behalf," "merely provides a right of action to challenge the agency action alleged to be" unlawful and "does not direct trial courts to conduct *de novo* review in such actions") (quoting 16 U.S.C. 1540(g)(1) (1976)). APA suits to set aside final agency action (see 5 U.S.C. 702, 706) are "civil action[s]" brought in district court, yet they are governed by traditional administrative-law principles.

The court of appeals read *Chandler* v. *Roudebush*, 425 U.S. 840 (1976), to hold that "[w]here the statute permits a 'civil action' in relation to agency actions, * * * this amounts to a trial de novo" in which "the admission of new evidence" is "subject only to the Federal Rules of Evidence and Civil Procedure." Pet. App. 30a. The court's reliance on *Chandler* was misplaced. This Court in *Chandler* held that Title VII of the Civil Rights Act of 1964, 42 U.S.C. 2000e *et seq.*, conferred on federal employees the right to "trials *de novo*" on their discrimination claims, rather than simply to "'substantial evidence' review" of "administrative dispositions of federal

employee discrimination complaints." 425 U.S. at 863. As the dissent below explained, however, the Court did not base that conclusion on the statute's use of the term "civil action" standing alone. Rather, the Court relied on Title VII's structure: the statute gave federal workers the *same* right as private-sector employees to file suit alleging unlawful employment discrimination, and private-sector employees had an unquestioned right to trial de novo. See *id.* at 844-846, 863; Pet. App. 59a-60a (distinguishing *Chandler*). The PTO's disposition of patent applications, by contrast, has no private-sector analogue, and no structural feature of the Patent Act suggests congressional intent to depart from administrative-review principles.

B. Evidence That Reasonably Could Have Been Presented To The PTO Should Not Be Admissible In Section 145 Suits, And The PTO's Decision Should Be Reviewed Deferentially In All Cases

For the reasons set forth above, Section 145 provides a mechanism for judicial review of agency action, and it should accordingly be construed to incorporate traditional administrative-law principles. Two such principles—the rule that reviewing courts will ordinarily consider only evidence that was first presented to the agency, and the requirement of judicial deference to agency authority and expertise—are directly relevant here.

1. Permitting introduction of new evidence that could have been presented to the agency conflicts with administrative-exhaustion principles

a. An applicant before an agency ordinarily must present his arguments and evidence to the agency, thereby affording it a full opportunity to apply its judg-

ment and expertise to the issues at hand, before seeking judicial review of the agency's decision. *McKart* v. *United States*, 395 U.S. 185, 193 (1969); see *Citizens to Preserve Overton Park, Inc.* v. *Volpe*, 401 U.S. 402, 413-414 (1971). Judicial review then takes place using the existing administrative record. When material evidence that was previously unavailable is brought to the court's attention, the proper course is usually "to remand to the agency for additional investigation or explanation." *Florida Power & Light Co.* v. *Lorion*, 470 U.S. 729, 744 (1985); see *Tagg Bros. & Moorhead* v. *United States*, 280 U.S. 420, 444-445 (1930) (*Tagg Bros.*).

The requirement of administrative exhaustion permits the agency to "develop the necessary factual background upon which decisions should be based" and gives the agency the opportunity to "apply[] a statute in the first instance." *McKart*, 395 U.S. at 193-194; see *McCarthy* v. *Madigan*, 503 U.S. 140, 145 (1992) (Exhaustion concerns have "particular force * * * when the agency proceedings in question allow the agency to apply its special expertise."). The exhaustion requirement also ensures that the agency is "given a chance to discover and correct its own errors" and prevents "frequent and deliberate flouting of administrative processes."[4] *McKart*, 395 U.S. at 195.

---

[4] Respondent contends (Br. in Opp. 23) that exhaustion principles may not "be invoked to bar the introduction of *new evidence* relevant to issues that were raised and decided by the agency." To the contrary, the Court has emphasized that exhaustion principles are particularly important in the context of evidence not presented to the agency, because proffering new evidence to a reviewing court deprives the agency of the opportunity to make its decision based on a full record and threatens to "substitute the court for the administrative tribunal as the [policy-]making body." *Tagg Bros.*, 280 U.S. at 444; see *McKart*, 395 U.S. at 198 n.15 ("[T]he present case does not present an instance

These rationales are not rendered inapposite simply because Section 145 does not preclude the introduction of new evidence in all circumstances. Section 145 provides a safety valve in situations where a disappointed patent applicant had no reasonable opportunity to present particular relevant evidence to the PTO. With respect to evidence that *could* have been submitted to the agency, however, the reasons for treating exhaustion as a prerequisite to consideration of the evidence by a reviewing court apply with full force. Withholding evidence that could be presented to the PTO deprives the agency of the opportunity to apply its specialized expertise to the full body of evidence, and it deprives the court of the benefit of the agency's judgment.

b. The court of appeals disregarded these principles by creating a regime in which a patent applicant may purposefully withhold existing evidence from the PTO in order to present that evidence to a non-expert judge. The court's decision also allows the applicant, after the PTO has rendered its decision, to produce and present to the court new evidence (such as respondent's declaration in this case) that could have been assembled earlier. Allowing the court to consider such evidence in the first instance flouts established rules of exhaustion and undermines Congress's decision to entrust the issuance of patents to an expert agency. See *Carlo Bianchi & Co.*, 373 U.S. at 717 (Congress's purpose "would be frustrated if either side were free to withhold evidence at the administrative level and then introduce it in a judicial proceeding.").

---

where a registrant is trying to challenge [an agency decision] on the basis of facts not presented to the local board. In such a case, the smooth functioning of the system may well require that [such challenges] be barred.").

The regime created by the court of appeals also hinders the PTO's effectiveness by excusing violations of the agency's rules of practice. "Proper exhaustion demands compliance with any deadlines and other critical procedural rules because no adjudicative system can function effectively without imposing some orderly structure on the course of its proceedings." *Woodford* v. *Ngo*, 548 U.S. 81, 90-91 (2006). The PTO's rules allow applicants to submit new evidence in response to an examiner's rejection, see 37 C.F.R. 41.33(d)(1), but they also provide that arguments not timely presented to the Board are forfeited, see 37 C.F.R. 41.37(c)(1)(vii), and they limit the circumstances in which new evidence may be submitted after an appeal has been taken, see 37 C.F.R. 41.33(d)(1); see also 37 C.F.R. 41.39(b)(1), 41.50(a)(2)(i) and (b)(1). An applicant who has received an adverse Board decision may also submit new evidence to the PTO by filing a request for continued examination or a continuation application. See 37 C.F.R. 1.53(b), 1.114. Those procedures afford applicants various opportunities to present evidence that becomes available as the administrative process unfolds, but they also facilitate the PTO's orderly administration of its examination process by imposing limitations on the time and manner of presentation. By mandating district-court consideration of evidence that an applicant failed without cause to present to the agency in a timely fashion, the court of appeals' decision undermines the PTO's control of its own proceedings.

2. *Permitting de novo review of issues involving new evidence conflicts with longstanding principles of deference to agency authority and expertise*

a. A court reviewing an agency's decision "is not generally empowered to conduct a *de novo* inquiry into the matter being reviewed and to reach its own conclusions based on such an inquiry." *Lorion*, 470 U.S. at 744; see *INS* v. *Orlando Ventura*, 537 U.S. 12, 16 (2002) (per curiam). Rather, agency factual findings, made within the agency's sphere of delegated authority and expertise, are subject only to deferential review. See, *e.g.*, 5 U.S.C. 706; *Interstate Commerce Comm'n* v. *Union Pacific R.R.*, 222 U.S. 541, 548 (1912). Such review "frees the reviewing courts of the time-consuming and difficult task of weighing the evidence, * * * gives proper respect to the expertise of the administrative tribunal and * * * helps promote the uniform application of the statute." *Consolo*, 383 U.S. at 620-621.

Those rationales apply with full force to review of the PTO's decision whether to issue a patent. See *Zurko*, 527 U.S. at 160-162. In considering a patent application, a PTO examiner with specialized expertise in the relevant scientific or technical fields must analyze the application and relevant material, and "must make various factual determinations" based on a technical evaluation of the invention and knowledge of the state of the art in the relevant fields. *Microsoft*, 131 S. Ct. at 2242. The PTO's decision to deny a patent reflects the conclusion of both the examiner and a Board panel of expert patent judges that the application does not satisfy the Patent Act's requirements. Those determinations should not be overturned by a generalist district judge absent a clear demonstration that the PTO was wrong. See *Morgan*,

153 U.S. at 125 (when the evidence is "doubtful[,] the decision of the Patent Office must control").

The justifications for deferential review continue to be relevant even when a Section 145 plaintiff challenges the PTO's decision based on evidence that the PTO did not consider. Respondent argues that in such cases, "there is no prior decision on that record for the district court to review." Br. in Opp. 29. But even when the plaintiff's challenge rests on new evidence, the PTO *has* made a decision within its delegated authority on the ultimate question of patentability, and it has applied its expertise to the evidence before it. The presence of new evidence alone therefore does not justify discarding the bedrock principle that a court should not overturn the agency's decision without a high degree of confidence that the agency erred. See *Orlando Ventura*, 537 U.S. at 16; *Morgan*, 153 U.S. at 124.

This Court's decision in *Microsoft* demonstrates that, even when a disappointed patent applicant establishes a satisfactory reason for presenting to the district court evidence that was not before the PTO, the court's review should still reflect appropriate deference to the agency's authority and expertise. 131 S. Ct. at 2250-2251. The Court in *Microsoft* held that a party challenging the validity of a patent in the context of an infringement suit must establish invalidity by clear and convincing evidence, even when it relies on evidence of invalidity that was not before the PTO when it granted the patent. *Id.* at 2444-2451. The Court observed that the presumption of validity of a granted patent, 35 U.S.C. 282, is grounded in "the basic proposition that a government agency * * * was presumed to do its job," *Microsoft*, 131 S. Ct. at 2243 (quoting *American Hoist & Derrick Co.* v. *Sowa & Sons, Inc.*, 725 F.2d 1350, 1359 (Fed.

Cir.), cert. denied, 469 U.S. 821 (1984) (*American Hoist*)). The Court acknowledged that, when an invalidity challenge is based on new evidence, the PTO's "considered judgment may lose significant force" because "the PTO did not have all material facts before it." *Id.* at 2251. Rather than lowering the standard of proof when new evidence is admitted, however, the Court held that the standard should remain the same in all actions, but that "new evidence supporting an invalidity defense may 'carry more weight.'" *Ibid.* (quoting *American Hoist*, 725 F.2d at 1360).

The same principles should apply when a Section 145 plaintiff presents new evidence that it had no opportunity to submit to the PTO. This Court has long recognized that challenges to patent grants and denials are "closely" related. See *Morgan*, 153 U.S. at 123; see also *Radio Corp. of Am.* v. *Radio Eng'g Labs., Inc.*, 293 U.S. 1, 9 (1934) (*RCA*). Both are in substance attacks on the PTO's disposition of a patent application, see *Morgan*, 153 U.S. at 124, and both require the court to review the "various factual determinations" made by PTO examiners with expertise in the relevant fields, *Microsoft*, 131 S. Ct. at 2242. Just as it is possible to accommodate administrative-deference concerns while accounting for new evidence in the invalidity context, it is possible to do so in Section 145 actions. See pp. 44-46, *infra*; *Morgan*, 153 U.S. at 124-125; *RCA*, 293 U.S. at 7-9.

b. The court of appeals held that, whenever a Section 145 plaintiff introduces new evidence, the district court should "make de novo fact findings with respect to factual issues to which the new evidence relates." Pet. App. 31a. Because questions of patentability are either heavily reliant on factual components or are treated as "entirely factual," see *id.* at 47a (Dyk, J., dissenting),

that approach permits the district court to substitute its judgment for that of the PTO not only on subsidiary factual issues where the new "evidence conflicts with any related Patent Office finding," *id.* at 32a, but also on ultimate questions of patentability such as anticipation or the adequacy of the written description, both of which the Federal Circuit treats as questions of fact. See *Cordis Corp.* v. *Boston Scientific Corp.*, 561 F.3d 1319, 1331-1332, 1335 (Fed. Cir.), cert. denied, 130 S. Ct. 748, and 130 S. Ct. 749 (2009). The Federal Circuit's approach thus allows disappointed patent applicants to treat the expert agency's decision as a mere "tryout on the road" rather than as the "main event." Cf. *Wainwright* v. *Sykes*, 433 U.S. 72, 90 (1977).

Combined with this Court's decision in *Microsoft*, moreover, the court of appeals' interpretation of Section 145 creates an irrational asymmetry between judicial review of patent grants and review of patent denials. Under the Federal Circuit's decision, factual determinations underlying the PTO's denial of a patent receive no deference whenever new evidence is introduced, even though (under *Microsoft*) factual determinations underlying the grant of a patent receive deference even when the challenger presents new evidence of invalidity. That inconsistency is especially unjustifiable because a party challenging a granted patent often will have had no opportunity to present evidence of invalidity to the PTO, see *Microsoft*, 131 S. Ct. at 2251-2252, while an unsuccessful patent applicant who brings a Section 145 action will generally have had the opportunity (indeed, multiple opportunities) to present evidence of patentability to the agency examiner.

The court of appeals adopted a two-tiered approach, in which the district court in a Section 145 suit should

apply de novo review only "[w]hen new evidence is introduced," and should apply the deferential APA standard "when no party introduces new evidence." Pet. App. 31a-32a. Although that aspect of the court's decision might reduce the sheer number of Section 145 cases in which a de novo standard applies, it exacerbates the ill effects of the court's erroneous determination that the plaintiff may introduce new evidence without limitation. By holding that a more plaintiff-friendly standard of review applies when the plaintiff introduces evidence for the first time in district court, even when the plaintiff had a reasonable opportunity to present the relevant information to the agency, the court of appeals created an affirmative incentive for patent applicants to withhold relevant evidence from the PTO, or to create new evidence later, in order to improve their chances of success in court. This case illustrates the point, as the result of the court of appeals' approach is that respondent may obtain de novo review of the PTO's conclusions on the written description requirement simply by proffering a declaration containing arguments that respondent could have presented to the PTO.

As the court of appeals (Pet. App. 33a) and respondent (Br. in Opp. 26) have observed, certain countervailing incentives—*e.g.*, the applicant's desire to maximize his chances of success in the agency proceedings, and the added expense associated with Section 145 actions—may encourage applicants to present all their evidence to the PTO and thereby mitigate the practical impact of the court's decision. But the existence of such incentives does not distinguish disappointed patent applicants from plaintiffs who challenge other types of agency action. Such plaintiffs likewise have an interest in prevailing before the agency and thereby avoiding the expense of

a lawsuit, but those incentives have never been thought to be sufficient to eliminate the need for rules regarding exhaustion and timely presentation of evidence. In any event, a rule that rewards applicants for withholding evidence from the agency does substantial harm to the patent system even if it does not affect every applicant's behavior. The Federal Circuit's approach would create the strongest incentive to "bypass the PTO" in those "cases where the patent is commercially significant and the costs of a separate proceeding can be justified"—yet those are the cases in which "PTO review is most important." Pet. App. 79a-80a (Dyk, J., dissenting).

II. CONGRESS'S REENACTMENT OF SECTION 145 IN THE PATENT ACT OF 1952 SHOULD BE UNDERSTOOD TO INCORPORATE THE PREVAILING JUDICIAL PRACTICE OF LIMITING THE INTRODUCTION OF NEW EVIDENCE AND APPLYING A DEFERENTIAL STANDARD OF REVIEW

This Court in *Morgan* made clear that suits brought under R.S. 4915 were proceedings for judicial review of agency action. Consistent with that understanding, early twentieth century courts regularly excluded evidence that plaintiffs had failed without cause to present to the PTO, and they applied a deferential standard of review even when new evidence was admitted. When Congress recodified R.S. 4915 as Section 145, "mak[ing] no fundamental change in the various appeals and other review of Patent Office action," *Senate Report* 7, it adopted that settled judicial practice.

A. This Court's Analysis Of R.S. 4915 In *Morgan* Supports Limitations On New Evidence And Deferential Review Of The PTO's Factfindings

1. As discussed above, this Court recognized in *Morgan* that the "bill in equity" authorized under R.S. 4915 was "something more than a mere appeal." 153 U.S. at 124. An R.S. 4915 suit was "an application to the court to set aside the action of one of the executive departments of the government," made in the exercise of its delegated authority and expert judgment. *Ibid.* A judicial proceeding to overturn such a determination, the Court explained, "is something in the nature of a suit to set aside a judgment, and as such is not to be sustained by a mere preponderance of evidence." *Ibid.* Rather, any error in the agency's decision must be established "by testimony which in character and amount carries thorough conviction." *Id.* at 125.

The *Morgan* Court's characterization of equity proceedings under R.S. 4915 as "something in the nature of a suit to set aside a judgment," 153 U.S. at 124, is telling. Under the principles of federal equity practice that prevailed at the time, a suit to set aside a judgment was brought as a "bill of review" or as an "original bill in the nature of a bill of review."[5] A district court presented with such a bill would not rehear arguments or evidence that had been adjudicated in the prior proceeding, nor would it consider new evidence that could have been

---

[5] The "bill of review" and "original bill in the nature of a bill of review" were particular types of "bill[s] in equity"—the equity proceeding authorized by R.S. 4915. See, *e.g.*, *Barrett* v. *Failing*, 111 U.S. 523, 528 (1884) (referring to "a bill in equity * * * in the nature of a bill of review for newly discovered evidence"); Benjamin J. Shipman, *Handbook of the Law of Equity Pleading* §§ 207-208, at 303 (1897); *id.* §§ 215-220, at 309-315.

produced during that proceeding in the exercise of reasonable diligence. In *Beard* v. *Burts*, 95 U.S. 434 (1877), for example, the Court noted "the general rule in equity" that "[t]he facts are not open for a re-trial [under a bill of review], unless the bill asserts that new evidence has been discovered, not obtainable before the first trial by the exercise of reasonable diligence." *Id.* at 436; see *Scotten* v. *Littlefield*, 235 U.S. 407, 411 (1914); 2 Thomas Atkins Street, *Federal Equity Practice* § 2119, at 1256 (1909) (*Federal Equity Practice*); *id.* § 2150, at 1272; Benjamin J. Shipman, *Handbook of the Law of Equity Pleading* §§ 215-220, at 309-315 (1897). In addition, a bill of review could not be obtained unless the new evidence clearly established the claimant's right to relief. See *Southard* v. *Russell*, 57 U.S. (16 How.) 547, 567, 569 (1854) (new evidence must be "decided and controlling" on the disputed questions); *Federal Equity Practice* § 2151, at 1272 (To obtain leave to file a bill of review, new evidence "must be so controlling in its effect" as to "probably induce a different conclusion" on the merits.). In characterizing a bill in equity under R.S. 4915 as "something in the nature of a suit to set aside a judgment," the Court in *Morgan*, 153 U.S. at 124, thus embraced a conception of the statute that is fundamentally inconsistent with the Federal Circuit's.[6]

---

[6] The court of appeals dismissed the significance of the *Morgan* Court's analogy on the ground that the bill authorized under R.S. 4915 was not a bill of review in the technical sense, since it was not a mechanism by which a court could "reverse its own decree." See Pet. App. 27a. The point of the analogy, however, was that, like a suit to set aside a court's own prior judgment, the bill in equity authorized by R.S. 4915 was a mechanism to attack a governmental decision that had already been made. See *Morgan*, 153 U.S. at 124 (explaining that a suit under R.S. 4915 is "a proceeding to set aside the conclusions reached by the administrative department").

2. The Federal Circuit relied on this Court's decision in *Butterworth* v. *United States*, 112 U.S. 50 (1884), as well as later decisions citing *Butterworth*, which the court viewed as establishing that new evidence was admissible without limitation in R.S. 4915 proceedings. See Pet. App. 23a-24a; Br. in Opp. 16. In *Butterworth*, the Court stated in dicta that an R.S. 4915 proceeding was "heard upon all competent evidence adduced and upon the whole merits." 112 U.S. at 61 (citing, *e.g.*, *In re Squire*, 22 F. Cas. 1015, 1016 (C.C.E.D. Mo. 1877) (No. 13,269)). Contrary to the court of appeals' view, however, *Butterworth* and the subsequent decisions on which the Federal Circuit relied, see Pet. App. 25a, 41a (citing *Hoover Co.*, 325 U.S. at 83, and *In re Hien*, 166 U.S. 432, 439 (1897)), shed no light on the extent to which new evidence was admissible in R.S. 4915 proceedings or on the standard of review that applied in such suits.

Rather, in stating that an R.S. 4915 action was not "confined to the case as made in the record of" the Patent Office, the decisions on which the court of appeals relied simply distinguished between a bill in equity under R.S. 4915 and a direct appeal under Rev. Stat. § 4911 (1878) (R.S. 4911) (Section 141's predecessor). *Butterworth*, 112 U.S. at 61 (describing R.S. 4915 proceeding and other review avenues in the course of determining the Secretary of the Interior's authority to overrule a Patent Office decision); *Hoover Co.*, 325 U.S. at 83 (holding that an R.S. 4915 action is a proceeding to review the PTO's decision, and citing *Butterworth* in observing that, unlike an appeal, an R.S. 4915 action "may include evidence not presented in the Patent Office"); *Hien*, 166 U.S. at 439 (noting the admissibility of new evidence in R.S. 4915 proceedings in order to "distin-

guish[] the proceeding by bill in equity under section 4915 from an appeal under section 4911"); *Gandy* v. *Marble*, 122 U.S. 432, 439 (1887) (holding that timeliness rule governing direct appeals applied to R.S. 4915, even though it "is not a technical appeal from the Patent Office, nor confined to the case as made in the record of that office"). But while those decisions made clear that the introduction of new evidence in Section 4915 proceedings was not *categorically* foreclosed, they did not suggest that the plaintiff could introduce such evidence after failing without cause to present it to the agency.

B. Under R.S. 4915, The Prevailing Judicial Practice Following *Morgan* Was To Exclude Evidence That The Plaintiff Had Failed Without Cause To Present To The PTO

1. In the years between *Morgan* and the enactment of the Patent Act of 1952, federal courts repeatedly held that plaintiffs in R.S. 4915 proceedings were not entitled to introduce evidence that they had failed without cause to present to the PTO. Although the courts used varying formulations to describe that rule, they consistently grounded it in the principle that an administrative agency should have the opportunity to make its decision on a complete record.

In *Boucher Inventions, Ltd.* v. *Sola Elec. Co.*, 131 F.2d 225, 227 (D.C. Cir. 1942), cert. denied, 318 U.S. 770 (1943), for example, the court stated that "[t]he practice, under Section 4915 as well as within the Patent Office itself, contemplates a full disclosure to that office, so far as is reasonably possible." The court explained that, "[w]hile the 4915 suit is de novo and permits introduction of evidence not presented to the Patent Office, it does not contemplate the suppression or the withholding

of evidence so readily available * * * or oversight of such glaring proportions." *Ibid.*; see *Schilling* v. *Schwitzer-Cummins Co.*, 142 F.2d 82, 84-85 (D.C. Cir. 1944).

Similarly in *Barrett Co.* v. *Koppers Co.*, 22 F.2d 395, 397 (3d Cir. 1927), the court excluded evidence that had been intentionally withheld from the Patent Office even though it was "wholly within [the plaintiffs'] possession and control at the interference proceeding." The court explained that "[t]he law has established Patent Office tribunals peculiarly qualified to try issues of priority of invention," and that withholding evidence from the agency in order to present it in an R.S. 4915 action "made it impossible for [the Patent Office] to render what they, the plaintiffs, now maintain is the right decision." *Ibid.*[7]

Subsequent decisions applied the *Barrett* standard while reaffirming that the rule served to protect the integrity of the Patent Office's administrative processes.[8]

---

[7] Relying on the *Barrett* court's statement that "plaintiffs in this action * * * are estopped to offer" the withheld evidence, 22 F.2d at 397, respondent contends (Br. in Opp. 21-22) that the court applied equitable estoppel rather than administrative-review principles. The court in *Barrett*, however, did not discuss or require a showing of the elements of equitable estoppel, such as prejudice to the opposing party. See 22 F.2d at 397; cf. *Ashwander* v. *TVA*, 297 U.S. 288, 323 (1936) (discussing equitable estoppel). Rather, the *Barrett* court grounded its exclusion of evidence on its view that permitting withholding would undermine the PTO's expertise and authority. See 22 F.2d at 397-398.

[8] The judicial consensus on this point was not unanimous. In *Minnesota Mining & Mfg. Co.* v. *Carborundum Co.*, 155 F.2d 746 (3d Cir. 1946), the court refused to exclude evidence that had been available to the plaintiffs at the time of the Patent Office proceeding, stating that to do so would "change the nature of an R.S. Section 4915 proceeding." *Id.* at 748. Despite that lack of uniformity, however, the prevailing practice

In *Globe-Union, Inc.* v. *Chicago Tel. Supply Co.*, 103 F.2d 722 (7th Cir. 1939) (*Globe-Union*), the court observed that "all pertinent evidence, actually available, should be submitted in the first instance," because "[t]o permit partial presentation before the Patent Office is to sanction the destruction of administrative justice." *Id.* at 728; see *Knutson* v. *Gallsworthy*, 164 F.2d 497, 508-509 (D.C. Cir. 1947) (stating that "[t]he rule is well settled that new and additional evidence may be received in a civil action under Section 4915, but it is equally well settled that a party may not successfully offer to the court evidence withheld from the Patent Office") (footnote omitted); *Greene* v. *Beidler*, 58 F.2d 207, 209-210 (2d Cir. 1932) (holding that district court erred in finding for plaintiff based on evidence not presented to the Patent Office); see also Pet. App. 74a-78a (Dyk, J., dissenting); *Schering Corp.* v. *Marzall*, 101 F. Supp. 571, 573 (D.D.C. 1951); *Etten* v. *Kauffman*, 32 F. Supp. 186, 187 (W.D. Pa. 1940), aff'd, 121 F.2d 137 (3d Cir. 1941); *O'Donnell* v. *United Shoe Mach. Corp.*, 2 F. Supp. 178, 181 (D. Mass. 1933); 2 Anthony William Deller, *Walker on Patents: Deller's Edition* § 214, at 971 (1937) (noting that an R.S. 4915 proceeding is "*de novo*," but "a party to an interference suit, who withheld certain evidence which was available to him, in the Patent Office proceedings, was not permitted to introduce such evidence in a subsequent suit under section 4915").

When courts admitted new evidence in R.S. 4915 proceedings, moreover, they applied *Morgan*'s deferential standard of review rather than reviewing the Patent Of-

---

was to exclude evidence that the plaintiff had failed without cause to present to the Patent Office.

fice's findings de novo.[9] In *Globe-Union*, the court held that, because new evidence relating to the date on which the patentee had reduced his invention to practice "casts a heavy shadow of suspicion" over the evidence on which the Patent Office had relied, the plaintiff had "overcome the interference-judgment by 'testimony which in character and amount carries thorough conviction.'" 103 F.2d at 729 (quoting *Morgan*, 153 U.S. at 125); see *Minnesota Mining & Mfg. Co.* v. *Carborundum Co.*, 155 F.2d 746, 748 (3d Cir. 1946) (citing *Morgan* and stating that "[t]he question therefore is whether all competent evidence, 'new' and 'old', offered to the District Court carries 'thorough conviction' that the Patent Office erred"); *Schilling*, 142 F.2d at 85; *Nichols* v. *Minnesota Mining & Mfg. Co.*, 109 F.2d 162, 163, 166 (4th Cir. 1940) (district court admitted new testimony and had experiments conducted under its direction, and "properly applied the rule of Morgan v. Daniels" to newly available evidence); *Dowling* v. *Jones*, 67 F.2d 537, 538-539 (2d Cir. 1933) (L. Hand, J.); *Gold* v. *Newton*, 254 F. 824, 828 (2d Cir. 1918), cert. denied, 249 U.S. 608 (1919).

---

[9] When no party objected to the admission of new evidence, courts considered that evidence in addition to the record before the PTO, applying *Morgan*'s "thorough conviction" standard of review to the record as a whole. See, *e.g.*, *Abbott* v. *Shepherd*, 135 F.2d 769, 774 (D.C. Cir. 1942); see also *S. & S. Corrugated Paper Mach. Co.* v. *George W. Swift, Jr., Inc.*, 176 F.2d 358, 360 (3d Cir. 1949) (noting "additional testimony," but stating that "we do not find any substantial difference" between the new evidence and the administrative record, and finding that new evidence did not create a "thorough conviction" that the Patent Office had erred) (citation omitted). In such cases, the courts had no occasion to address any limitations on the admissibility of evidence that had not been presented to the Patent Office.

C. When Congress Reenacted R.S. 4915 As Section 145, It Adopted The Prevailing Judicial Understanding Of R.S. 4915

1. In the Patent Act of 1952, Congress readopted without material change the provisions governing judicial review of Patent Office decisions, reenacting R.S. 4915 as Section 145. The reports accompanying the 1952 Act explained that the statute effected "no fundamental change in the various appeals and other review of Patent Office action." *Senate Report* 7. Because "Congress is presumed to be aware of an administrative or judicial interpretation of a statute and to adopt that interpretation when it re-enacts a statute without change," *Forest Grove Sch. Dist.* v. *T.A.*, 129 S. Ct. 2484, 2492 (2009) (quoting *Lorillard* v. *Pons*, 434 U.S. 575, 580 (1978)), Section 145 should be understood to incorporate the prevailing judicial view that admitting new evidence without limitation and engaging in de novo review would be inconsistent with administrative-law principles. See, *e.g.*, *California Research Corp.* v. *Ladd*, 356 F.2d 813, 821 n.18 (D.C. Cir. 1966) (interpreting Section 145 to establish a proceeding that "may not be conducted in disregard of the general policy of encouraging full disclosure to administrative tribunals"); see also *DeSeversky* v. *Brenner*, 424 F.2d 857, 858 n.5 (D.C. Cir. 1970) ("Although each side 'may strengthen its case with additional material' the plaintiff may not submit for the first time evidence which he was negligent in failing to submit to the Patent Office.").

The inference that Congress intended Section 145 to be governed by established administrative-law principles is particularly strong because Congress reenacted Section 145 only six years after enacting the APA, which synthesized and codified the concepts of deferential judi-

cial review that had developed over the preceding years. See *Zurko*, 527 U.S. at 157-158. The pre-1952 limitations on judicial consideration of evidence that could have been presented to the Patent Office, and the courts' deferential review of Patent Office decisions, were simply the application to a particular agency proceeding of more general principles reflected in the APA. See 5 U.S.C. 704, 706. It is therefore particularly unlikely that Congress intended, *sub silentio*, to make new evidence admissible without limitation in Section 145 proceedings, and to treat such evidence as a justification for *de novo* reconsideration of the PTO's conclusions.

2. In construing Section 145 to allow introduction of new evidence without limitation, the court of appeals relied heavily on testimony offered in the congressional hearings that preceded the 1927 amendments to the Patent Act.[10] See Pet. App. 14a-18a. In those hearings, witnesses supporting and opposing the proposed amendments offered a variety of views about the characteristics of judicial proceedings under R.S. 4915. The court of appeals read that testimony to reflect an understanding that "an applicant [could] freely introduce new evidence to the district court." Pet. App. 16a.

As this Court has repeatedly made clear, isolated hearing testimony, particularly the testimony of opponents of proposed legislation, is not reliable evidence of congressional intent and carries little weight in the interpretation of federal statutes. *Bryan* v. *United States*, 524 U.S. 184, 196 (1998); *Kelly* v. *Robinson*, 479 U.S. 36, 51 n.13 (1986). In any event, the testimony on which the court of appeals relied does not establish that the wit-

---

[10] In the 1927 amendments, Congress retained R.S. 4915 without making material changes. Pet. App. 14a-18a; see pp. 4-5, *supra*.

nesses understood new evidence to be admissible without limitation in R.S. 4915 proceedings. Witnesses testified that litigants proceeding under R.S. 4915 could "supplement [the administrative record] by additional evidence." Pet. App. 16a (citation omitted) (quoting testimony of chairman of Patent Section of ABA Legislation Committee). Those observations, however, simply reflected the settled understanding that proceedings under R.S. 4915, unlike direct appeals under R.S. 4911, were not categorically limited to the administrative record. See pp. 33-34, *supra*.

Nor is it significant that some witnesses characterized R.S. 4915 suits as "de novo" proceedings. See, *e.g.*, Pet. App. 16a-17a. Courts have often described R.S. 4915 and Section 145 actions as "de novo" proceedings even while affirming that administrative-law principles preclude the introduction of new evidence that was reasonably available during the PTO proceeding. See, *e.g.*, *DeSeversky*, 424 F.2d at 858 & n.5; *Globe-Union*, 103 F.2d at 728 (describing R.S. 4915 as a "de novo" proceeding while acknowledging limits on admissibility of new evidence). Witnesses' use of the term in 1926 is particularly unrevealing, since the "relevant linguistic conventions" of administrative law "were less firmly established before adoption of the APA." *Zurko*, 527 U.S. at 156.

Much of the testimony on which the court of appeals relied, moreover, reflects the understanding that R.S. 4915 served primarily as a safety valve, allowing the plaintiff to introduce oral testimony that could not have been introduced before the Patent Office.[11] For

---

[11] The Patent Office did not (and the PTO still does not) entertain oral testimony in ex parte proceedings. Although oral testimony was some-

instance, one witness emphasized that R.S. 4915 was "a valuable thing in the unusual case" because it permitted private litigants to "take evidence in a court," thereby allowing the applicant to "make up a record in addition to that he has been enabled to furnish the examiners in the Patent Office." *To Amend Section 52 of the Judicial Code and Other Statutes Affecting Procedure in Patent Office: Hearing on H.R. 6252 and H.R. 7087 Before the House Comm. on Patents*, 69th Cong., 1st Sess. 21 (1926) (statement of ABA representative Charles Howson). The Commissioner of Patents likewise testified that disappointed applicants "want these witnesses to come before the court so that the court can see them."[12] *Procedure in the Patent Office: Hearing on H.R. 7563 and H.R. 13487 Before the House Comm. on Patents*, 69th Cong., 2d Sess 15 (1926) (statement of Commissioner Thomas Robertson); see *id.* at 11. The witnesses' recognition that R.S. 4915 proceedings served that function in no way implied that R.S. 4915 plaintiffs could introduce evidence that they had failed without cause to present to the agency.

---

times permitted in interference proceedings, cross-examination of witnesses was not allowed. See Pet. App. 64a-65a (Dyk, J., dissenting) (summarizing testimony regarding Patent Office practice).

[12] An R.S. 4915 proceeding would thus permit the introduction of oral testimony to supplement the depositions presented to the Patent Office when, for instance, a priority dispute turned on an inventor's testimony as to when he had invented the device in question, such that the district court's ability to make credibility determinations based on observing the witnesses would materially aid the resolution of the case. See, *e.g.*, *Pintarelli* v. *Brogan*, 65 F. Supp. 281, 283-284 (D.R.I. 1946) (using "the advantage of hearing the oral testimony of witnesses" whose depositions were presented to the Patent Office in order to resolve who had invented the device first).

III. NEW EVIDENCE SHOULD BE ADMITTED IN A SECTION 145 SUIT ONLY IF ITS PROPONENT HAD NO REASONABLE OPPORTUNITY TO PRESENT IT TO THE PTO, AND THE COURT SHOULD OVERTURN THE PTO'S DECISION ONLY IF THE EVIDENCE CLEARLY ESTABLISHES THAT THE AGENCY ERRED

A. Consistent with established exhaustion principles, the plaintiff in a Section 145 suit should be permitted to introduce new evidence only if he had no reasonable opportunity to present that evidence to the PTO in the first instance. That rule respects the PTO's primary decisionmaking authority, increases the incentive for patent applicants to compile a full factual record in the agency proceedings, and limits the frequency with which courts must consider new information without the benefit of the agency's expertise. See pp. 21-24, *supra*. Under that approach, Section 145 still provides a useful supplement to Section 141 appeals by allowing a disappointed applicant to introduce evidence that was not reasonably available to him during the examination proceedings.

Contrary to respondent's contention (Br. in Opp. 25-26), restricting the admissibility of new evidence in Section 145 actions will not deprive disappointed patent applicants of full and fair judicial review. The PTO examination process consists of iterative exchanges between the examiner and the applicant, as claims are amended in response to initial rejections and invalidity concerns are addressed. 35 U.S.C. 131-132; 37 C.F.R. 1.105, 1.130, 1.131. If the examiner rejects an application, its final office action must explain the reasons for the rejection. 37 C.F.R. 1.113. PTO rules then afford applicants several opportunities to introduce new evi-

dence designed to overcome the rejection, see p. 24, *supra*, limiting applicants' ability to present new evidence only after the matter is on appeal to the Board, 37 C.F.R. 41.33.[13] Enforcement of these procedural rules is central to the PTO's efficient conduct of its examination process and its ability to allocate its resources, and analogous rules are a ubiquitous feature of federal agency practice. Limiting the admission of new evidence in Section 145 proceedings simply requires patent applicants to comply with the same sorts of evidence-presentation rules that are routinely imposed on parties who appear before other agencies.

B. When a Section 145 plaintiff introduces relevant new evidence that he had no reasonable opportunity to present to the PTO, the appropriate judicial response may depend on the nature of the evidence. When the evidence consists of materials (such as published prior art) that the PTO can consider as part of its examination process, the court ordinarily should remand the case to the PTO to allow the agency to consider the evidence in the first instance. See Pet. App. 52a n.4 (Dyk, J., dis-

---

[13] Respondent contends (Br. in Opp. 26) that the Board's decision in this case contained additional reasoning that could be rebutted only through the introduction of new evidence. Respondent was on notice, however, that he bore the burden of demonstrating error before the Board, and that his opportunities to introduce new evidence on appeal would be limited under PTO rules. When the Board's decision is based on a "new ground of rejection," 37 C.F.R. 41.50(b), such that the applicant lacked a "fair opportunity to react to the thrust of the rejection," *In re Kronig*, 539 F.2d 1300, 1302-1303 (C.C.P.A. 1976), PTO rules allow the applicant to reopen prosecution and submit new evidence in response. 37 C.F.R. 41.50(b)(1). If an applicant receives a Board decision that he believes has that effect, the proper course would be to present that issue to the Board. Respondent never did that here, even though he requested that the Board rehear its initial decision.

senting). That approach is consistent with the principles that generally govern judicial review of agency action, see *Lorion*, 470 U.S. at 744, and it conserves judicial resources by enabling the PTO to correct any errors in its prior decision. See *McKart*, 395 U.S. at 193-195. It is also consistent with the understanding of Section 145 that prevailed before the en banc court's decision in this case. See, *e.g.*, *Putman* v. *Dudas*, 539 F. Supp. 2d 414, 416-421 (D.D.C. 2008) (remanding on the basis of the PTO's statement that reopening the examination was appropriate in light of evidence of patentability not considered during the initial examination process).

When the plaintiff in a Section 145 suit introduces relevant and non-cumulative new evidence that the PTO may not consider (such as oral testimony, see 37 C.F.R. 1.2), remanding to the agency is not a useful option, and the district court must evaluate the new evidence in the first instance. To the extent the new evidence differs from the information that was before the PTO, the court may give it more weight in the analysis. Cf. *Microsoft*, 131 S. Ct. at 2251. But the court should overturn the agency's decision only if the new evidence, considered together with the administrative record, creates a "thorough conviction" that the PTO erred. See *Morgan*, 153 U.S. at 125; pp. 25-27, *supra*. This approach recognizes that the agency's decision should not be reversed unless the court has a high degree of confidence that the decision was incorrect, while permitting the court to give effect to the fact that the district court has before it a fuller record than the PTO.

That approach conforms judicial review of patent denials to review of patent grants. Under *Microsoft*, the presumption that a granted patent is valid can be rebutted only by "clear and convincing evidence" of invalidity,

even when the defendant in an infringement suit introduces evidence that was not before the PTO when it granted the patent. 131 S. Ct. at 2251. In applying the "clear and convincing evidence" standard, however, the judge or jury may give greater weight to evidence that the PTO had no opportunity to consider. *Ibid.* Because judicial review of patent grants is "closely" related to review of patent denials, *Morgan*, 153 U.S. at 123, applying the *Morgan* "thorough conviction" standard in all Section 145 proceedings creates an appropriate symmetry with the *Microsoft* approach. See p. 28, *supra*.

Employing the "thorough conviction" standard in all Section 145 suits also avoids instituting a "standard of [review] that would rise and fall with the facts of each case." *Microsoft*, 131 S. Ct. at 2250. Under the Federal Circuit's approach, Section 145 functions as a judicial-review proceeding subject to the APA when the plaintiff does not rely on new evidence; but when new evidence is introduced, the district court must engage in de novo review of any issues to which that evidence pertains. Pet. App. 30a-31a. The *Microsoft* Court rejected just such a "variable standard" as "unusual and impractical," stating that Congress "would have said so expressly" if it had intended to adopt such a regime. 131 S. Ct. at 2250. A variable standard would be even more anomalous here, since a Section 145 plaintiff (*i.e.*, a disappointed patent applicant) typically has had a far greater opportunity than the defendant in an infringement suit to develop the record before the PTO. In the Section 145 context, affording a more favorable standard of review when new evidence is introduced effectively rewards and encourages the withholding of evidence from the PTO. See pp. 23-24, *supra*.

The court of appeals did not even suggest a policy rationale that might have led Congress to adopt the odd judicial-review scheme that the court's decision creates. In particular, the court identified no reason to believe that the usual policy justifications for exhaustion requirements and deferential review of agency action are somehow absent here. To the contrary, given the technical and fact-intensive nature of the issues involved, and the expert judgments that are reflected in PTO patentability decisions, the concerns that generally underlie those administrative-law principles apply with particular force to Section 145 suits. And the review scheme fashioned by the Federal Circuit can be expected to cause precisely the harms those principles are intended to prevent. The court of appeals therefore erred in construing Section 145 to deviate from well-established principles of administrative review.

CONCLUSION

The judgment of the court of appeals should be vacated and the case remanded for further proceedings.

Respectfully submitted.

DONALD B. VERRILLI, JR.
Solicitor General

TONY WEST
Assistant Attorney General

MALCOLM L. STEWART
Deputy Solicitor General

BETH S. BRINKMANN
Deputy Assistant Attorney General

GINGER D. ANDERS
Assistant to the Solicitor General

SCOTT R. MCINTOSH
Attorney

BERNARD J. KNIGHT, JR.
General Counsel

RAYMOND T. CHEN
Solicitor and Deputy General Counsel

ROBERT J. MCMANUS
THOMAS W. KRAUSE
Associate Solicitors
U.S. Patent and Trademark Office

AUGUST 2011

RESPONDENT'S BRIEF

Supreme Court, U.S.
FILED
OCT 31 2011

No. 10-1219

IN THE
Supreme Court of the United States

DAVID J. KAPPOS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR, UNITED STATES PATENT AND TRADEMARK OFFICE,
Petitioner,

v.

GILBERT P. HYATT,
Respondent.

On Writ of Certiorari to the United States Court of Appeals for the Federal Circuit

BRIEF FOR RESPONDENT

GREGORY L. ROTH
5712 Parkwest Circle
La Palma, California 90623
(714) 723-6871

AARON M. PANNER
Counsel of Record
KELLOGG, HUBER, HANSEN, TODD, EVANS & FIGEL, P.L.L.C.
1615 M Street, N.W.
Suite 400
Washington, D.C. 20036
(202) 326-7900
(apanner@khhte.com)

October 31, 2011

QUESTIONS PRESENTED

1. Whether the Federal Circuit correctly decided that a patent applicant who files a "civil action" under 35 U.S.C. § 145, rather than an "appeal" under § 141, may generally introduce new evidence, in accordance with the Federal Rules of Civil Procedure and the Federal Rules of Evidence, to show that the "applicant is entitled to receive a patent."

2. Whether the Federal Circuit correctly reaffirmed existing law holding that a district court in an action under § 145 adjudicates factual issues *de novo* in cases where an applicant introduces new evidence that was not before the Patent and Trademark Office.

TABLE OF CONTENTS

Page

QUESTIONS PRESENTED i

TABLE OF AUTHORITIES iii

STATEMENT 1

SUMMARY OF ARGUMENT 10

ARGUMENT 15

I. SECTION 145 BROADLY ALLOWS A PATENT APPLICANT TO CHALLENGE A REJECTION THROUGH THE INTRODUCTION OF NEW EVIDENCE 16

A. The Text of § 145, Reinforced by Context, Makes Clear That District Courts Are Authorized To Determine Patentability *De Novo* on a Complete Record 16

B. The History of § 145 Confirms That a Plaintiff Under That Provision Is Entitled To Introduce New Evidence in Accordance with Ordinary Rules of Equity Practice 24

C. The Introduction of Evidence Under § 145 Is Supported by Important Institutional Considerations 37

II. THE DISTRICT COURT DETERMINES FACTUAL ISSUES ON A NEW RECORD BY A PREPONDERANCE OF THE EVIDENCE 42

CONCLUSION 52

TABLE OF AUTHORITIES

Page

CASES

American Heritage Life Ins. Co. v. Heritage Life Ins. Co., 494 F.2d 3 (5th Cir. 1974) 18

Appert v. Brownsville Plate Glass Co., 144 F. 115 (C.C.W.D. Pa. 1904)..... 27

Armstrong v. De Forest, 13 F.2d 438 (2d Cir. 1926)..... 27

Barrett Co. v. Koppers Co., 22 F.2d 395 (3d Cir. 1927).....34, 35, 36

Bernardin v. Northall, 77 F. 849 (C.C.D. Ind. 1897).....27, 29

Berry v. Robertson, 40 F.2d 915 (D. Md. 1930)..... 27

Boucher Inventions v. Sola Elec. Co., 131 F.2d 225 (D.C. Cir. 1942)..... 34

Bragdon v. Abbott, 524 U.S. 624 (1998) 12, 31

Butler v. Shaw, 21 F. 321 (C.C.D. Mass. 1884) 26, 29, 48

Butterworth v. United States ex rel. Hoe, 112 U.S. 50 (1884) 10, 12, 24, 26, 34, 42, 45

Cannon v. University of Chicago, 441 U.S. 677 (1979) 24

Cantrell v. Wallick, 117 U.S. 689 (1886)..... 47

Carter-Mondale Reelection Comm., Inc., In re, 642 F.2d 538 (D.C. Cir. 1980) 49

Central Ry. Signal Co. v. Jackson, 254 F. 103 (E.D. Pa. 1918)..... 27

Chandler v. Roudebush, 425 U.S. 840 (1976) 17

Christie v. Seybold, 55 F. 69 (6th Cir. 1893) 27

Citizens To Preserve Overton Park, Inc. v. Volpe, 401 U.S. 402 (1971) 10

Coffin v. Ogden, 85 U.S. (18 Wall.) 120 (1874) 47

Consolo v. Federal Maritime Comm'n, 383 U.S. 607 (1966) 19

Curtiss Aeroplane & Motor Corp. v. Janin, 278 F. 454 (2d Cir. 1921) 27

Custis v. United States, 511 U.S. 485 (1994) 21

Dickinson v. Zurko, 527 U.S. 150 (1999) 10, 13, 37, 42, 43, 45, 46, 50

Dowling v. Jones, 67 F.2d 537 (2d Cir. 1933) 36

Etten v. Kauffman, 32 F. Supp. 186 (W.D. Pa. 1940), *aff'd*, 121 F.2d 137 (3d Cir. 1941) 36

Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co., 535 U.S. 722 (2002) 42

Forest Grove Sch. Dist. v. T.A., 129 S. Ct. 2484 (2009) 31

Fregeau v. Mossinghoff, 776 F.2d 1034 (Fed. Cir. 1985) 9, 42, 50

Gandy v. Marble, 122 U.S. 432 (1887) 20, 26

General Elec. Co. v. Steinberger, 208 F. 699 (E.D.N.Y. 1913), *aff'd*, 214 F. 781 (2d Cir. 1914) 27

Globe-Union, Inc. v. Chicago Tel. Supply Co., 103 F.2d 722 (7th Cir. 1939) 34, 35

Gould v. Quigg, 822 F.2d 1074 (Fed. Cir. 1987) 20

Greene v. Beidler, 58 F.2d 207 (2d Cir. 1932) 35

Greenwood v. Dover, 194 F. 91 (1st Cir. 1911)..... 27

Griswold, In re, 9 App. D.C. 496 (D.C. Cir. 1896)..... 46

Grogan v. Garner, 498 U.S. 279 (1991)..... 44

Hien, In re, 166 U.S. 432 (1897)..... 26

Hoover Co. v. Coe, 325 U.S. 79 (1945).....10, 12, 31, 34, 36

Ibrahim v. United States, 834 F.2d 52 (2d Cir. 1987)..... 33

Ingersoll v. Holt, 104 F. 682 (C.C.N.D. Cal. 1900)..... 46

Kellogg Co. v. Toucan Golf, Inc., 337 F.3d 616 (6th Cir. 2003)..... 18

Kumar, In re, 418 F.3d 1361 (Fed. Cir. 2005)..... 39

Leithem, In re, No. 2011-1030, 2011 WL 4351585 (Fed. Cir. Sept. 19, 2011)..... 39

Lorillard v. Pons, 434 U.S. 575 (1978)..... 31

Lucke v. Coe, 69 F.2d 379 (D.C. Cir. 1934) 23, 46

Markman v. Westview Instruments, Inc., 517 U.S. 370 (1996) 38

Mazzari v. Rogan, 323 F.3d 1000 (Fed. Cir. 2003)..... 50

Merrill Lynch, Pierce, Fenner & Smith, Inc. v. Curran, 456 U.S. 353 (1982) 24, 31

Microsoft Corp. v. i4i Ltd. P'ship, 131 S. Ct. 2238 (2011) 25, 33, 43, 45, 47, 49, 50, 51

Minnesota Mining & Mfg. Co. v. Carborundum Co., 155 F.2d 743 (3d Cir. 1946) 36

Monessen S.W. Ry. Co. v. Morgan, 486 U.S. 330 (1988) 24

Morgan v. Daniels, 153 U.S. 120 (1894).....12, 14, 29, 30, 43, 46, 47, 48

Motor Vehicle Mfrs. Ass'n of United States, Inc. v. State Farm Mut. Auto. Ins. Co., 463 U.S. 29 (1983) 49

Nichols v. Minnesota Mining & Mfg. Co., 109 F.2d 162 (4th Cir. 1940) 35

O'Donnell v. United Shoe Mach. Corp., 2 F. Supp. 178 (D. Mass. 1933)..... 36

Oetiker, In re, 977 F.2d 1443 (Fed. Cir. 1992) 51

PHC, Inc. v. Pioneer Healthcare, Inc., 75 F.3d 75 (1st Cir. 1996) 18

Radio Corp. of Am. v. Radio Eng'g Labs., Inc., 293 U.S. 1 (1934) 47

Redken Labs., Inc. v. Clairol, Inc., 501 F.2d 1403 (9th Cir. 1974)..... 18

Rodriguez v. Compass Shipping Co., 451 U.S. 596 (1981) 36-37

Rousso v. First Nat'l Bank, 37 F.2d 281 (6th Cir. 1930) 29

Ruschig, In re, 379 F.2d 990 (C.C.P.A. 1967) 7

Schering Corp. v. Marzall, 101 F. Supp. 571 (D.D.C. 1951) 36

Schilling v. Schwitzer-Cummins Co., 142 F.2d 82 (D.C. Cir. 1944)..... 34

Sims v. Apfel, 530 U.S. 103 (2000)..... 23

Smith v. Prutton, 127 F.2d 79 (6th Cir. 1942)..... 36

Sosa v. Alvarez-Machain, 542 U.S. 692 (2004) 21

Spraying Sys. Co. v. Delavan, Inc., 762 F. Supp. 772 (N.D. Ill. 1991), *aff'd*, 975 F.2d 387 (7th Cir. 1992) 18

Squire, In re, 22 F. Cas. 1015 (C.C.E.D. Mo. 1877) 26

St. Paul Fire & Marine Ins. Co. v. United States, 6 F.3d 763 (Fed. Cir. 1993) 44

Stepan Co., In re, No. 2010-1261, 2011 WL 4582488 (Fed. Cir. Oct. 5, 2011) 39

Streck, Inc. v. Research & Diagnostic Sys., Inc., No. 2011-1045, 2011 WL 4978510 (Fed. Cir. Oct. 20, 2011) 40

Syntex (U.S.A.), Inc. v. USPTO, 882 F.2d 1570 (Fed. Cir. 1989) 52

Therasense, Inc. v. Becton, Dickinson & Co., 649 F.3d 1276 (Fed. Cir. 2011) 13, 39

United States v. Carlo Bianchi & Co., 373 U.S. 709 (1963) 19, 20

United States v. Welden, 377 U.S. 95 (1964) 37

Vas-Cath Inc. v. Mahurkar, 935 F.2d 1555 (Fed. Cir. 1991) 7

Warren v. United States, 932 F.2d 582 (6th Cir. 1991) 44

Wright v. Runge, 31 F. Supp. 844 (D.D.C. 1939) 36

CONSTITUTION, STATUTES, REGULATIONS, AND RULES

U.S. Const. art. I, § 8, cl. 8 51

Act of Mar. 2, 1927, ch. 273, § 11, 44 Stat. 1335, 1336-37 30

Act of Dec. 12, 1980, Pub. L. No. 96-517, § 1, 94 Stat. 3015, 3016 37

Administrative Orders Review Act § 2, 5 U.S.C. § 1032 (1964) 19

Administrative Procedure Act, 5 U.S.C. § 501 *et seq.* & § 701 *et seq.* 10, 14, 15, 16, 33, 37, 43, 44, 51

5 U.S.C. § 554 (§ 5) 33

5 U.S.C. § 706(2)(F) 14, 44

Civil Rights Act of 1964, Title VII, 42 U.S.C. § 2000e *et seq.* 17

Leahy-Smith America Invents Act, Pub. L. No. 112-29, § 3(j)(1), 125 Stat. 284, 290 (2011)..... 2

Patent Act of 1836, ch. 357, 5 Stat. 117 25

§ 16, 5 Stat. 123-24 25

Patent Act of 1839, ch. 88, § 10, 5 Stat. 353, 354 25

Patent Act of 1952 (35 U.S.C.) 32, 33, 34

35 U.S.C. § 102 51

35 U.S.C. § 141 .....9, 11, 16, 21, 22, 50

35 U.S.C. §§ 141-144 .....21, 37, 45

35 U.S.C. § 144 .....11, 21

35 U.S.C. § 145 .....2, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 29, 30, 36, 37, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 52

35 U.S.C. § 146 .....14, 30, 40

35 U.S.C. § 282 .....43, 45, 51

35 U.S.C. § 291 18

35 U.S.C. § 306 37

35 U.S.C. § 315(b) 52

Wunderlich Act, 41 U.S.C. § 321 19

7 U.S.C. § 2462 18

15 U.S.C. § 1071 18

15 U.S.C. § 1071(b) 18

28 U.S.C. § 2640(a) 18

Rev. Stat.:

§ 4911 .....25, 28

§ 4915 .....8, 9, 26, 27, 28, 29, 30, 32, 33, 34, 45, 46

37 C.F.R. § 1.114(e)(2) 40

37 C.F.R. § 1.132 (1997) 41

Fed. R. Evid.:

Rule 402 23

Rule 1101(b) 23

Rule 1101(e) 23

LEGISLATIVE MATERIALS

H.R. Rep. No. 96-1307(I) (1980), *reprinted in* 1980 U.S.C.C.A.N. 6460 37

Procedure in the Patent Office: Hearing Before the S. Comm. on Patents, 69th Cong. (1926) 32

S. Rep. No. 82-1979 (1952) 33

To Amend Section 52 of Judicial Code and Other Statutes Affecting Procedure in the Patent Office: Hearing Before the H. Comm. on Patents, 69th Cong. (1926) 30, 31, 32

ADMINISTRATIVE MATERIALS

United States Patent and Trademark Office:

Manual of Patent Examining Procedure (8th ed. rev. 2008) 3

Performance and Accountability Report: Fiscal Year 2010 (2010) 51, 52

OTHER MATERIALS

Brief for the United States as Amicus Curiae Supporting Respondents, *Microsoft Corp. v. i4i L.P.*, No. 10-290 (U.S. filed Mar. 18, 2011)..... 34

4 Donald S. Chisum, *Chisum on Patents* (2005)..... 42

P.J. Federico, *Evolution of Patent Office Appeals*, 22 J. Pat. Off. Soc'y 838 (1940) 25, 28, 33

Mark A. Lemley, *Rational Ignorance at the Patent Office*, 95 Nw. U. L. Rev. 1495 (2001) 38

Jerry L. Mashaw, *Administration and "The Democracy": Administrative Law from Jackson to Lincoln, 1829-1861*, 117 Yale L.J. 1568 (2008) 28

Mem. in Support of Def. PTO's Mot. for J. on the Pleadings and in Opp. to Pls.' Mot. for Summ. J., *Association for Molecular Pathology v. USPTO*, No. 09 Civ. 4515 (RWS) (S.D.N.Y. filed Dec. 24, 2009), 2009 WL 5785024 52

Thomas W. Merrill, *Article III, Agency Adjudication, and the Origins of the Appellate Review Model of Administrative Law*, 111 Colum. L. Rev. 939 (2011) 28, 29

Casper W. Ooms, *The United States Patent Office and the Administrative Procedure Act*, 38 Trademark Rep. 149 (1948) 33

Patstats, patstats.org/Patstats3.html 16

1 Richard J. Pierce, Jr., *Administrative Law Treatise* (5th ed. 2010) 28

Giles S. Rich, *Outline of Patent Law and Procedure*, 3 J. Fed. Cir. Hist. Soc'y 61 (2009) 33

2 William C. Robinson, *The Law of Patents* (1890) 32

2A Norman J. Singer, *Statutes and Statutory Construction* (6th rev. ed. 2000) 21

Emerson Stringham, *Patent Interference Equity Suits* (1930) 29

Albert H. Walker, *The Law of Patents* (5th ed. 1917) 32

STATEMENT

1. Plaintiff Gilbert Hyatt filed a patent application in June 1995 describing a data compression system for storing and processing image information. JA9-259. As amended, the application has 117 independent and dependent claims covering both memory systems and a process of operating such systems. JA274-364.

The examiner found that plaintiff did not "point out the novelty of the amended and added claims" and had "failed to point out where in the specification support may be found for the amended and added claims." C.A. App. A10493. In response, plaintiff filed a "Supplemental Amendment" that included "Remarks" identifying the distinguishing features of the claims over the art. *Id.* at A10504. Plaintiff also identified specific page numbers in the specification where there was antecedent basis for claim features, *id.* at A10504-05, and referred the examiner to the Table of Contents of the specification for additional antecedent basis, *id.* at A10505. Plaintiff noted that he "appreciate[d] th[e] opportunity to provide this support" and would "provide additional support as requested by the Examiner." *Id.*

On July 30, 1997, the examiner issued a final office action rejecting all claims for lack of written description and lack of enablement. JA368-85. All claims were also provisionally rejected for double patenting. JA385-89. In addition, numerous claims were rejected on anticipation and obviousness grounds. JA389-91.

For certain claim features, the examiner provided a brief explanation for the written-description rejections. For example, the examiner rejected all claims because he read them to "cover *simultaneous* writing and reading of a block of graphic image data," while

"[t]he specification describes a *sequential* write to and read from the block memory." JA371 (emphases added). The examiner rejected several claims that he found were "weight related" (that is, related to the intensity to be assigned to the pixels of an image) because the specification "failed to describe an address generator which will generate weight addresses and . . . failed to describe an address generator which will apply the weight addresses . . . at the same time the intensity bits are being applied." JA378-79; *see also* JA369, 376.

In most cases, however, the examiner provided no explanation; instead, the examiner simply identified a claim feature and stated that the written description provided no support for that feature. For example, the examiner rejected multiple claims that included the feature "a vector processor responsive to an accessed block of video pixel image information and to vector information." JA372-73. The rejection states without further elaboration that "[t]his feature of the claims is not supported by applicant[']s originally filed specification nor by [the] parent application." JA373. The examiner took the same approach with respect to nine other groups of claims. JA373-84.

2. Plaintiff appealed the rejection to the Board of Patent Appeals and Interferences ("Board"),[1] filing a 129-page appeal brief. Plaintiff argued, first, that the examiner "has not provided the required objective reasons" in support of the written-description

---

[1] Pursuant to the Leahy-Smith America Invents Act, Pub. L. No. 112-29, § 3(j)(1), 125 Stat. 284, 290 (2011), the Board is now known as the "Patent Trial and Appeal Board." Section 145 has been amended accordingly.

and enablement rejections. JA413.[2] Plaintiff noted that the specification included "detailed schematic diagrams showing actual commercially available electrical components . . . and even showing component pin designations and wire connections" but that the examiner failed to consider that disclosure as a whole. JA416. Next, plaintiff argued that "[v]arious claims stand rejected . . . based upon unclaimed subject matter" – that is, the examiner rejected claims because features *not* claimed were inadequately disclosed. JA417.

Plaintiff explained that the examiner's rejection had failed to "evaluate[] the numerous occurrences of" the terminology that provided the basis for the rejections. JA419. "The experimental system embodiment described in the specification and shown in the figures represents a detailed disclosure of an actual reduced to practice system." JA420. "With the extensive memory disclosure (*e.g.*, Spec. at 99-135) and processor disclosure (*e.g.*, Spec. at 87-98, 214-36) . . . , it is unbelievable that the Examiner would object to the disclosure of memory and processor features." JA421.

Plaintiff then provided an annotated concordance of claim terms. "Table-1" listed "representative terminology" related to the examiner's written-description rejections, the number of occurrences, and "representative cites" to the specification. JA421-22. Table-1 was followed by notes elaborating on disclosure of several features.

---

[2] Plaintiff relied on § 706.03 of the Manual of Patent Examining Procedure (8th ed. rev. 2008), which states that rejections for "lack of proper disclosure . . . should be stated with a full development of the reasons rather than by a mere conclusion coupled with some stereotyped expression." JA412 n.13.

3. The Board reversed many of the rejections but affirmed written-description and enablement rejections in part. App. 200a-254a; *see also* App. 5a ("Mr. Hyatt prevailed on over 93% of the examiner's rejections at the Board level.").[3]

In the case of each of the written-description rejections for which the examiner provided some explanation beyond a bare assertion that the feature did not appear in the disclosure, the Board reversed the rejection. In some of those cases, the Board concluded that certain rejected claims simply did not include the feature. App. 220a-221a, 230a-231a. In others, it concluded that the specification did adequately disclose the feature. App. 219a, 229a. Along the way, the Board criticized plaintiff for "[m]erely pointing to individual words of the limitation," App. 218a,[4] but in at least one case (involving the "data compression" claim phrase) the Board found "support in the specification" at the very page to which Table-1 pointed the Board, App. 219a.

For the other written-description rejections, the Board affirmed while providing explanations absent from the examiner's rejection. For example, as noted above, the examiner did not explain what aspect of the feature "vector processor responsive to an

---

[3] The Board stated that it would "treat the enablement rejections as standing or falling together with the written description rejections." App. 240a.

[4] That is not an accurate characterization even of the annotated Table-1, much less of plaintiff's appeal brief, which refers throughout to the specification. The specification itself is highly structured: it presents a top-level broad block diagram and detailed schematic diagrams; describes all of the relevant components and their interconnections and functions; and outlines this organized presentation in the Table of Contents and in the Brief Description of the Drawings.

accessed block of video pixel image information and to vector information" he found unsupported. JA372-73. By contrast, the Board devoted three pages to an explanation of its reasons for agreeing with the examiner's unexplained conclusion. After finding that the written description did provide "support for a processor 'coupled to the accessing circuit and coupled to the vector generator,'" as recited in the claim, the Board stated:

> However, the limitation at issue requires that the processor perform the function of "generating two dimensional processed image information in response to . . . video pixel information . . . and in response to the two dimensional vector information generated by the vector generator." This implies that the "generating" function operates on two kinds of input data: pixel information from memory and vector information. However, the specification describes graphics vectors being generated (strobed) into image memory (e.g. spec. at 11-12), *not* being generated and used by a processor together with accessed pixel data read out from the block image memory, which would require bypassing the block memory. That is, the disclosed processor only controls the vector generator, it does not receive data from it or operate "in response to" it. Since the vector information is stored into the block memory, we find no written description for a processor coupled to and performing the "generating" function "in response to" the vector information as well as "in response to" image information from the image memory.

App. 223a (ellipses in original); *see also* App. 229a-230a (cross-referencing prior discussion). This was entirely new reasoning.

4. Plaintiff filed a 50-page rehearing request with 100 pages of exhibits that provided detailed responses to the explanations the Board had newly offered. For example, in response to the rejection quoted at length above, plaintiff explained the manner in which the claim limitation at issue read on the disclosure, concluding:

> [B]ecause the vector generation function first accesses a block of image information from image memory and then overlays the block with the vector, the image information written into the image memory is generated in response to both (1) accessed blocks of image information and (2) vector information.

JA689; *see also* JA688-90, 703-11, 716-26. Plaintiff provided comparable elaboration with regard to the Board's other new rationales. JA678-731.

The Board refused to consider the request, stating that plaintiff had added new arguments not contained in his prior briefing. The Board stated that "[t]he examiner's final rejection specifically identified [l]imitations in the claims that were without written description support" and that plaintiff's "only arguments were that words in the various limitations appear in the specification." App. 257a. "Appellant now attacks our decision with extensive new arguments about how the disclosure can be interpreted to satisfy the claim limitations. . . . Since the final rejection expressly identified the limitations without written descriptive support, appellant could have presented the arguments earlier and cannot contend

that he is merely responding to new rationale[s] in our opinion." *Id.*

5. Plaintiff filed an action in the U.S. District Court for the District of Columbia against the Director of the Patent and Trademark Office ("PTO") pursuant to 35 U.S.C. § 145. In opposition to the Director's motion for summary judgment, plaintiff proffered a declaration explaining that one of ordinary skill in the art would have found an adequate written description for each of the rejected claims.[5] The court held that plaintiff had provided no adequate explanation for failing to submit his declaration to the PTO during prosecution; that his failure was "negligent"; and that the evidence would be disregarded. App. 189a. Reviewing the Board's finding on the record before the Board under a "deferential 'substantial evidence' standard," the court granted summary judgment against plaintiff. App. 189a-190a; *see* App. 190a-198a. Plaintiff's request for reconsideration was denied. C.A. App. A26-32.

6. A divided panel of the Federal Circuit affirmed. The decision held that the district court had properly disregarded plaintiff's declaration because plaintiff had "willfully refused to provide evidence in his possession in response to a valid action by the examiner." App. 139a. The panel majority stated that it was not resolving the question whether a district court could exclude evidence "on grounds other than

---

[5] The Federal Circuit and its predecessor, the Court of Customs and Patent Appeals, have long held that the adequacy of written description is an issue of fact: that is, whether the specification "'convey[s] clearly to those skilled in the art, . . . in any way, the information that appellants invented'" the claimed invention. *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1561 (Fed. Cir. 1991) (Rich, J.) (quoting *In re Ruschig*, 379 F.2d 990, 996 (C.C.P.A. 1967) (Rich, J.)).

the type of refusal at issue here and in [*Barrett Co. v. Koppers Co.*, 22 F.2d 395 (3d Cir. 1927)]." App. 140a n.31. Judge Moore dissented, stating that the majority opinion "takes away this patent applicant's fundamental right to a 'civil action to obtain [a] patent' as granted by Congress in" § 145. App. 149a (alteration in original).

7. The *en banc* Federal Circuit granted rehearing and reversed. The court noted that § 145 authorizes a "civil action," without placing any special limitations on a plaintiff's right to introduce evidence. App. 12a. Such an action "is distinct from an appeal, in which the applicant would be limited to the record before the Patent Office"; the "plain language" of § 145 provides that "this civil action does not merely afford judicial review of agency action" but "directs that the district court may 'adjudge that such applicant is entitled to receive a patent for his invention . . . as the facts in the case may appear.'" *Id.* (ellipsis in original). The court found that the "lengthy legislative history of § 145 and its predecessor statute" confirms that "Congress intended to provide for a civil action in which an applicant would be free to introduce new evidence." *Id.*

The court rejected the government's argument that an applicant "is only allowed to introduce new evidence that the applicant could not reasonably have provided to the agency in the first instance." App. 21a (internal quotations omitted). With respect to the government's principal argument – namely, that the "bill in equity" authorized by Revised Statutes § 4915 ("R.S. § 4915"), the predecessor to § 145, was only a "bill of review" – the court held that a bill of review was strictly a mechanism for a court in equity to revisit *its own* prior decree. Such a charac-

terization of the "bill in equity" authorized by R.S. § 4915 was contrary to not only basic rules of equity procedure but also Supreme Court and other federal court precedent. The court dismissed the government's "policy considerations" as matters within Congress's discretion. App. 32a-33a. Relying in part on *amicus* briefs filed by the leading associations of patent lawyers, the court specifically rejected the government's claim that its holding would either encourage patent applicants to withhold evidence or push them to file actions under § 145 rather than on-the-record appeals under § 141. App. 33a-34a.

The court held that "proceedings before the Patent Office remain relevant in a § 145 action." App. 27a. First, the court observed that, in the absence of new evidence, "the district court must apply the court/agency standard of review to [agency] fact finding." *Id.* (citing *Fregeau v. Mossinghoff*, 776 F.2d 1034, 1038 (Fed. Cir. 1985)). Second, the court noted that "issues (and evidence relating to new issues) that were not raised in the Patent Office proceedings generally may not be raised in a § 145 proceeding." App. 28a. Third, while the court "reject[ed] the Director's proposed restrictions on admissibility," it stated that, under existing law, "the district court may consider the proceedings before and findings of the Patent Office in deciding what weight to afford an applicant's newly-admitted evidence." *Id.*

8. Judge Newman concurred in part and dissented in part. She would have held that the district court is required to make all determinations *de novo* – whether or not new evidence is introduced. App. 36a-43a.

Judge Dyk, joined by Judge Gajarsa, dissented. They would have held that an action under § 145 is no different from any other action for judicial review

under the Administrative Procedure Act ("APA") and "based on the agency record" unless "'agency fact-finding procedures are inadequate.'" App. 51a (quoting *Citizens To Preserve Overton Park, Inc. v. Volpe*, 401 U.S. 402, 415 (1971)). Acknowledging that this was not the government's position, the dissent insisted that "there is little difference between the standard for the receipt of new evidence urged by the PTO and the standard I think is appropriate." App. 52a n.4.

SUMMARY OF ARGUMENT

I. **Admission of Evidence.** The core procedural right afforded by the civil action under § 145 – confirmed by its text, structure, and history – is to "sav[e] to litigants the option of producing new evidence in a court." *Hoover Co. v. Coe*, 325 U.S. 79, 87 (1945); *see also Dickinson v. Zurko*, 527 U.S. 150, 164 (1999) (noting that § 145 "permits the disappointed applicant to present to the court evidence that the applicant did not present to the PTO"); *Butterworth v. United States ex rel. Hoe*, 112 U.S. 50, 61 (1884) (district court rules on "all competent evidence adduced, and upon the whole merits"). The government is wrong to ask this Court to take away a right that Congress has so carefully preserved.

A. The language of § 145 establishes that a district court, in an action under that provision, has the power to receive evidence whether or not the evidence was, or could have been, introduced before the PTO. The wording of § 145 – which calls for a "civil action" in which the court "may adjudge that such applicant is entitled to receive a patent . . . as the facts in the case may appear" – is distinctive. That language indicates that the trial judge must determine factual issues for itself, not generally limit

itself to on-the-record review of the PTO's determination.

The conclusion that § 145 authorizes a *de novo* proceeding with new evidence is particularly clear when its language is contrasted with the language of other provisions of the statute. Section 141 authorizes an "appeal" of a PTO decision in the Federal Circuit, and § 144 directs that, in a § 141 "appeal," the court "shall *review* the decision from which an appeal is taken *on the record*" before the PTO (emphases added). Section 141 expressly states that its appellate-review path, which is subject to § 144, is an either-or alternative to a § 145 proceeding. Congress provided the civil action under § 145 as an alternative to § 141, drawing a fundamental distinction between an on-the-record appeal (§§ 141, 144) and a *de novo* action (§ 145) where new evidence would be admitted and the merits of the applicant's claims "adjudicat[ed]" by the district judge.

B. The long history of § 145 strongly reinforces the conclusion that plaintiffs, in supporting their claims under § 145, may present evidence that they could have presented to the PTO (but did not). Section 145 is the current codification of a cause of action that dates back to 1839. From that date until 1952 (when Congress adopted the modern terminology "civil action"), the statute authorized a "bill in equity" that – like § 145 – required the court to "adjudge that such applicant is entitled" to a patent. Congress would have understood that such a bill would invoke the original – not appellate – jurisdiction of the federal court and that new evidence would consequently be admitted in such cases.

Indeed, this Court long ago recognized that the basic distinction between direct appeal and the "bill

in equity" authorized by § 145's predecessors was precisely that the latter allowed for introduction of new evidence and an adjudication of the patent applicant's rights on the complete record. *See Butterworth*, 112 U.S. at 61 (noting that such an action is not "confined to the case as made in the record of [the patent office], but is prepared and heard upon all competent evidence adduced, and upon the whole merits"). When Congress preserved the bill in equity in its 1927 recodification, it did so against the backdrop of that settled interpretation – thereby incorporating it. *See Bragdon v. Abbott*, 524 U.S. 624, 645 (1998). This Court adopted no limitations on the introduction of new evidence beyond those applicable in any equitable action prior to the enactment of § 145, in a form close to its present form, in 1952. *See Hoover*, 325 U.S. at 87.

Although the government argues otherwise, *Morgan v. Daniels*, 153 U.S. 120 (1894), cannot support any limitation on the introduction of evidence in actions under § 145. The plaintiff there did not seek to introduce new evidence, so the question was not even presented. Nor can *Morgan* be read, without pure anachronism, as treating the predecessor statute as a "judicial review" provision that incorporates "background principles" governing "judicial review of agency action" (Pet'r Br. 11); the modern concept of "judicial review" did not exist when the case was decided. Divergent post-1927 lower-court opinions likewise provide no basis for inferring that Congress, in 1952, intended to modify the accepted practice – reaffirmed by this Court in 1945 – of allowing applicants like plaintiff to introduce new evidence in district court even if the evidence could have been provided to the PTO; much less do those decisions

support the virtual prohibition on new evidence the government advocates.

C. Congress's decision to preserve the original action to obtain a patent sensibly reflects important institutional considerations. There is, indeed, a gap between the "without cause" standard the government endorses and the "could have presented" interpretation it tries to give that standard: an applicant can plainly have good cause for *not* presenting to the PTO every bit of evidence that the applicant *could* present, including evidence that should be presented in court for a sound adjudication. Specifically, to build a case for consideration by a non-expert district judge may require evidence that would be superfluous before the PTO with its technical experts. The government's pervasive emphasis on the PTO's comparative expertise thus itself provides a central explanation for § 145's allowance of additional evidence when non-expert district courts must address patentability issues. Furthermore, limiting a patent applicant to the record made before the PTO pressures applicants to submit any evidence of conceivable later relevance, further burdening an overburdened agency. *See Therasense, Inc. v. Becton, Dickinson & Co.*, 649 F.3d 1276, 1289-90 (Fed. Cir. 2011) (en banc).

II. **Standard of Proof.** When a plaintiff under § 145 introduces new evidence, the district court must decide factual questions on the record before it "as the facts in the case may appear." 35 U.S.C. § 145; *see Zurko*, 527 U.S. at 164 (noting that, in an action under § 145, "[t]he presence of . . . new or different evidence makes a factfinder of the district judge"). By its terms, the statute authorizes a new factual determination, not deferential review. The

government nevertheless argues that a plaintiff under § 145 bears a heightened standard of proof to establish entitlement to a patent. But there is no textual or historical support for imposing a standard of proof different from the preponderance-of-the-evidence standard that applies in other civil litigation, including *de novo* trials challenging agency action. *See* 5 U.S.C. § 706(2)(F).

Morgan does not provide any precedent for imposing a heightened burden in a case challenging an *ex parte* rejection under § 145 with new evidence. That case and its express ruling were limited to an effort (a) without new evidence (b) to deprive another private party of property – an issued patent – (c) after an adversarial adjudication resolving a priority dispute between the two purported inventors. Whatever the current status of *Morgan* for that context (addressed by § 146), it did not establish any heightened standard of proof for the present *ex parte* denial context of § 145.

The argument that there is an "irrational asymmetry" between the regime governing challenges to patent denials and the standard governing challenges to the validity of issued patents (Pet'r Br. 28) ignores the fundamental statutory difference between the two, based on the special solicitude Congress has long shown for inventors. Thus, when a patent is granted, as the PTO itself has repeatedly insisted, adversely affected interested persons (*e.g.*, those likely to be infringing) cannot obtain direct APA-type judicial review but instead generally challenge the correctness of patent grants in private litigation (to which the PTO is not even a party) where a clear-and-convincing-evidence standard applies. In contrast, Congress gave a person *denied* a patent two

separate avenues for relief – one by direct appellate review, the other by *de novo* adjudication in district court. The contrast in treatment of grants and denials in this distinctive patent-specific regime cannot properly be erased by the government's proposed analogy to validity challenges in infringement suits.

ARGUMENT

The government's contention that § 145 generally does no more than authorize deferential review of a patent denial on the record before the PTO substitutes the government's policy preference for the clear meaning of a venerable statute. For generations, § 145 has been understood to permit a patent applicant to bring an original action, complete with new evidence, to show that the PTO has wrongfully deprived the applicant of the intellectual property that a patent represents.

The government's contrary arguments rest centrally on a background assumption that PTO-judicial interactions broadly and in general conform to the modern administrative law model. But that picture is fundamentally inaccurate. The PTO today is, as it has always been, an agency that falls largely outside the ordinary APA regime of judicial review. The reason is that, when the PTO *grants* a patent, a person aggrieved by that determination (*i.e.*, a potential infringer) can virtually never litigate the correctness of the PTO determination (*i.e.*, litigate patent validity) in an APA action for direct judicial review. Rather, except in the rare cases where the PTO engages in *inter partes* reexamination – from which a third-party challenger may seek Federal Circuit review – a potential infringer must challenge the validity of a patent through infringement litigation. In such litigation, the PTO is not a party, and the parties

are never limited to the PTO record. Such non-APA actions form by far the largest category of court cases involving PTO determinations.[6] Section 145 thus must be understood within a distinctive patent-law framework, in which patentability decisions are almost always made in court outside the APA regime and on a new and complete record.

I. SECTION 145 BROADLY ALLOWS A PATENT APPLICANT TO CHALLENGE A REJECTION THROUGH THE INTRODUCTION OF NEW EVIDENCE

A. The Text of § 145, Reinforced by Context, Makes Clear That District Courts Are Authorized To Determine Patentability *De Novo* on a Complete Record

1. The language of § 145 authorizes an original "civil action" seeking *de novo* adjudication of the merits of an applicant's patent application; it does not support the imposition of limitations on new evidence associated with appellate-style on-the-record review. First, the statute authorizes a "civil action" in district court – *i.e.*, a court of original jurisdiction that customarily takes evidence. Second, the statute authorizes the district court to "adjudge that such applicant is entitled to receive a patent for his invention"; it does not limit the district court to evaluating

---

[6] Patent *grants* are usually litigated in infringement suits – of which more than 2,500 are filed each year, with validity at issue in most. In comparison, patent *denials*, when litigated, go either to the Federal Circuit under § 141 – averaging 50-100 appeals each year – or to district court under § 145 – averaging fewer than 10 each year. *See* patstats.org/Patstats3.html; Hyatt Br. in Opp. 24-25. PTO patent decisions thus get challenged in private validity litigation (without the PTO present and outside the APA) vastly more often than in litigation with the PTO.

the prior determination of the Board. Third, the statute authorizes the district court to make its determination "as the facts in the case may appear"; it does not limit the court to consideration of the record before the PTO. In *Chandler v. Roudebush*, 425 U.S. 840 (1976), this Court determined that the private-sector "civil action" authorized by the Civil Rights Act of 1964 (as amended) was "clearly" a "*de novo*" action, in part because of the requirement that the district court, itself, make "find[ings]" after a hearing. *Id.* at 845. The same conclusion applies to § 145's "civil action" for district court "adjudication" based on all "the facts in the case."

The government makes little effort to address the significance of the "terminology employed by Congress," *Chandler*, 425 U.S. at 845, instead arguing that, because § 145 might be described as authorizing "judicial review," § 145 must "incorporate background administrative-law principles," including limitations on the introduction of new evidence, Pet'r Br. 19. But that argument builds an inference on language that is not even in § 145, and the provision's actual language is to the contrary. Section 145 does not, by its terms, authorize the court to review the PTO's determination but to "adjudicate" the underlying merits of the applicant's entitlement to a patent on "the facts in the case." Indeed, while Congress has enacted a variety of provisions authorizing judicial review, the wording of § 145 – in particular its instruction that the district court rule "as the facts in the case may appear" – is essentially unique in the United States Code, appearing only in that provision and two other intellectual-property provi-

sions modeled on it.[7] *See* 7 U.S.C. § 2462 (plant-variety protection); 15 U.S.C. § 1071(b) (trademark registration).[8] Likewise, the statutory authorization for a court to "adjudicate" a substantive issue in a "civil action" is distinctive – and it, too, elsewhere denotes a *de novo* proceeding, not limited on-the-record review (and nowhere is used to authorize limited on-the-record review). *See, e.g.*, 35 U.S.C. § 291 (granting the "owner of an interfering patent" the right to bring a "civil action" in which "the court may adjudge the question of the validity of any of the interfering patents").[9]

---

[7] The government acknowledges that, where a court is directed to make its determination on "the record made before the court," the court's review is *de novo*. *See* Pet'r Br. 19 n.3 (citing 28 U.S.C. § 2640(a)). The statutory phrase "as the facts in the case may appear" likewise indicates that the district court should receive new evidence – *i.e.*, permit the parties to develop "the facts" – and not limit itself to the record developed before the PTO.

[8] While 7 U.S.C. § 2462 does not appear to have been judicially construed, 15 U.S.C. § 1071 – which authorizes a civil action to challenge a PTO determination involving registration of a trademark – has been uniformly interpreted to permit a plaintiff to introduce new evidence not before the agency. *See, e.g.*, *Kellogg Co. v. Toucan Golf, Inc.*, 337 F.3d 616, 622-23 (6th Cir. 2003); *PHC, Inc. v. Pioneer Healthcare, Inc.*, 75 F.3d 75, 80 (1st Cir. 1996); *Redken Labs., Inc. v. Clairol, Inc.*, 501 F.2d 1403, 1404 (9th Cir. 1974); *American Heritage Life Ins. Co. v. Heritage Life Ins. Co.*, 494 F.2d 3, 9 (5th Cir. 1974); *Spraying Sys. Co. v. Delavan, Inc.*, 762 F. Supp. 772, 775 (N.D. Ill. 1991), *aff'd*, 975 F.2d 387 (7th Cir. 1992); *see also* AIPLA Br. 18-20.

[9] Although the government cites (at 19 n.3) statutes that expressly provide for the introduction of evidence, those statutes shed little light on the proper construction of § 145 – which has its own distinctive language – particularly because each of the statutes was enacted when on-the-record review of agency action was the established norm. Those statutes do, however,

The government relies on *Consolo v. Federal Maritime Commission*, 383 U.S. 607 (1966), and *United States v. Carlo Bianchi & Co.*, 373 U.S. 709 (1963), but the provisions at issue there were sharply different from § 145. Neither statute authorized the court to adjudicate the merits of the underlying legal question. *Consolo* involved a provision authorizing an action *in the court of appeals* "'to enjoin, set aside, suspend . . . , or to determine the validity of . . . final orders of the . . . Federal Maritime Board.'" 383 U.S. at 613 (third ellipsis in original) (quoting Administrative Orders Review Act § 2, 5 U.S.C. § 1032 (1964)). Because courts of appeals have no procedures for taking evidence, and because the scope of review is expressly limited to the "validity" of an agency's order and refers to the action as a "direct *review* proceeding," *see id.* (emphasis added), the statute cannot be read to authorize a *de novo* civil action. *Carlo Bianchi* involved a provision (the Wunderlich Act) that preserves "judicial review" of certain executive branch decisions under "'disputes' clause[s]" of federal contracts, allowing the court to intervene only if the agency's decision was "'fraudulent or capricious or arbitrary or so grossly erroneous as necessarily to imply bad faith, or . . . not supported by substantial evidence.'" 373 U.S. at 714 (quoting 41 U.S.C. § 321). This Court held that, in light of the statute's express authorization of "review" and its use of language that is "consistently . . . associated with a review limited to the administrative record," the language Congress enacted indicated that the "reviewing court" should determine "the reasonable-

---

show that, while on-the-record review of agency action is the norm, it is not the exclusive means by which Congress provides for judicial review.

ness of what the agency did *on the basis of the evidence before it*." *Id.* at 715. The language of § 145 is not compatible with such a limited function.

This does not mean that the proceedings before the PTO have no bearing on the nature of the action under § 145 or that the district court disregards the administrative record. By its terms, § 145 authorizes the district court to "adjudge that [the] applicant is entitled to receive a patent for his invention, *as specified in any of his claims involved in the decision of the Board*." 35 U.S.C. § 145 (emphasis added). Thus, a § 145 "proceeding is, in fact and necessarily, a part of the application for the patent," *Gandy v. Marble*, 122 U.S. 432, 439 (1887), in that the question is whether the plaintiff is entitled to a patent on the claims as presented in the application.

Furthermore, this case does not present any question concerning the scope of the remedy in a case where a district court determines that an applicant is "entitled to receive a patent." The government's contention that "[t]he court's role is . . . to review the PTO's conclusions and to set them aside if they are erroneous," Pet'r Br. 16, however, contradicts the express terms of the statute. The statute directs the district court to "adjudge that [the] applicant is entitled to receive a patent for his invention" and then to "authorize the Director to issue such patent *on compliance with the requirements of law*." 35 U.S.C. § 145 (emphasis added). That language has been understood to indicate that the PTO (not the district court) must issue any patent and to permit the PTO to consider additional objections to patentability not at issue in the civil action before doing so. *See Gould v. Quigg*, 822 F.2d 1074, 1079 (Fed. Cir. 1987). But the procedure that governs *after* the district court

adjudication does not change the fact that the district court is required to adjudicate the merits of the claims presented to the PTO, and not simply to review a prior administrative determination.

2. The contrast between the trial-court procedure under § 145 and the appellate review provided under §§ 141-144 reinforces the conclusion that § 145 authorizes a *de novo* civil action. Section 141 expressly authorizes an "appeal" to the Federal Circuit and declares that this is (now) an either-or alternative to the procedure under § 145. Section 144 directs the Federal Circuit to "*review* the decision . . . *on the record* before the [PTO]" (emphases added). These restrictions on the scope of appellate review of PTO determinations are the very restrictions that the government argues should be imported into § 145. That is, § 141 designates an appellate court (which ordinarily does not consider new evidence) as the venue for an "appeal," and § 144 limits the appellate court to review of the PTO's decision – as opposed to adjudication of the underlying merits – on the administrative record. To read § 145 to provide equivalent relief – at least in most cases – violates the principle that effect must be given to the use of divergent language in closely related statutory provisions. *See, e.g.*, *Sosa v. Alvarez-Machain*, 542 U.S. 692, 711 n.9 (2004) (applying "the usual rule that 'when the legislature uses certain language in one part of the statute and different language in another, the court assumes different meanings were intended'") (quoting 2A Norman J. Singer, *Statutes and Statutory Construction* § 46:06, at 194 (6th rev. ed. 2000)); *Custis v. United States*, 511 U.S. 485, 492 (1994).

The government's argument that § 145 has a "distinct role[]" so long as a plaintiff "may introduce

evidence that he had no reasonable opportunity to present to the PTO" (Pet'r Br. 19) fails to respect the sharp difference in statutory language. As a practical matter, the government does not explain what sort of evidence would fall into the "no reasonable opportunity" category. The government would not concede that an applicant lacked the opportunity to introduce "published prior art" (at 43) during patent prosecution. And, while an applicant cannot introduce "oral testimony" in the PTO (at 44), the *content* of any such oral testimony could be submitted in writing.[10] Thus, the government's standard would at most permit a change in the form of testimony, not its substance. While it is possible to conceive of a case in which a change in the form of testimony will matter in the *ex parte* application cases that § 145 governs, the government's position reduces § 145 to virtually nothing. *Cf.* IPOA Br. 9 & n.4.

The question is not whether the government's reading would render § 145 complete surplusage but whether it makes sense to read the statute as creating two essentially equivalent avenues for relief. In the usual case – where a patent applicant cannot show that the evidence that the applicant seeks to introduce could not have been introduced before the PTO – there is no longer any distinction between § 141 and § 145, except that the latter provides for a stop at the district court before review by the Federal Circuit, with the patent applicant bearing the cost of

---

[10] To cover this very case, the government must be insisting that the content of proposed oral testimony generally have been submitted in writing to the PTO. Plaintiff's proffered declaration at summary judgment, like summary-judgment declarations generally, was a proffer of what his oral testimony would be at trial, yet the government argued that it could not be considered.

an additional proceeding. *See* 35 U.S.C. § 145 ("All the expenses of the proceedings shall be paid by the applicant."). The government's construction would thus eliminate § 145 as a meaningful alternative for nearly all patent applicants.

3. Because § 145 is a *de novo* civil action, the admissibility of evidence is governed by the Federal Rules of Evidence and Civil Procedure. *See* Fed. R. Evid. 1101(b) ("[t]hese rules apply generally to civil actions"); *id.* 402 ("All relevant evidence is admissible, except as otherwise provided by the Constitution of the United States, by Act of Congress, by these rules, or by other rules prescribed by the Supreme Court pursuant to statutory authority."); *cf. id.* 1101(e) (noting that Federal Rules of Evidence apply in proceedings for "review of agency actions when the facts are subject to trial de novo under [5 U.S.C. §] 706(2)(F)").

The government argues that otherwise-admissible evidence that an applicant failed to introduce before the PTO may be excluded under principles of administrative exhaustion, but that argument conflicts with the statutory remedy that § 145 provides. Plaintiff here met the statute's express exhaustion requirement by pursuing his application for a patent through "the [Board] in an appeal under section 134(a)," and he limits his § 145 suit to "claims involved in the decision of the Board." 35 U.S.C. § 145; *cf. Lucke v. Coe*, 69 F.2d 379, 382 (D.C. Cir. 1934) ("[W]hile section 4915 authorizes the introduction of new evidence, it does not authorize the filing of additional claims."). Moreover, because plaintiff contested the examiner's written-description rejections at every stage before the PTO, he satisfied any non-textual "issue exhaustion" requirement as well. *Sims v. Apfel*, 530 U.S. 103, 110 (2000). Beyond

claims for relief and issues, if administrative-exhaustion doctrine ever focuses on the supporting evidence presented to the agency, it cannot be so extended unless the statutory scheme so contemplates. Here, it plainly does not. General exhaustion principles could not be stretched to effect the exclusion of evidence the government seeks – barring all evidence that could reasonably have been presented to the PTO – without effectively destroying the remedy that Congress preserved.

B. The History of § 145 Confirms That a Plaintiff Under That Provision Is Entitled To Introduce New Evidence in Accordance with Ordinary Rules of Equity Practice

From the time that the predecessor to § 145 was enacted in 1839 until today, courts, including this Court, have construed the provision to require a trial court to adjudicate a patent applicant's rights based on "all competent evidence adduced, and upon the whole merits," and "according to the ordinary course of equity practice and procedure." *Butterworth*, 112 U.S. at 61. Congress's "failure to disturb a consistent judicial interpretation of a statute" by this Court indicates that "'Congress at least acquiesces in, and apparently affirms, that [interpretation].'" *Monessen S.W. Ry. Co. v. Morgan*, 486 U.S. 330, 338 (1988) (quoting *Cannon v. University of Chicago*, 441 U.S. 677, 703 (1979)) (alteration in original). That principle applies with particular force where, as here, "Congress has amended the [statute] on several occasions," but "has never attempted to amend" the settled judicial interpretation. *Id.* at 338-39; *see also Merrill Lynch, Pierce, Fenner & Smith, Inc. v. Curran*, 456 U.S. 353, 382 n.66 (1982). Because the nature of the action provided under § 145 has had

"an established meaning traceable to the mid-19th century," *Microsoft Corp. v. i4i Ltd. P'ship*, 131 S. Ct. 2238, 2248 n.7 (2011), the Court should reject the government's plea to depart from that prior understanding.

1. Under the Patent Act of 1836, ch. 357, 5 Stat. 117 ("1836 Act"), Congress eliminated the system of patent registration that had been in place since 1793, in favor of a system of patent examinations.[11] In 1839, Congress expanded the remedy of a bill in equity – which had previously been limited to certain cases involving interferences – to cover all cases in which patents were refused.[12] From 1839 until 1927, an aggrieved patent applicant was required first to pursue an appeal of the Patent Office decision – that is, direct, on-the-record review. If the appeal was unsuccessful, the applicant could initiate a suit in federal court with original equity jurisdiction. "This form of review" – that is, the bill in equity – "was thus . . . given the scope which has been maintained to the present day."[13]

This Court understood that the basic distinction between direct appeal and the bill in equity was that the latter allowed for introduction of new evidence and an adjudication of the patent applicant's rights on the complete record. As this Court explained, under the appeal provision – Revised Statutes § 4911 – "the court act[s] only on the evidence adduced before [the Commissioner], and confin[es] its revision

---

[11] *See* P.J. Federico, *Evolution of Patent Office Appeals*, 22 J. Pat. Off. Soc'y 838, 838 (1940).

[12] *See* Patent Act of 1839, ch. 88, § 10, 5 Stat. 353, 354; *see also* 1836 Act § 16, 5 Stat. 123-24.

[13] Federico, 22 J. Pat. Off. Soc'y at 935.

to the points set forth in the reasons of appeal." *Butterworth*, 112 U.S. at 60. By contrast, the "bill in equity" – § 4915 – "means a proceeding in a court of the United States having original equity jurisdiction under the patent laws, according to the ordinary course of equity practice and procedure." *Id.* at 61. The Court continued:

> It is not a technical appeal from the patent-office, like that authorized in section 4911, confined to the case as made in the record of that office, but is prepared and heard upon all competent evidence adduced, and upon the whole merits. Such has been the uniform and correct practice in the circuit courts.

Id. In addition, the lower-court cases cited in *Butterworth* make clear that new evidence was admissible without restriction. *See In re Squire*, 22 F. Cas. 1015, 1016 (C.C.E.D. Mo. 1877) (No. 13,269) ("[T]he hearing is altogether independent of that before the commissioner, and takes place on such testimony as the parties may see fit to produce agreeably to the rules and practice of a court of equity.") (internal quotations omitted); *Butler v. Shaw*, 21 F. 321, 327 (C.C.D. Mass. 1884) ("[T]he court may receive new evidence, and has the same powers as in other cases in equity.").

This Court has repeatedly confirmed this understanding. *See In re Hien*, 166 U.S. 432, 439 (1897) ("The bill in equity provided for by section 4915 is wholly different from the proceeding by appeal from the decision of the commissioner .... The one is in the exercise of original, the other of appellate, jurisdiction."); *Gandy*, 122 U.S. at 439 ("the proceeding by bill in equity, under section 4915, on the refusal to grant an application for a patent, intends a suit

according to the ordinary course of equity practice and procedure, and is not a technical appeal from the patent-office, nor confined to the case as made in the record of that office, but is prepared and heard upon all competent evidence adduced"). Section 4915 was applied in numerous cases by the lower federal courts, all of which recognized that such suits invoked the courts' original equity jurisdiction, "with all the customary power of an equity court to hear the evidence fully and to make its own findings." *Berry v. Robertson*, 40 F.2d 915, 917 (D. Md. 1930).[14]

The authorization of a *de novo* action as a remedy for the unlawful action of the Patent Office was, moreover, consistent with contemporary understanding of the judicial role vis-à-vis executive action. "[I]n the nineteenth century, either a court had authority to review administrative action or not, and

---

[14] *See, e.g.*, *Armstrong v. De Forest*, 13 F.2d 438, 440 (2d Cir. 1926) ("That the suit is also a new and independent proceeding to obtain a patent, and not an appeal from an antecedent decision, is well settled."); *Curtiss Aeroplane & Motor Corp. v. Janin*, 278 F. 454, 458 (2d Cir. 1921); *Central Ry. Signal Co. v. Jackson*, 254 F. 103, 105 (E.D. Pa. 1918) ("[A]lthough [the] purpose [of a proceeding under § 4915] is to secure the issue of a patent, the issue of which has been refused, it does not seek that issue through a reversal of the ruling first made, but through an independent finding that the applicant is entitled upon the merits of his application to a patent."); *General Elec. Co. v. Steinberger*, 208 F. 699, 700 (E.D.N.Y. 1913), *aff'd*, 214 F. 781 (2d Cir. 1914); *Greenwood v. Dover*, 194 F. 91, 92 (1st Cir. 1911); *Appert v. Brownsville Plate Glass Co.*, 144 F. 115, 117 (C.C.W.D. Pa. 1904); *Bernardin v. Northall*, 77 F. 849, 852 (C.C.D. Ind. 1897) ("[t]he trial in the circuit court is in the strictest sense a judicial hearing by original bill, with all the powers of a court of equity"); *Christie v. Seybold*, 55 F. 69, 72 (6th Cir. 1893) (Taft, J.).

if it did, it decided the whole case."[15] "In all cases, . . . the court based its decision on the record produced in court. That might include the record generated by the agency, but it could include supplemental evidence as well."[16] The idea that a court in equity would be constrained in its consideration of any legal or factual issues in an original action that properly invoked the court's authority would have been alien to contemporary lawyers.

To read appellate-type constraints into § 4915 would have been particularly untenable, because a plaintiff complaining of an *ex parte* denial under that provision would *already* have pursued a direct appeal under § 4911. Prior to 1927, an unsuccessful patent applicant was required to appeal a rejection twice within the Patent Office – to the Board of Examiners-in-Chief and then to the Commissioner of Patents – and then to the Court of Appeals of the District of Columbia. Only once those appeals were exhausted could the applicant file a suit in equity.[17] If the suit in equity were generally limited to the Patent Office record, such further proceeding would generally be barred by *res judicata*. But that was plainly not so. Because the appellate court decided the appeal "on

---

[15] Thomas W. Merrill, *Article III, Agency Adjudication, and the Origins of the Appellate Review Model of Administrative Law*, 111 Colum. L. Rev. 939, 952 (2011). During that period, non-ministerial executive action was broadly considered unreviewable by courts; the remedy for an invasion of rights by an executive official was a common-law action against that official. *See* Jerry L. Mashaw, *Administration and "The Democracy": Administrative Law from Jackson to Lincoln, 1829-1861*, 117 Yale L.J. 1568, 1669-84 (2008); 1 Richard J. Pierce, Jr., *Administrative Law Treatise* § 1.4, at 11 (5th ed. 2010).

[16] Merrill, 111 Colum. L. Rev. at 952.

[17] *See* Federico, 22 J. Pat. Off. Soc'y at 941.

the record made up in that office, while the circuit court hear[d] the case upon a bill in equity in due course of judicial procedure, not only on the evidence heard by the commissioner of patents and the court of appeals, but upon such additional evidence as either party to the suit may choose to present," "the doctrine of res adjudicata . . . ha[d] no application." *Bernardin*, 77 F. at 852; *see also Rousso v. First Nat'l Bank*, 37 F.2d 281, 283 (6th Cir. 1930); Emerson Stringham, *Patent Interference Equity Suits* § 7951, at 76-77 (1930).

2. *Morgan* has nothing to do with the standard governing admission of evidence in an action under § 145. No party sought to introduce new evidence, so the issue did not arise. To the contrary, the specific mention by the Court that no additional testimony was introduced suggests that such testimony was commonly admitted. And the Court cited and relied on *Butler*, which specifically holds (on the page cited by *Morgan*) that, in an action under § 4915, "the statute contains no provision requiring the case to be heard upon the evidence produced before the commissioner"; "the court may receive new evidence." 21 F. at 327. Nor can *Morgan* be read to adopt a modern judicial review model under § 4915 because that model would not emerge until more than a decade later.[18]

The claim that *Morgan* supports any limitation on the introduction of new evidence in an action under § 145 is particularly untenable because that case was an action between private parties following an interference – and not an action by a disappointed *ex parte* applicant against the Patent Office. Accord-

---

[18] *See* Merrill, 111 Colum. L. Rev. at 953.

ingly, the action was analogous to a modern action under § 146, not § 145. Section 146 – which the government ignores – expressly provides that, while the record before the PTO is admissible, it is "without prejudice to the right of the parties to take further testimony." 35 U.S.C. § 146.[19] It makes no sense to argue that *Morgan* was understood by Congress to suggest any limitation on the introduction of new evidence – because, if it was so understood (and there is no evidence of it), Congress expressly overruled any such limitation in 1927.

3. It was against this backdrop of settled judicial interpretation of § 4915 that Congress, in 1927, recodified the provision for a bill in equity to challenge a patent rejection. Under the new statute, an applicant was given a choice between challenging the Patent Office decision on direct appeal or filing a bill in equity.[20] The law otherwise preserved the existing provision for a bill in equity in *ex parte* rejections.

By re-enacting a provision for a "bill in equity" in light of decades of precedent interpreting that provision to allow for the introduction of new evidence in a *de novo* proceeding before a court of original jurisdic-

---

[19] The wording of § 146, which was added to R.S. § 4915 in 1927, *see infra* n.20, reflects the uncertainty that existed prior to 1927 concerning the admissibility of the record before the Patent Office in a suit between private parties. Congress also clarified that parties were nevertheless free to introduce new evidence in such an action.

[20] *See* Act of Mar. 2, 1927, ch. 273, § 11, 44 Stat. 1335, 1336-37 (amending § 4915). An initial draft of what became the 1927 statute would have eliminated the direct appeal altogether while preserving the bill in equity. *See To Amend Section 52 of Judicial Code and Other Statutes Affecting Procedure in the Patent Office: Hearing Before the H. Comm. on Patents*, 69th Cong. 7-8 (1926) ("House Hr'g").

tion, Congress incorporated that settled interpretation into the revised provision. *See Forest Grove Sch. Dist. v. T.A.*, 129 S. Ct. 2484, 2492 (2009) ("'Congress is presumed to be aware of . . . judicial interpretation of a statute and to adopt that interpretation when it re-enacts a statute without change.'") (quoting *Lorillard v. Pons*, 434 U.S. 575, 580 (1978)); *Bragdon v. Abbott*, 524 U.S. 624, 645 (1998) (when "judicial interpretations have settled the meaning of an existing statutory provision, repetition of the same language in a new statute indicates, as a general matter, the intent to incorporate its . . . judicial interpretations as well"); *Merrill Lynch*, 456 U.S. at 378-79. Congress thus must be understood to have intended to continue to allow plaintiffs under this provision to introduce new evidence in accordance with ordinary equity practice. *See Hoover*, 325 U.S. at 87 (holding that 1927 statute "sav[ed] to litigants the option of producing new evidence in a court, by retaining the equity procedure").

The legislative hearings that led up to the adoption of the 1927 revision drive the point home. Henry Huxley, a member of the American Bar Association ("ABA") committee that had drafted the 1927 bill, explained that, in *ex parte* cases, a patent applicant could "start a suit in equity and have a real trial" to obtain a patent.[21] Charles Howson, the chairman of the ABA Committee on Patent Law Revision, testified:

---

[21] House Hr'g 9; *see also id.* at 13 ("Mr. Barnett: Will you point out how, in the original suit, the inventor would be allowed to strengthen his case? Mr. Huxley: He could take testimony and bring out all the facts pertinent and have an absolutely full hearing in the matter, and if he does not get justice from the Patent Office he could get it from the courts.").

> Section 4915 has always been regarded by the patent bar, or those experienced in patent practice, as the final check on the Patent Office to enable a deserving inventor to get his just deserts if everything else fails. The advantage of section 4915 is that it enables the party in interest, desiring to obtain a patent to take evidence in a court or tribunal whose business it is to try issues of facts and make up a record in addition to that he has been enabled to furnish the examiners in the Patent Office, and therefore get before a court of competent jurisdiction everything connected with his rights and every fact connected with his patent[.][22]

In the Senate hearing, testifying in support of the bill, Patent Commissioner Thomas Robertson testified that "a suit in equity under Section 4915 of the Revised Statutes" allowed a patent applicant to "start de novo and litigate the matter through the courts."[23]

4. The 1952 Act, though it substitutes the modern term "civil action" for the term "bill in equity," otherwise preserves the critical language from the

---

[22] House Hr'g 20-21; *see also id.* at 32 (testimony of Otto Barnett, American Patent Law Ass'n President: under § 4915, patent applicant "demonstrates to the court by the production of evidence . . . in such a way that an appeal on the same record that was in the Patent Office would not permit").

[23] *Procedure in the Patent Office: Hearing Before the S. Comm. on Patents*, 69th Cong. 7 (1926). Contemporary treatises clearly expressed the same understanding. *See* Albert H. Walker, *The Law of Patents* § 134, at 159 (5th ed. 1917) ("[i]n order to decide the issues of such a bill in equity [under § 4915], the court . . . will take testimony, and any other admissible evidence, according to the course of courts in equity"); 2 William C. Robinson, *The Law of Patents* § 571, at 188-89 & n.2 (1890).

1927 statute, indicating that (as the Senate Report noted) the recodification made "no fundamental change" in the available remedy.[24] S. Rep. No. 82-1979, at 7 (1952).[25] Nevertheless, the government argues (at 34-37) that the cases decided under § 4915 between 1927 and 1952 sharply restricted the introduction of new evidence in such cases and that Congress intended to incorporate that new understanding. But the only case of this Court under § 4915 decided between 1927 and 1952 – which, like this case, involved a direct challenge to an *ex parte* denial

---

[24] The late Judge Giles Rich, meticulous even as a law student, wrote in his 1929 paper on patent procedure that the "obvious difference between the regular bill and this bill in equity [under the 1927 version of § 4915] is that in the former the case is heard on the record from the Patent Office, where in the latter new evidence may be introduced." *See* Giles S. Rich, *Outline of Patent Law and Procedure*, 3 J. Fed. Cir. Hist. Soc'y 61, 78 (2009). Judge Rich was one of the principal drafters of the 1952 Act; P.J. Federico – who shared Judge Rich's understanding of the scope of the bill in equity – was the other. *See* Federico, 22 J. Pat. Off. Soc'y at 935. *Cf. Microsoft*, 131 S. Ct. at 2243 (citing views of Judge Rich, "a principal drafter of the 1952 Act").

[25] The government argues (at 38-39) that the enactment of the APA several years before the 1952 recodification somehow suggests that Congress understood the pre-1952 rule regarding introduction of new evidence to be consistent with the APA standard. In fact, as the then-Commissioner of Patents observed, Patent Office adjudications were understood from the beginning to be exempt from § 5 of the new APA precisely because those adjudications were "subject to subsequent trial of the law and the facts *de novo* in . . . court" – this is, under § 4915. Casper W. Ooms, *The United States Patent Office and the Administrative Procedure Act*, 38 Trademark Rep. 149, 150 (1948) (internal quotations omitted). With particular reference to judicial review under the APA, Commissioner Ooms observed that "[a]n optional trial *de novo* is available under the Patent statute for each final adjudication refusing a patent." *Id.* at 159.

on written-description grounds in a suit against the head of the Patent Office, a suit in which substantial new evidence was admitted – reaffirmed *Butterworth* without qualification, noting that § 4915 affords "a formal trial . . . on proof which may include evidence not presented in the Patent Office." *Hoover*, 325 U.S. at 83. If the 1952 Congress that enacted the Patent Act was looking anywhere, it had to look at that authoritative 1945 decision of this Court. Moreover, none of the lower-court cases decided prior to 1952 articulated or applied the government's "no reasonable opportunity" standard or, indeed, any uniform standard restricting the introduction of new evidence – as the government admits. *See* Pet'r Br. 35 n.8 (conceding that the "consensus" was "not unanimous"). Congress could not have "implicitly adopted the different approaches various courts took with regard to an admissibility standard." App. 19a; *see* U.S. Br. at 18 n.4, *Microsoft Corp. v. i4i L.P.*, No. 10-290 (U.S. filed Mar. 18, 2011) ("Congress's inaction . . . raises no inference that it acquiesced in any particular standard . . . because there was no clear consensus among the courts of appeals.").

In most of the cases that the government cites, the courts admitted and considered (or, in one case, considered without formally admitting) proffered evidence.[26] *Barrett Co. v. Koppers Co.*, 22 F.2d 395 (3d

---

[26] *See Schilling v. Schwitzer-Cummins Co.*, 142 F.2d 82, 85 (D.C. Cir. 1944) (affirming district court "after a careful examination of the record – including the disputed evidence"); *Boucher Inventions v. Sola Elec. Co.*, 131 F.2d 225, 227 (D.C. Cir. 1942); *see also id.* at 229 (Stephens, J., dissenting) (noting that, where plaintiff had acted without any "intention of concealment," district court properly admitted new evidence, and that "[p]roceedings under [§] 4915 are de novo"); *Globe-Union, Inc. v. Chicago Tel. Supply Co.*, 103 F.2d 722, 728 (7th Cir. 1939)

Cir. 1927), represents the furthest that any court of appeals went in sanctioning the exclusion of evidence not proffered to the Patent Office, and it based its holding squarely on traditional notions of equitable estoppel. *See id.* at 396.[27] Later courts properly read *Barrett* to hold narrowly that it was the deliberate suppression of evidence and the attempt to maintain a factual position in a subsequent action different from the position before the PTO that gave rise to an estoppel.[28] The Third Circuit itself rejected attempts

---

(rejecting defendant's argument that "additional evidence taken in the district court should have been disregarded on the ground that it was available to the Patent Office"); *Greene v. Beidler*, 58 F.2d 207, 208-09 (2d Cir. 1932) (finding admitted evidence to be incredible in light of discrepancies between trial testimony and prior testimony before Patent Office).

[27] In *Barrett*, the plaintiff had, during the interference proceeding before the Patent Office, "expressly refused to disclose and to allow [its] witnesses to answer questions which would disclose subsequent commercial practices." 22 F.2d at 396. In court, the plaintiff sought to introduce "evidence of commercial practices to show actual reduction to practice through the year 1917 following the laboratory experiments of 1916 and for a year before [the defendant's] claimed date, *the very subject-matter concerning which, at the interference hearings, witnesses for the [plaintiff's] application were asked questions and the [plaintiff] forbade them to answer.*" *Id.* (emphasis added). The district court held that the Barrett Company was "estopped to present this evidence," and the court of appeals affirmed. *Id.*

[28] *See Nichols v. Minnesota Mining & Mfg. Co.*, 109 F.2d 162, 166-67 (4th Cir. 1940) (reading *Barrett* to hold that "a party may estop himself from offering testimony in a suit instituted under R.S. § 4915 by intentionally withholding it in the proceedings in the Patent Office"); *Globe-Union*, 103 F.2d at 728 ("The Barrett case stands on facts clearly showing intentional withholding of evidence. . . . We must always be conscious of the distinction between a de novo trial, where the case is tried a second time and the record is made up in the district court, and [the] court's review of findings of an administrative body, where

to over-read *Barrett*, holding that to exclude evidence simply because it was "available to the plaintiffs at the time of the proceedings in the Patent Office" "would be to change the nature of a[] [§] 4915 proceeding and to rewrite the statute." *Minnesota Mining & Mfg. Co. v. Carborundum Co.*, 155 F.2d 746, 748 (3d Cir. 1946).[29] Pre-1952, pre-*Hoover* lower-

---

the record is solely that of the administrative body. The instant case falls in the former class."); *Dowling v. Jones*, 67 F.2d 537, 538 (2d Cir. 1933) (L. Hand, J.) (noting that *Barrett* involved evidence "which the inventor had *deliberately suppressed*" and that "it does not follow that it would have extended the doctrine to evidence not *suppressed*, but merely *neglected* through the plaintiff's slackness in preparation") (emphases added); *Wright v. Runge*, 31 F. Supp. 844, 845 (D.D.C. 1939) ("It may well be that the plaintiff might be estopped from offering testimony here that he had suppressed in the Patent Office, but the mere failure to exercise the highest degree of diligence in producing evidence before the Patent Office would not . . . prevent its introduction here."); *see also Smith v. Prutton*, 127 F.2d 79, 81 (6th Cir. 1942) ("[t]he statute . . . gives the litigants permission to present the case anew to the District Court after it has been finally closed in the Patent Office, and imposes upon the District Judge the obligation of hearing the evidence and determining the issue").

[29] The government cites a single district court case in which the court ruled evidence inadmissible on the stated ground that "there was no showing that the evidence sought to be introduced was not available to the plaintiffs at the time of taking testimony in the Patent Office in the interference proceedings." *Etten v. Kauffman*, 32 F. Supp. 186, 187 (W.D. Pa. 1940), *aff'd*, 121 F.2d 137 (3d Cir. 1941); *see also Schering Corp. v. Marzall*, 101 F. Supp. 571, 573 (D.D.C. 1951) (considering proffered evidence and ruling "it is clearly insufficient"); *O'Donnell v. United Shoe Mach. Corp.*, 2 F. Supp. 178, 181 (D. Mass. 1933) (new evidence admitted). An isolated district court decision provides no basis for inferring that Congress intended to modify the longstanding understanding of the remedy provided under § 145's predecessors. *See, e.g., Rodriguez v. Compass Shipping*

court cases thus cannot support the government's view of § 145.[30]

C. The Introduction of Evidence Under § 145 Is Supported by Important Institutional Considerations

1. Congress's determination to retain the civil action to obtain a patent under § 145 – as an alternative to an APA-type on-the-record appeal, *see* 35 U.S.C. §§ 141-144, *Zurko*, 527 U.S. at 154 – reflects a sensible accommodation of the distinct institutional attributes of the PTO and generalist courts. As explained below, non-technical judges require evidence to provide background knowledge that an expert PTO examiner already has; submission of unnecessary evidence puts a burden on an already overburdened PTO; and the PTO often articulates new grounds of decision at a point when the applicant lacks a fair opportunity to respond – as it did here.

First, patent examiners are expected to have expertise in their particular fields, while district courts lack such background technical knowledge. To permit informed fact-finding by a district court therefore requires presentation of evidence concerning the subject matter of the application and (for example)

Co., 451 U.S. 596, 615-16 & n.36 (1981); *United States v. Welden*, 377 U.S. 95, 102 n.12 (1964).

[30] When Congress amended the patent laws in 1980 to provide for the current *ex parte* reexamination procedure codified in 35 U.S.C. § 306, *see* Act of Dec. 12, 1980, Pub. L. No. 96-517, § 1, 94 Stat. 3015, 3016, it "grant[ed] a patent owner the right to pursue the same appeal routes available to patent applicants." H.R. Rep. No. 96-1307(I), at 7 (1980). The Committee Report accompanying the legislation noted that, under that provision, "[a]dverse final decisions . . . could be appealed . . . *or de novo review of the reexamination decision could be sought*" in district court. *Id.* at 8 (emphasis added).

the knowledge of a person of ordinary skill in the relevant art – a matter that would be relevant to factual and legal issues bearing on patentability, including obviousness and (as in this case) written description. This case provides an illustration: the principal purpose of plaintiff's declaration was to establish the factual basis for arguments that a person of ordinary skill in the art would have found a description of the claimed invention in the specification.[31] Plaintiff could reasonably have judged that such detailed exposition would not be necessary in the PTO and that pointing the patent examiner (and the Board) to the relevant portions of the disclosure – in a highly structured specification, *see supra* n.4 – would suffice. Even if plaintiff "could" have presented this exposition to the PTO, he acted quite reasonably – he was anything but "without cause" (to use one of the government's standards, Pet'r Br. 34) – in not doing so.

Second, as a result of the nearly overwhelming volume of applications filed each year, patent examiners are constrained to devote relatively little time to the examination of each application. *See generally* Mark A. Lemley, *Rational Ignorance at the Patent Office*, 95 Nw. U. L. Rev. 1495, 1500 (2001). A rule

---

[31] One group of *amici* argues that the written-description requirement is an issue of law and that the substance of plaintiff's declaration should have been considered by the district court as legal argument. *See* Verizon *et al.* Br. 4-17. The court reviews legal issues *de novo* – without deference to the PTO's interpretation of the statute's patentability requirements. *See, e.g., Markman v. Westview Instruments, Inc.*, 517 U.S. 370 (1996). Accordingly, that argument would, if accepted by this Court, require affirmance of the judgment below and a remand to the district court for consideration of the written-description issue under the correct standard.

that requires applicants to submit all evidence that might later prove to be relevant would place unfair burdens on patent applicants who would face an obligation to develop and to submit evidence in the PTO directed at later district court proceedings, not at the reasonable needs of the PTO itself. And the rule would further over-burden patent examiners, who would be confronted with evidentiary submissions that would "strain[] the agency's examining resources and directly contribute[] to the backlog" in patent applications. *Therasense*, 649 F.3d at 1289-90 (quoting ABA white paper); *see* IPOA Br. 12.

Third, because of the necessarily limited time that an examiner can devote to each application, office actions (as examiner's decisions are called) may do only a poor job of identifying the reasons of a rejection, making a focused response difficult. *See* IEEE-USA Br. 11. This case again provides an illustration: the examiner identified broad features of the patent claims for which written description was said to be lacking (among many other supposed defects, all of which the Board subsequently reversed). After the Board provided the explanation for the written-description rejections that the examiner failed to provide, plaintiff tried to respond, but the Board refused to consider his rehearing request, directed at the new explanation provided in the Board opinion. While this action was itself improper and would have provided a basis for reversal of the Board on appeal,[32] plaintiff could not, in an appeal, obtain an adjudication on new evidence. Section 145 – which

---

[32] *See In re Stepan Co.*, No. 2010-1261, 2011 WL 4582488 (Fed. Cir. Oct. 5, 2011); *In re Leithem*, No. 2011-1030, 2011 WL 4351585 (Fed. Cir. Sept. 19, 2011); *In re Kumar*, 418 F.3d 1361 (Fed. Cir. 2005).

Congress enacted and maintained precisely to afford applicants an opportunity to present evidence not before the Board – should provide a remedy.[33]

2. There is no realistic basis for the argument that a rule allowing new evidence under § 145 will encourage applicants to withhold evidence from the PTO in the hope of a more favorable forum in court. *Cf.* Pet'r Br. 29-30. Irrespective of the opportunity to present additional evidence later, applicants always have an incentive to present their best case to the PTO: any appeal is expensive, and an action under § 145 is even more so because a plaintiff under § 145 must pay the costs of the proceeding – even if the plaintiff prevails.[34] Expert witness testimony – which is rare before the PTO but often needed in district court – further inflates the applicant's financial burden. As *amici* explain, it would be contrary to an applicant's interest to fail to put the best possible case before the PTO to overcome a rejection. *See*

---

[33] As the Federal Circuit recently observed in explaining the importance of additional evidence in a proceeding under § 146, a district court also has an advantage over the Board because of the "inherent limits to [the Board's] fact finding function that arise from the sterile nature of a proceeding that is limited to documentary and declaration or deposition evidence." *Streck, Inc. v. Research & Diagnostic Sys., Inc.*, No. 2011-1045, 2011 WL 4978510, at *4 (Fed. Cir. Oct. 20, 2011). The fact-finding procedures in *ex parte* proceedings are even more restricted.

[34] Furthermore, an applicant may frequently be able to address any evidentiary deficiency through a request for continued examination or a continuation application. *See* Pet. 3. Those remedies make district court litigation even more unlikely. Those remedies were not available to plaintiff, however, because his application was filed before June 8, 1995, claiming benefit of a 1984 application, *see* 37 C.F.R. § 1.114(e)(2), and because, if plaintiff had filed a continuation application, any issued patent would have expired in 2004.

AIPLA Br. 23-25; IPOA Br. 10-11; NYIPLA Br. 22. A nearly unanimous Federal Circuit, including judges with long experience dealing with the patent system, rightly concluded that "[a]n applicant has every incentive to provide the Patent Office with the best evidence in its possession, to obtain a patent as quickly and inexpensively as possible." App. 33a.

Any supposed temptation that an applicant might otherwise have to withhold evidence before the PTO is further counterbalanced by the general risk that the district court will rule against the applicant. An applicant has every incentive to get a favorable decision from the PTO in the first instance and not to rely on § 145 litigation. Here, the evidence that plaintiff sought to introduce simply provided – in response to grounds given for the first time in the Board decision – further explanation of what was already before the PTO, that is, the patent disclosure, in terms more understandable to the non-technical district court. Plaintiff did his best to submit additional argument responding to the new grounds of decision articulated in the Board's decision, but the Board dismissed his request for rehearing.[35] There can be no question of any sandbagging.

It has long been the understanding of the patent bar that new evidence is generally admissible in actions under § 145. *See* AIPLA Br. 15 (explaining that adopting government's position would "'disrupt the settled expectations of the inventing community'")

---

[35] Moreover, plaintiff's opportunity to introduce affidavit or declaration evidence to the PTO was limited, both before and after a final action, and did not include the opportunity to submit such evidence in response to the written-description rejections now on appeal. *See* 37 C.F.R. § 1.132 (1997) (limiting grounds for submission of affidavits and declarations).

(quoting *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 535 U.S. 722, 739 (2002)). The most-cited treatise advises that, "[u]nlike the 'on-the-record' review by direct appeal to the Federal Circuit, the civil action is a *de novo* proceeding. The PTO record is admissible evidence, but both the applicant and the PTO may offer additional evidence." 4 Donald S. Chisum, *Chisum on Patents* § 11.06[3][c][ii] (2005) (footnotes omitted). Yet the government points to no recent cases – and few of any vintage – in which an applicant attempted to withhold evidence in the way that the government claims the statute invites. That is sufficient reason to reject the government's purported concern.

II. THE DISTRICT COURT DETERMINES FACTUAL ISSUES ON A NEW RECORD BY A PREPONDERANCE OF THE EVIDENCE

A. When new evidence is admitted in an action under § 145, the "presence of such new or different evidence makes a factfinder of the district judge." *Zurko*, 527 U.S. at 164. The text and history of the statute make clear that such district court "factfinding" is *de novo* in the sense that the district court does not evaluate whether the PTO's decision is supported by substantial evidence, but instead decides factual issues "upon the whole merits" based on the new record. *Butterworth*, 112 U.S. at 61. The Federal Circuit has consistently held that, when new evidence is introduced, PTO factual determinations are not entitled to deference. *See Fregeau*, 776 F.2d at 1038; *see also* AIPLA Br. 30-31. And the burden that the plaintiff bears is the preponderance-of-the-evidence standard that applies in any civil litigation in the absence of a clear basis – in the statute or in

established common-law practice – for a different, heightened standard.

The government does not (and cannot, in light of this Court's statement in *Zurko*) argue that the APA "substantial evidence" standard applies to such factual issues. That concession reflects the fact that, in circumstances where new evidence is admitted the district court is necessarily ruling on a new evidentiary record. Instead, the government urges the Court to adopt, under § 145, a heightened standard of proof – which the government dubs the "thorough conviction" standard (Pet'r Br. 44-45) – analogous to the burden that applies in litigation between private parties, where the *invalidity* of an issued patent must be established by clear and convincing evidence. *See Microsoft*, 131 S. Ct. at 2247. But this Court's construction of 35 U.S.C. § 282's "presumed valid" language in *Microsoft* was based on the Court's "authoritative" pre-1952 precedent recognizing that an infringer was required at common law to meet a heightened standard of proof to demonstrate patent invalidity. *See* 131 S. Ct. at 2245-51. That rationale does not apply here, because there is no such authoritative precedent, and no basis in the text, for a heightened standard under § 145. In particular, this Court's decision in *Morgan* – which involved a challenge, without new evidence, to an issued patent following an adjudication in the defendant's favor by the Patent Office – does not support any departure from the ordinary preponderance-of-the-evidence standard for a challenge, with new evidence, to the denial of an *ex parte* application.

1. As discussed above, the language of § 145 is inconsistent with the claim that Congress intended to require deference to the prior fact-finding of the

PTO. *See supra* pp. 16-18. The statute requires the district court to adjudicate the applicant's entitlement to a patent "as the facts in the case may appear," without affording any special weight to the PTO's prior finding. The text includes no language suggesting departure from the default preponderance standard that applies to factual issues in civil actions. This Court has made clear that, at least in civil litigation between private parties, in the absence of a clear contrary indication, Congress does not intend to impose any "special, heightened standard of proof." *Grogan v. Garner*, 498 U.S. 279, 286 (1991). And lower courts have consistently applied the preponderance standard under statutes that provide for review of agency action through a *de novo* trial where new evidence is introduced. *See, e.g., St. Paul Fire & Marine Ins. Co. v. United States*, 6 F.3d 763, 769 (Fed. Cir. 1993); *Warren v. United States*, 932 F.2d 582, 586 (6th Cir. 1991); *Ibrahim v. United States*, 834 F.2d 52, 53-54 (2d Cir. 1987).

The preponderance standard is also consistent with the APA, which does not impose any heightened evidentiary burden in cases where the "reviewing court" takes new evidence and determines factual issues anew. Section 706(2)(F) requires a court to set aside agency findings that are "unwarranted by the facts" where "the facts are subject to trial de novo." 5 U.S.C. § 706(2)(F).[36] We have located no case suggesting that the standard of proof under § 706(2)(F) is anything but preponderance-of-the-evidence. If the APA supplies the standard in a case under § 145

---

[36] As noted above, the Commissioner of Patents, shortly after the adoption of the 1946 APA, reaffirmed the understanding that the action that would become an action under § 145 was a trial *de novo*. *See supra* n.25.

– as it does in cases under §§ 141-144, *see Zurko*, 527 U.S. at 154 – the government must "clear[ly]" establish any departure from that preponderance-of-the-evidence standard. *Id.* at 155. As discussed below, it cannot do so here.

2. This Court's conclusion in *Microsoft* that § 282 imposes a heightened standard of proof on accused infringers challenging the validity of an issued patent does not support the government. The *Microsoft* holding, of course, does not apply: that case involved the application of the statutory presumption of validity of an issued patent in infringement litigation; this case involves a civil action under § 145 following the PTO's denial of plaintiff's application.

Furthermore, this Court's interpretation of § 282 was based on a "presumption of patent validity" that "had long been a fixture of the common law" with a "settled meaning." *Microsoft*, 131 S. Ct. at 2246. The statutory text, referring to patents' being "presumed valid," adopted a common-law term that provided the clear meaning that the statutory text, read in isolation, did not supply. Here, by contrast, the statutory provision is one that has existed, more or less in present form, for 175 years. That text contains no standard-elevating language. It authorizes the court to decide matters of fact "as the facts in the case may appear," and there is no common-law basis for giving that text (or any other) a meaning that departs from the background rule that facts are to be proven by a preponderance of the evidence.

To the contrary, precedent under § 4915 contradicts the "thorough conviction" standard that the government advocates. As noted, the Court in *Butterworth* explained that the district court rules "upon the whole merits," 112 U.S. at 61, which implies fact-

finding by a preponderance of the evidence, not deference. Moreover, there is no indication in any pre-1952 cases involving challenges to *ex parte* denials of patent applications that the courts applied any heightened standard of proof. *See, e.g., Lucke*, 69 F.2d at 383 (reversing findings of Patent Office without any suggestion that heightened standard of proof applied); *Ingersoll v. Holt*, 104 F. 682, 684 (C.C.N.D. Cal. 1900) ("[T]he plaintiff now stands in the position of one applying for an original patent, subject to the ordinary rules of equity practice and procedure."); *see also supra* pp. 25-27 & n.14 (cases establishing that ordinary rules of equity practice and procedure applied in actions under § 4915).[37]

Morgan does not support (much less provide "clear" support for) a heightened evidentiary standard in cases under § 145 at all, let alone in cases involving new evidence. Not only did that case involve no new evidence, but it did not involve the *ex parte* denial situation of § 145. Rather, it followed an interference proceeding – that is, an *inter partes* proceeding to determine priority – and involved a challenge to the validity of the defendant's issued patent. *See also Zurko*, 527 U.S. at 158. The Court's holding was expressly limited to that interference situation: the "rule" that the Court "laid down" was that, "where the question decided in the patent office *is one between contesting parties as to priority of invention*, the decision there made must be accepted as control-

---

[37] We have located a single pre-1952 case in which a court invoked the *Morgan* standard in a case involving an *ex parte* rejection, and that court made clear that it understood the required heightened standard of proof to reflect the fact that the Patent Office finding had already been reviewed in court on direct appeal. *See In re Griswold*, 9 App. D.C. 496 (D.C. Cir. 1896).

ling upon that question of fact in any subsequent suit between the same parties, unless the contrary is established by testimony which in character and amount carries thorough conviction." 153 U.S. at 125 (emphasis added). A civil action under § 145 does not involve any prior adjudication of a dispute between private parties, nor does it involve any challenge to an award of priority or the validity of an issued patent.

The Court's reasoning, like its express ruling, was squarely premised on the fact that the plaintiff was challenging the validity of another's patent. *Id.* at 123. Citing *Coffin v. Ogden*, 85 U.S. (18 Wall.) 120 (1874), and *Cantrell v. Wallick*, 117 U.S. 689 (1886), the Court noted that, in an infringement action, a party seeking to challenge a patent's validity not only would bear "the burden of proof to make good this defense . . . , but it has been held that every reasonable doubt should be resolved against him." *Morgan*, 153 U.S. at 123 (internal quotations omitted). The Court concluded that "[t]hese two cases are closely in point," and it explained why: "[t]he plaintiff in this case, like the defendant in those cases, is challenging the priority awarded by the patent office, and should, we think, be held to as strict proof." *Id.*[38]

The Court further relied on the fact that the suit in question sought to deprive the defendant of property already granted after an adversarial proceeding between two claimants. The Court noted that the Patent Office "determination gave to the defendant

---

[38] This Court in turn relied on *Morgan* when it adopted its "authoritative" formulation of the clear-and-convincing standard for invalidity defenses in *Radio Corp. of America v. Radio Engineering Laboratories, Inc.*, 293 U.S. 1, 5-6, 8 (1934). *Microsoft*, 131 S. Ct. at 2245.

the exclusive rights of a patentee" and that the plaintiff was seeking to take "the rights there awarded to the defendant." *Id.* at 124. The Court thus found the case to be comparable to one involving "a contest between two claimants for land patented by the United States to one of them," in which agency fact-finding would be presumptively final and unreviewable. *Id.* at 124-25. It was for that reason – *i.e.*, that a "special tribunal" had already adjudicated "a controversy between two individuals" resulting in the award of property to one of them – that the suit was treated as "something in the nature of a suit to set aside a judgment" in the defendant's favor. *Id.* at 124.[39]

Neither the "rule" of *Morgan* nor its rationale applies in a case where the PTO has merely denied a patent. In a case under § 145, there is no challenge to the validity of an issued patent, and there is no opposing party defending a property right gained through an adversarial adjudication before the PTO. Still less did *Morgan*, which involved no new evidence and did not invoke any general principle of deference to agency expertise, establish precedent for departing from the ordinary preponderance-of-the-evidence standard in a § 145 case involving new evidence. To the contrary, the Court's solicitude for property rights weighs against imposing any special burdens on a plaintiff under § 145.

---

[39] The Court then cited the page of *Butler v. Shaw* that distinguishes the interference context from the *ex parte* context. *See* 21 F. at 327. Even in the former context, *Butler* emphasizes the plenary nature of the equity court's authority to take new evidence and resolve factual issues anew to decide the question of "the right[s] of . . . the parties to the suit." *Id.*

B. Because the district court refused to consider plaintiff's proffered declaration, there has been no occasion in this case to consider what weight a district court should afford to a prior PTO finding of fact when new evidence is introduced. That issue will necessarily be case-specific. In this case, the PTO's conclusion that plaintiff's claims lacked written-description support is entitled to no weight.

First, the evidence that plaintiff seeks to introduce was not considered by the PTO and bears directly on the issue that the PTO purported to resolve. Even if the government were correct that plaintiff is required to meet a heightened standard of proof under § 145, the fact that new evidence is introduced that was not considered by the PTO would reduce plaintiff's burden. "Simply put, if the PTO did not have all material facts before it, its considered judgment may lose significant force." *Microsoft*, 131 S. Ct. at 2251.

Second, plaintiff did make *available* to the PTO, in his request for rehearing and in response to the new grounds for rejection articulated by the Board, the substance of the evidence proffered in the district court. The PTO's insistence on adhering to its prior decision without even considering plaintiff's responsive submission renders that decision especially suspect. As this Court has held in the judicial-review context, an agency acts arbitrarily when it "fail[s] to consider an important aspect" of the issue before it. *Motor Vehicle Mfrs. Ass'n of United States, Inc. v. State Farm Mut. Auto. Ins. Co.*, 463 U.S. 29, 43 (1983); *see also In re Carter-Mondale Reelection Comm., Inc.*, 642 F.2d 538, 550 (D.C. Cir. 1980) (agency should not "blind itself to materials available to the agency") (Wald, J., concurring in decision to affirm). The Board's refusal to consider plaintiff's

request for rehearing further undermines any argument that its conclusion is entitled to weight.

C. This case does not present the question whether, in cases under § 145 where no new evidence is presented, the district court is limited to reviewing PTO fact-finding under the substantial-evidence standard that applies under § 141. The Federal Circuit has so held, *see Mazzari v. Rogan*, 323 F.3d 1000, 1004 (Fed. Cir. 2003); *see also Fregeau*, 776 F.2d at 1038; and this Court has noted that "an anomaly might exist insofar as [a] district judge does no more than review PTO factfinding" in an action under § 145 if the standard of review were different from the standard that applies in an appeal, *Zurko*, 527 U.S. at 164. Plaintiff has not challenged (and has had no reason in this case to challenge) that rule.[40]

The possibility, however, that a district court might have to apply different standards of proof depending on the evidence submitted with respect to a particular issue poses nothing like the practical problems of judicial administration that the Court noted in *Microsoft*. *See* 131 S. Ct. at 2250. Because an action under § 145 is tried to the court and not to a jury, the difficulties of instructing a lay jury in "a standard of proof that would rise and fall with the facts of each case" would not arise. *Id.* A district judge would likely have no difficulty in separating the factual issues as to which new evidence is relevant and those

---

[40] At the same time, the statutory language would suggest that all issues are reviewed *de novo* (which would not preclude the reviewing court from affording substantial weight to well-supported factual conclusions of the PTO reached on an identical record). *See* App. 36a-43a (Newman, J., concurring in part and dissenting in part); IEEE-USA Br. 4; IPOA Br. 16.

issues that the plaintiff is raising simply on the record below.

D. Any supposed "asymmetry" (Pet'r Br. 28) between the remedies that the statute provides to disappointed patent applicants and those accused of infringing validly issued patents reflects deliberate asymmetry in the statutory scheme. Substantively, the statute provides that an inventor "shall be entitled to a patent unless" certain disqualifying conditions are met, 35 U.S.C. § 102; that statutory provision has been understood to place the burden on the PTO to show that a patent should *not* issue on a duly filed application; where an examiner fails to make out a prima facie case of unpatentability, the patent should issue for that reason. *See In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). Furthermore, once issued, a patent enjoys a statutory presumption of validity (§ 282), which is reinforced by a heightened standard of proof where validity is challenged, *see Microsoft*. These statutory presumptions reflect a judgment that "the Progress of Science and useful Arts" would be harmed if inventors are denied "the exclusive Right to their respective . . . Discoveries." U.S. Const. art. I, § 8, cl. 8.

The statute's procedures for challenging PTO actions in court reflect a similar "asymmetry" in favor of the inventor. In 2010, the PTO granted more than 200,000 patents;[41] for parties "aggrieved" by such issuance – that is, potential infringers – the statute has long been read, at the government's urging, not to permit APA judicial review, but to remit such parties to validity challenges in the context of later infringement litigation (or to the

---

[41] *See* PTO, *Performance and Accountability Report: Fiscal Year 2010*, at 129 (2010) ("PTO Report").

rarely used *inter partes* reexamination proceeding, which may be followed by Federal Circuit review, 35 U.S.C. § 315(b)).[42] By contrast, the Board affirmed or affirmed-in-part rejections of fewer than 5,000 applications in fiscal year 2010.[43] For those applicants, the statute provides two distinct judicial remedies. Moreover, the statute provided those remedies from the earliest years of the patent examination system, in an era when comparable executive action was considered unreviewable by the courts. To preserve the character of the civil action under § 145 is thus the only course consistent with the will of Congress as expressed in the statute.

CONCLUSION

The judgment of the court of appeals should be affirmed.

---

[42] *See* Mem. in Support of Def. PTO's Mot. for J. on the Pleadings and in Opp. to Pls.' Mot. for Summ. J. at 3-4, *Association for Molecular Pathology v. USPTO*, No. 09 Civ. 4515 (RWS) (S.D.N.Y. filed Dec. 24, 2009), 2009 WL 5785024 (citing *Syntex (U.S.A.), Inc. v. USPTO*, 882 F.2d 1570, 1572-74 (Fed. Cir. 1989)).

[43] *See* PTO Report at 138.

Respectfully submitted,

GREGORY L. ROTH
5712 Parkwest Circle
La Palma, California 90623
(714) 723-6871

AARON M. PANNER
Counsel of Record
KELLOGG, HUBER, HANSEN,
TODD, EVANS & FIGEL,
P.L.L.C.
1615 M Street, N.W.
Suite 400
Washington, D.C. 20036
(202) 326-7900
(apanner@khhte.com)

October 31, 2011

REPLY BRIEF

No. 10-1219

In the Supreme Court of the United States

DAVID J. KAPPOS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR, UNITED STATES PATENT AND TRADEMARK OFFICE, PETITIONER

v.

GILBERT P. HYATT

ON WRIT OF CERTIORARI TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

REPLY BRIEF FOR THE PETITIONER

DONALD B. VERRILLI, JR.
Solicitor General
Counsel of Record
Department of Justice
Washington, D.C. 20530-0001
SupremeCtBriefs@usdoj.gov
(202) 514-2217

TABLE OF CONTENTS

Page

I. Consistent with established principles of administrative law, Section 145 is properly construed to limit the circumstances under which the Court may consider evidence not presented to the PTO, and to provide for deferential review of the agency's decision 3
   A. A Section 145 suit is a proceeding for judicial review of agency action 3
   B. New evidence should be admissible in a Section 145 suit only if the plaintiff had no reasonable opportunity to present the evidence to the PTO 6
   C. Under background principles of administrative law, the PTO's decision should be reviewed deferentially in all Section 145 cases 11
II. Congress's reenactment of Section 145 in the 1952 Patent Act should be understood to incorporate the prevailing judicial practice of limiting new evidence and applying a deferential standard of review 16
Conclusion 22

TABLE OF AUTHORITIES

Cases:

Austin v. *Coe*, 69 F.2d 832 (D.C. Cir.), cert. denied, 293 U.S. 561 (1934) 18
Barrett Co. v. *Koppers Co.*, 22 F.2d 395 (3d Cir. 1927) 17, 19

Cases—Continued: Page

Boucher Inventions, Ltd. v. *Sola Elec. Co.*, 131 F.2d 225 (D.C. Cir. 1942), cert. denied, 318 U.S. 770 (1943) 18

Butterworth v. *United States ex rel. Hoe*, 112 U.S. 50 (1884) 20

DeSeversky v. *Brenner*, 424 F.2d 857 (D.C. Cir. 1970) 8

Dickinson v. *Zurko*, 527 U.S. 150 (1999) 3, 5, 13

Fregeau v. *Mossinghoff*, 602 F. Supp. 484 (D.D.C. Sept. 10, 1984), aff'd 776 F.2d 1034 (Fed. Cir. 1985) 7

Gandy v. *Marble*, 122 U.S. 432 (1887) 20

Globe-Union, Inc. v. *Chicago Tel. Supply Co.*, 103 F.2d 722 (7th Cir. 1939) 17, 19

Grogan v. *Garner*, 498 U.S. 279 (1991) 12

Hien, In re, 166 U.S. 432 (1897) 20

Hoover Co. v. *Coe*, 325 U.S. 79 (1945) 3, 21

Hyatt v. *Dudas*, No. 03-0901, 2006 WL 4606037, (D.D.C. Sept. 30, 2006) 8

Lemelson v. *Mossinghoff*, No. 83-0217, 1985 WL 1787, (D.D.C. Mar. 26, 1985) 8

Microsoft Corp. v. *i4i Ltd. P'ship*, 131 S. Ct. 2238 (2011) 12, 14

Morgan v. *Daniels*, 153 U.S. 120 (1894) ..... *passim*

Nichols v. *Minnesota Mining & Mfg. Co.*, 109 F.2d 162 (4th Cir. 1940) 17

Pintarelli v. *Brogan*, 65 F. Supp. 281 (D.R.I. 1946) 8

Radio Corp. of Am. v. *Radio Eng'g Labs., Inc.*, 293 U.S. 1 (1934) 14

Cases—Continued: Page

Robertson v. *Cooper*, 46 F.2d 766 (4th Cir. 1931) 12
Schilling v. *Schwitzer-Cummins Co.*, 142 F.2d 82 (D.C. Cir. 1944) 17, 19
Standard Cap & Seal Corp. v. *Coe*, 124 F.2d 278 (D.C. Cir. 1941) 12
Tagg Bros. & Moorhead v. *United States*, 280 U.S. 420 (1930) 6
Takeda Pharm. Co. v. *Dudas*, 511 F. Supp. 2d 81 (D.D.C. 2007), vacated on other grounds, 561 F.3d 1372 (Fed. Cir. 2009) 7
Therasense, Inc. v. *Becton, Dickinson & Co.*, 649 F.3d 1276 (Fed. Cir. 2011) 11
Velsicol Chem. Corp. v. *Monsanto Co.*, 579 F.2d 1038 (7th Cir. 1978) 18

Statutes, regulations and rule:

Act of Mar. 2, 1927, ch. 273, § 11, 44 Stat. 1336-1337 17
Administrative Procedure Act, 5 U.S.C. 701 *et seq.* 4
5 U.S.C. 706(2)(F) 13
Patent Act of 1952, 35 U.S.C. 1 *et seq.*:
35 U.S.C. 102 15
35 U.S.C. 141 ..... 3, 5, 7
35 U.S.C. 144 3
35 U.S.C. 145 ..... 3, 4, 5, 7, 15
35 U.S.C. 146 12
35 U.S.C. 282 17
15 U.S.C. 1057 7
15 U.S.C. 1071 (2006 & Supp. IV 2010) 7
15 U.S.C. 1119 7

Statutes, regulations and rule—Continued: Page

Rev. Stat. (1878)
§4911 20
§4915 ..... *passim*
37 C.F.R.:
Section 1.2 7
Section 1.192(c)(8)(i)(A) (1998) 10
Section 1.56 11
Section 41.50(b) 10
Section 41.50(b)(1) 10
Fed. R. Civ. P. 2 4

Miscellaneous:

Donald S. Chisum, *Chisum on Patents* § 11.06[3][c][iii] (2005) 8
S. Rep. No. 1979, 82d Cong., 2d Sess. (1952) 16
To Amend Section 52 of the Judicial Code and Other Statutes Affecting Procedure in Patent Office: Hearing on H.R. 6252 and H.R. 7087 Before the House Comm. on Patents, 69th Cong., 1st Sess. (1926) 21

In the Supreme Court of the United States

No. 10-1219

DAVID J. KAPPOS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR, UNITED STATES PATENT AND TRADEMARK OFFICE, PETITIONER

v.

GILBERT P. HYATT

ON WRIT OF CERTIORARI TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

REPLY BRIEF FOR THE PETITIONER

The court of appeals held that an unsuccessful patent applicant may challenge the considered decision of the United States Patent and Trademark Office (PTO) based on evidence that the applicant could have presented to the PTO, and that the applicant may thereby obtain de novo review of any issues to which the new evidence pertains. As the government's opening brief explains, that regime disregards fundamental principles of administrative law, and it undermines the PTO's ability to exercise its expert judgment in determining whether patents should issue.

In defending the Federal Circuit's approach, respondent argues that a Section 145 suit is not an action for judicial review of the PTO's decision. Respondent further con-

tends that, because Section 145 does not wholly preclude the introduction of new evidence, the plaintiff in such a suit may introduce evidence that it failed without cause to present to the agency. When the new evidence "bears directly on the issue that the PTO purported to resolve," respondent asserts that the PTO's decision is "entitled to no weight." Br. 49.

Respondent advocates a striking departure from administrative-review principles that would permit applicants to bypass the PTO in favor of a de novo patentability determination by a non-expert judge. There is no reason to think that Congress, in providing alternate avenues of review of the PTO's decision in Sections 141 and 145, would have provided a choice between deferential on-the-record review and a de novo determination made on new evidence. Respondent's reading of Section 145 would, moreover, create an incentive for applicants to withhold evidence from the PTO, especially when the potential invention is commercially significant. Even when applicants do not intentionally withhold evidence, respondent's approach would reduce the incentive to develop relevant evidence at the administrative stage. And once the PTO has denied the patent, applicants will have every reason to develop new evidence in order to obtain de novo review.

Respondent's proposed textual and historical justifications for this perverse regime lack merit. This Court recognized long ago that actions under Section 145's statutory predecessor, Rev. Stat. § 4915 (1878) (R.S. 4915), involved judicial review of agency determinations. See *Morgan* v. *Daniels*, 153 U.S. 120, 124 (1894). The extent to which new evidence is admissible in a Section 145 suit, and the standard of review under which the PTO's decision should be evaluated, therefore should be determined in light of the background principles that govern review of agency action.

That conclusion is reinforced by courts' early twentieth-century practice of limiting new evidence and applying deferential review in R.S. 4915 suits. When Congress reenacted R.S. 4915 as Section 145 in the 1952 Patent Act, it adopted the predominant judicial understanding that Section 145 should be construed in light of administrative-review principles.

I. CONSISTENT WITH ESTABLISHED PRINCIPLES OF ADMINISTRATIVE LAW, SECTION 145 IS PROPERLY CONSTRUED TO LIMIT THE CIRCUMSTANCES UNDER WHICH THE COURT MAY CONSIDER EVIDENCE NOT PRESENTED TO THE PTO, AND TO PROVIDE FOR DEFERENTIAL REVIEW OF THE AGENCY'S DECISION

A. A Section 145 Suit Is A Proceeding For Judicial Review Of Agency Action

The Patent Act provides two "alternative rights of review" by which to challenge the PTO's decision to deny a patent: a civil action under Section 145, and a direct appeal under Section 141. *Hoover Co.* v. *Coe*, 325 U.S. 79, 83 (1945). While an appeal under Section 141 is limited to the administrative record, 35 U.S.C. 144, Section 145 permits the applicant to "present to the court evidence that the applicant did not present to the PTO." *Dickinson* v. *Zurko*, 527 U.S. 150, 164 (1999). As respondent acknowledges (Br. 23), however, Section 145 does not specify *when* new evidence may be admitted in a Section 145 action. Respondent argues that a Section 145 suit is an independent action to obtain a judicial ruling that a patent should issue, rather than an action for judicial review of the PTO's administrative decision, and that the statute therefore places *no* limits on the admission of new evidence. That characterization of Section 145 is foreclosed by the statutory text and by this Court's decision in *Morgan*.

1. Respondent contends that three aspects of Section 145's text—namely, its references to a "civil action" in which the district court "adjudge[s]" the plaintiff's entitlement to a patent "as the facts in the case may appear" (Br. 16-17)—demonstrate that Section 145 establishes an independent proceeding to obtain a patent. Those textual features will not bear the weight that respondent places on them. The phrase "civil action" without more does not denote an independent proceeding, since that term encompasses all non-criminal suits brought in district court, including suits to review final agency action under the Administrative Procedure Act (APA), 5 U.S.C. 701 *et seq.* See Fed. R. Civ. P. 2; Gov't Br. 19-21. The fact that the court "adjudicate[s]" the plaintiff's challenge (Resp. Br. 18) does not indicate the nature of the adjudication. And even if the court's authority to decide the matter "as the facts in the case may appear" is taken to suggest that the court may sometimes receive additional evidence, it does not shed light on the *extent* to which new evidence is admissible.

Respondent's argument also ignores the strong textual indications that a Section 145 suit is a judicial-review proceeding. The provision appears in the chapter of the Patent Act governing "Review of Patent and Trademark Office Decisions," and it provides a patent applicant who is "dissatisfied with the [PTO's] decision" a "remedy by civil action against the Director" in district court. 35 U.S.C. 145. The "remedy" takes the form of a decision "authoriz[ing] the Director to issue such patent on compliance with the requirements of law"—in effect, a remand to the agency to determine whether the patent should issue. *Ibid.*; Gov't Br. 14-16.

2. Respondent's argument is in any event foreclosed by *Morgan*. There, this Court construed R.S. 4915, which, in language materially identical to current Section 145, autho-

rized a "bill in equity" to have the district court "adjudge that such applicant is entitled * * * to receive a patent * * * as the facts in the case may appear." The Court explained that, because the plaintiff's suit was "an application to the court to set aside the action of one of the executive departments of the government," raising "a question of fact which has once been settled by a special tribunal, entrusted with full power in the premises," the plaintiff was required to prove Patent Office error by more than "a mere preponderance." *Morgan*, 153 U.S. at 124-125. The Court thus made clear that R.S. 4915 provided for judicial review of agency action, and it concluded on that basis that the court in such a suit must give deference to prior agency findings.

Respondent argues that the Court in *Morgan* could not have adopted a "modern judicial review model" because that model did not develop until the early twentieth century. Br. 29. That argument cannot be reconciled with *Morgan*'s express reliance on the Patent Office's delegated authority and expertise as justifying a deferential standard of review. Whenever the modern administrative-review framework may be said to have taken firm root, *Morgan*'s reasoning establishes the decision as an early example of that model. Indeed, this Court highlighted *Morgan*'s administrative-review underpinnings in *Zurko*, 527 U.S. at 159-160, where it relied on *Morgan*'s adoption of a "court/agency review standard" in holding that direct appeals of PTO decisions under Section 141 should be governed by the APA's deferential standards of review.

B. New Evidence Should Be Admissible In A Section 145 Suit Only If The Plaintiff Had No Reasonable Opportunity To Present The Evidence To The PTO

1. Because a Section 145 suit is a proceeding for judicial review of agency action, administrative exhaustion principles should govern the extent to which new evidence is admissible. To be sure, Section 145 does not categorically foreclose new evidence, and it thus reflects a limited exception to the usual rule that judicial review of agency action is limited to the administrative record. Nevertheless, the core justifications for the exhaustion requirement—the recognition that agencies should be afforded an adequate opportunity to consider the full range of relevant evidence and to correct their own errors before judicial review occurs—apply with full force to evidence that a Section 145 plaintiff had a reasonable opportunity to present to the PTO.[1] See Gov't Br. 21-24.

Respondent argues (Br. 21-24) that construing Section 145 to limit new evidence would be inconsistent with the Patent Act's structure because it would render Sections 141 and 145 "essentially equivalent avenues of relief." Respondent is incorrect. The structural inference that Section 145

---

[1] Respondent suggests (Br. 23-24) that, under background administrative-law rules, exhaustion requirements do not limit the introduction of new *evidence* in court so long as the plaintiff presented his substantive *claim* to the agency. But the general rule that review of agency decisions is limited to the administrative record is in substance an exhaustion requirement, and this Court has emphasized that exhaustion principles are particularly important in the context of evidence not presented to the agency. *Tagg Bros. & Moorhead* v. *United States*, 280 U.S. 420, 444-445 (1930). Nor would any sensible purpose be served by requiring Section 145 plaintiffs to pursue administrative appeals as a precondition to judicial review, while allowing them to reserve for court proceedings evidence that ostensibly supports their claims.

sometimes permits the introduction of new evidence (Gov't Br. 18) does not suggest that Section 145 permits such evidence to be introduced *without limitation*. Respondent's argument reflects the implausible premise that Congress provided disappointed applicants with a choice between deferential on-the-record review and an entirely independent action involving a de novo determination made on new evidence by a non-expert court. Construing Section 145 as a safety-valve proceeding that allows new evidence when consistent with administrative-exhaustion principles (*i.e.*, when the evidence could not reasonably have been presented to the agency) therefore best harmonizes Sections 141 and 145. That approach gives effect to both provisions while ensuring that, as alternate avenues for judicial review of the same PTO action, they retain a familial resemblance.[2]

Contrary to respondent's suggestion (Br. 22-23), this approach would give meaningful practical effect to Congress's decision to permit new evidence in Section 145 actions. Some types of evidence, such as oral testimony, cannot be presented to the PTO. 37 C.F.R. 1.2. Section 145 would ordinarily allow a disappointed patent applicant to present oral testimony in order to expand on affidavits that were before the PTO, or to respond to the PTO's credibility determinations. See, *e.g.*, *Fregeau* v. *Mossinghoff*, 602 F. Supp. 484, 488 (D.D.C. 1984), aff'd, 776 F.2d 1034 (Fed. Cir.

---

[2] Respondent argues (Br. 18 n.8) that courts have admitted new evidence in challenges to the PTO's decisions concerning trademark registration under 15 U.S.C. 1071 (2006 & Supp. IV 2010), but these decisions did not consider the existence of limits on admitting new evidence. The statutory framework governing trademarks, moreover, differs from the patent framework in a number of respects. For example, trademark registration provides only prima facie evidence of validity, and in "any action involving a registered mark," the court may order cancellation or restoration of the mark. 15 U.S.C. 1057(b) and 1119.

1985); *Pintarelli* v. *Brogan*, 65 F. Supp. 281, 283-284 (D.R.I. 1946). In addition, Section 145 permits new evidence—such as experiments, data, or studies—that came into existence after the record before the PTO had closed. The provision also provides a backstop when applicants are reasonably unaware of or unable to obtain evidence during the examination process. See, *e.g.*, *Takeda Pharm. Co.* v. *Dudas*, 511 F. Supp. 2d 81, 86-87 (D.D.C. 2007) (expert testimony on later-discovered patents), vacated on other grounds, 561 F.3d 1372 (Fed. Cir. 2009); *Lemelson* v. *Mossinghoff*, No. 83-0217, 1985 WL 1787, at *1 (D.D.C. Mar. 26, 1985) (sales evidence).

In applying this standard, the district court is well-positioned to determine whether the applicant lacked a reasonable opportunity to present the evidence in question during the PTO's proceedings. Indeed, district courts have long been doing just that. The D.C. Circuit employed the reasonable-opportunity standard when it heard appeals in Section 145 actions before the Federal Circuit's creation, *DeSeversky* v. *Brenner*, 424 F.2d 857, 858-859 & n.5 (D.C. Cir. 1970), and district courts have continued to limit new evidence, primarily employing the reasonable-opportunity standard.[3] See, *e.g.*, *Hyatt* v. *Dudas*, No. 03-0901, 2006 WL 4606037, at *1-*3 (D.D.C. Sept. 30, 2006). And although respondent's amicus suggests that limiting new evidence in this manner will occasion protracted collateral litigation into the reasonableness of the applicant's conduct, American Intellectual Prop. L. Ass'n Amicus Br. 12-14 (AILPA), that has not been the case in practice. See, *e.g.*, *Hyatt*, *supra*; Pet. App. 180a-189a.

---

[3] Amicus AIPLA is therefore incorrect in arguing (Br. 15-18) that the government's proposed rule would disrupt settled expectations. See 4 Donald S. Chisum, *Chisum on Patents* § 11.06[3][c][iii], at 11-625 to 11-627 (2005).

3. Respondent contends (Br. 37-42) that "institutional considerations" support a rule that new evidence may be admitted without limitation in Section 145 proceedings. Respondent is incorrect.

First, the possibility that a disappointed applicant may wish to introduce background materials for the benefit of a non-expert judge (Resp. Br. 37-38) does not justify respondent's proposed rule, which permits introduction of *all* new evidence that is material to patentability. This case is a prime example. Although respondent now attempts to characterize his declaration as nothing more than a background document for the judge's benefit, the examiner was unable to find support for the claims despite his expertise, and respondent's declaration would have been directly relevant to the examiner's concerns.

Second, respondent argues (Br. 39-40) that requiring applicants to submit all relevant evidence to the PTO would overburden applicants and examiners. It is a basic principle of administrative law, however, that applicants before an agency may ordinarily be expected to present to the agency all relevant evidence that they would later want a reviewing court to consider. To the extent that the applicant is reasonably unable to present such evidence, Section 145 provides an opportunity, not available in other administrative contexts, to have the reviewing court consider the evidence. The possibility that particular evidence could be useful to a court but unhelpful to the examiner cannot justify denying the examiner the opportunity to determine in the first instance what information he considers probative, and the PTO is in any event in a better position than respondent to assess that institutional concern.

Third, respondent contends (Br. 38-39) that the examiner's rejection in this case did not adequately explain the examiner's rationale, and that the Board's decision con-

tained additional reasoning that respondent could rebut only by introducing new evidence. Respondent was on notice, however, that the examiner was unable to find support for the claims, and that PTO rules required respondent to explain on appeal how the specification "[d]escribe[d] the subject matter defined by each of the rejected claims." 37 C.F.R. 1.192(c)(8)(i)(A) (1998). More generally, applicants have multiple opportunities during the examination process to present additional evidence in response to the examiner's concerns. Gov't Br. 42-43 & n.13. And when the Board's decision is based on a "new ground of rejection," 37 C.F.R. 41.50(b), PTO rules allow the applicant to reopen prosecution and submit new evidence, 37 C.F.R. 41.50(b)(1).[4]

Finally, respondent argues that applicants already have ample incentive to present all their evidence to the PTO in order to maximize their chances of success and avoid the expense of a Section 145 action. Br. 40-42; see AIPLA Am. Br. 23-25. The existence of such incentives does not distinguish disappointed patent applicants from plaintiffs who challenge other types of agency action, yet those incentives are routinely supplemented by rules requiring exhaustion and timely presentation of evidence. In any event, applicants would have the strongest incentive to withhold evidence in those "cases where the patent is commercially significant and the costs of a separate proceeding can be justified"—yet those are the cases in which "PTO review is most important." Pet. App. 79a-80a (Dyk, J., joined by

---

[4] Respondent suggests (Br. 1-7) that he diligently prosecuted his application. In denying respondent's rehearing request, however, the Board determined that respondent had failed without cause to comply with the PTO's evidence-presentation rules. Pet. App. 256a-258a. The district court agreed. *Id.* at 182a-190a; see 138a-141a. The PTO was entitled to enforce its rules to ensure the orderly conduct of its examination process.

Gajarsa, J., dissenting). And once the PTO has denied a patent, *all* applicants—even those who did not purposefully withhold evidence—would have every reason to develop new evidence to obtain de novo review and increase the likelihood of overturning the PTO's decision.[5]

C. Under Background Principles Of Administrative Law, The PTO's Decision Should Be Reviewed Deferentially In All Section 145 Cases

Respondent contends that when "the evidence that plaintiff seeks to introduce was not considered by the PTO and bears directly on the issue that the PTO purported to resolve," the agency's determination is "entitled to no weight." Br. 49. That startling proposition is contrary to well-established administrative-law principles counseling judicial deference to agency authority and expertise. Gov't Br. 25-30.

1. Respondent argues (Br. 43-44) that Section 145's text—in particular, its directive that the court should decide the suit "as the facts in the case may appear"—establishes that the court reviews the PTO's decision de novo when new evidence is introduced. In *Morgan*, however, this Court considered R.S. 4915's materially identical language and held that the Patent Office's decision could be overturned only if the plaintiff established error "by testimony which in character and amount carries thorough con-

---

[5] Amicus Intellectual Prop. Owners Ass'n (IPOA) argues (Br. 10-12) that limiting new evidence is unnecessary because PTO rules impose a duty of candor. See 37 C.F.R. 1.56. That duty applies only to evidence that an invention is *not* patentable. Contrary to IPOA's argument, the doctrine of inequitable conduct, which bars patent enforcement when the applicant has intentionally withheld from the PTO material evidence that the invention is not patentable, creates no incentive to present evidence that the invention *is* patentable. See *Therasense, Inc.* v. *Becton, Dickinson & Co.*, 649 F.3d 1276, 1289-1290 (Fed. Cir. 2011).

viction." 153 U.S. at 125. *Morgan* thus forecloses any argument that the statutory text imposes de novo review in all cases, and there is no basis in the text for a bifurcated standard. See p. 13, *infra*.

Respondent argues (Br. 46-47) that the rule announced in *Morgan* applied only to R.S. 4915 actions challenging Patent Office priority determinations, which are now reviewable under 35 U.S.C. 146. When *Morgan* was decided, however, R.S. 4915 encompassed challenges to both ex parte patent denials and priority decisions, and the Court did not suggest that its requirement of deferential review was limited to the latter context. Rather, in explaining why a deferential standard should apply, the Court emphasized that the plaintiff in a R.S. 4915 action seeks to overturn the decision of an agency, made within its delegated authority and expertise. *Morgan*, 153 U.S. at 124. That rationale is equally implicated by suits challenging ex parte patent denials. And, contrary to respondent's assertion (Br. 46), courts applied *Morgan*'s deferential standard in ex parte cases as well as interferences. See, *e.g.*, *Standard Cap & Seal Corp.* v. *Coe*, 124 F.2d 278, 282 & n.16 (D.C. Cir. 1941); *Robertson* v. *Cooper*, 46 F.2d 766, 768 (4th Cir. 1931).

Respondent also argues that, in the absence of a clear textual directive to apply a deferential standard, courts should not impose a heightened burden on Section 145 plaintiffs. Br. 44 (citing *Grogan* v. *Garner*, 498 U.S. 279 (1991)). Respondent thus urges the Court to apply the default preponderance standard that typically applies when the plaintiff does not challenge an agency's decision. That default rule is not relevant here, because Section 145 has long been understood to authorize judicial review of agency action. Cf. *Microsoft Corp.* v. *i4i Ltd. P'ship*, 131 S. Ct. 2238, 2244-2245 (2011). Nor does Section 706(2)(F) of the

APA, which provides that the reviewing court may set aside agency action that is "unwarranted by the facts to the extent that the facts are subject to trial de novo by the reviewing court," provide any guidance. 5 U.S.C. 706(2)(F). The "extent" to which "the facts are subject to trial de novo" is the disputed question here.

Finally, respondent's discussion (Br. 50-51) of the appropriate standard of review when a Section 145 plaintiff does *not* present new evidence further demonstrates the weakness in his position. When a Section 145 plaintiff presents no new evidence, *Morgan*—which concerned an R.S. 4915 action with no new evidence—requires deferential review. 153 U.S. at 125. The Federal Circuit accordingly held (and respondent previously agreed, see Br. in Opp. 18) that the court in such a suit reviews PTO factfindings under the APA's "substantial evidence" standard. Pet. App. 23a; see *Zurko*, 527 U.S. at 164. Under that view, however, Section 145 provides for sharply different standards depending on whether new evidence is admitted, even though the text provides no basis for a variable standard. Respondent has now changed tack, suggesting that Section 145 is best viewed to mandate that "all issues are reviewed de novo" even when no new evidence is presented. Br. 50 & n.40. Such an approach would be inconsistent with *Morgan* and would reflect a striking departure from administrative-law principles. There is no evident policy justification, moreover, for giving applicants who wish to challenge the PTO's decision on the administrative record a choice between traditional substantial evidence review under Section 141 and de novo review under Section 145.

2. As the government explained in its opening brief (at 28), reviewing de novo all issues on which new evidence is introduced would create an unjustified disparity between judicial review of patent grants and review of patent deni-

als. This Court held in *Microsoft* that when a party challenging a patent's validity in the context of an infringement suit relies on evidence not considered by the PTO, the statutory presumption that a patent is valid remains in effect, but the new evidence "may carry more weight" in the analysis. 131 S. Ct. at 2244-2251 (citation omitted); 35 U.S.C. 282. A parallel approach should apply in Section 145 suits challenging patent denials, see Gov't Br. 44, but the court of appeals' decision instead produces asymmetrical treatment of the two types of challenges.

Respondent argues (Br. 45) that *Microsoft* is inapposite because the presumption of validity has no application when the PTO has denied a patent. But the statutory presumption codified a judge-made rule that was grounded in "the basic proposition that a government agency * * * was presumed to do its job"—a rationale that applies equally to the PTO's decision to deny a patent. *Microsoft*, 131 S. Ct. at 2243 (citation omitted). When the Court first formalized the presumption of validity and its application to evidence that had not been before the PTO, moreover, it drew on the deferential standard of review used in R.S. 4915 actions, stating that *Morgan*'s "thorough conviction" requirement was "little more than another form of words" for the requirement of "clear and satisfactory" evidence to overcome the presumption of validity. *Radio Corp. of Am.* v. *Radio Eng'g Labs., Inc.*, 293 U.S. 1, 9 (1934). The *Morgan* Court likewise recognized that the two types of challenges were "closely" related. 153 U.S. at 123. There is consequently no justification for allowing the presentation of new evidence to vitiate administrative-deference principles in a Section 145 suit.

Respondent is also wrong in arguing (Br. 51) that any discrepancy in treatment is justified by patent law's "deliberate asymmetry" in favor of issued patents—namely, the

presumption of validity, and the statute's placement of the initial burden on the PTO to demonstrate that a patent should not be granted. See, *e.g.*, 35 U.S.C. 102. Even assuming that the PTO's examination procedures are weighted in favor of patent issuance, that fact simply reinforces the need for deference when the examiner and the Board have agreed that an application nevertheless should be denied. And the fact that an issued patent is presumed valid simply underscores the importance of maintaining primary responsibility for patent issuance in the hands of the expert agency.

As respondent observes (Br. 51), the issuance of a patent gives rise to reliance interests that provide an additional reason for requiring a high degree of confidence before the patent may be invalidated. But important interests likewise are served by requiring the court in a Section 145 suit to sustain the PTO's patent denial absent a "thorough conviction" that the agency has erred. Allowing the presence of new evidence to vitiate any deference to the PTO's conclusions would reward applicants for withholding or belatedly creating evidence, and would transfer responsibility for determining patentability to non-expert judges. According new evidence more weight in the analysis, making the "thorough conviction" standard easier to satisfy, avoids these consequences while accounting for the fact that the PTO did not consider the evidence in question.

II. CONGRESS'S REENACTMENT OF SECTION 145 IN THE 1952 PATENT ACT SHOULD BE UNDERSTOOD TO INCORPORATE THE PREVAILING JUDICIAL PRACTICE OF LIMITING NEW EVIDENCE AND APPLYING A DEFERENTIAL STANDARD OF REVIEW

Respondent argues (Br. 24-37) that, when Congress reenacted and recodified R.S. 4915 as Section 145 of the 1952 Patent Act, it ratified prior understandings that a disappointed applicant could introduce new evidence without limitation in an R.S. 4915 proceeding, and that the court would resolve de novo all issues to which that evidence pertained. As evidence of those supposed understandings, respondent relies on dicta in this Court's decisions stating that new evidence was admissible in R.S. 4915 actions, and equivocal witness statements in the hearings that preceded the 1927 reenactment of the Patent Act. Respondent's characterization of pre-1952 law is inconsistent with *Morgan*'s recognition of the need for deferential judicial review, and with appellate courts' subsequent practice of limiting evidence not presented to the agency and reviewing the PTO's decision deferentially even when new evidence was presented. See Gov't Br. 34-37. When Congress reenacted Section 145 with "no fundamental change," S. Rep. No. 1979, 82d Cong., 2d Sess. 7 (1952), it ratified that prevailing understanding, not the contrary (and anomalous) regime that respondent posits.

A. This Court recognized in *Morgan* that the "bill in equity" authorized under R.S. 4915 was "something more than a mere appeal"; it was an action for judicial review that was "something in the nature of a suit to set aside a judgment." 153 U.S. at 121, 124. Consistent with that characterization of the cause of action created by R.S. 4915, appellate courts subsequently invoked administrative-law

principles to limit new evidence, and they applied *Morgan*'s "thorough conviction" standard of review even when new evidence was introduced. See, *e.g.*, *Globe-Union, Inc.* v. *Chicago Tel. Supply Co.*, 103 F.2d 722, 727-728 (7th Cir. 1939); *Schilling* v. *Schwitzer-Cummins Co.*, 142 F.2d 82, 84-85 (D.C. Cir. 1944); *Nichols* v. *Minnesota Mining & Mfg. Co.*, 109 F.2d 162, 163, 166 (4th Cir. 1940).

Respondent argues (Br. 29) that, because the parties in *Morgan* did not introduce new evidence, the decision "has nothing to do with the standard governing admission of evidence" in R.S. 4915 proceedings. But the Court's characterization of the proceeding as one for judicial review of agency action spoke directly to that issue. As the lower courts subsequently recognized, this Court's identification of the Patent Office as the primary decisionmaker, and the courts as deferential reviewers, highlighted the need to present to the agency all evidence necessary to determine patentability. See *Barrett Co.* v. *Koppers Co.*, 22 F.2d 395, 397 (3d Cir. 1927). The Court's description of the action as "something in the nature of a suit to set aside a judgment," *Morgan*, 153 U.S. at 124—an allusion to the equity pleading known as a bill of review—reinforced that understanding. See Gov't Br. 31-32.

Respondent also argues (Br. 29-30) that because *Morgan* concerned an interference proceeding, the decision did not affect the admissibility of evidence in challenges to ex parte patent denials. Respondent observes (Br. 30 & n.19) that, as amended in 1927, R.S. 4915 made the administrative record underlying a Patent Office priority decision admissible in a subsequent judicial challenge "without prejudice * * * to the right of the parties to take further testimony." Act of Mar. 2, 1927, ch. 273, § 11, 44 Stat. 1336-1337; 35 U.S.C. 146. Respondent's reliance on that language is misplaced. Rather than authorizing the introduc-

tion of new evidence without limitation, that language accompanied Congress's elimination of equity-rule barriers to introducing the administrative record in R.S. 4915 proceedings, and it was deemed necessary to clarify that admitting the record did not preclude introducing new evidence. See *Velsicol Chem. Corp.* v. *Monsanto Co.*, 579 F.2d 1038, 1045 (7th Cir. 1978). Although the 1927 amendment made clear that new evidence was not altogether precluded when an R.S. 4915 plaintiff challenged a Patent Office priority determination, it did not address the circumstances in which such evidence was admissible.

Respondent also suggests (Br. 28-29) that constraints on new evidence could not have applied in R.S. 4915 actions because such actions followed the District of Columbia courts' review of the Patent Office's decision, Gov't Br. 5, and res judicata would have warranted dismissal in the absence of new evidence. That argument proves too much. Like many other cases decided under R.S. 4915, *Morgan* involved no new evidence, but the Court did not invoke res judicata as a ground for dismissing the plaintiff's claims. See also, *e.g.*, *Austin* v. *Coe*, 69 F.2d 832 (D.C. Cir. 1934).

2. Respondent dismisses (Br. 33-34) the significance of the pre-1952 appellate decisions cited by the government, arguing that courts excluded only evidence that had been intentionally withheld from the Patent Office. But while the courts applied varying verbal formulations to describe the limitations they placed on the admissibility of evidence not presented to the Patent Office (Gov't Br. 34-36), some courts framed the standard as excluding evidence that was reasonably available during the PTO proceedings.[6] See,

[6] The fact that courts often admitted new evidence under the admissibility standard they announced (Resp. Br. 34 & n.26) is irrelevant. The salient point is that courts admitted the evidence only after concluding that it satisfied applicable limitations.

e.g., *Boucher Inventions, Ltd.* v. *Sola Elec. Co.*, 131 F.2d 225, 227 (D.C. Cir. 1942) ("Section 4915 * * * contemplates a full disclosure to [the Patent Office], so far as is reasonably possible."), cert. denied, 318 U.S. 770 (1943); *Globe-Union*, 103 F.2d at 728 (new evidence "which previously had not been procurable or which had become known after" PTO proceedings was admissible). Others stated that evidence "withheld" from the Patent Office should be excluded. See *Barrett*, 22 F.2d at 397; *Schilling*, 142 F.2d at 84-85. Despite those varying formulations, however, the courts grounded the exclusion of new evidence in a common source: the administrative-law principle that the agency should have the opportunity to consider relevant evidence in the first instance. See, *e.g.*, *Barrett*, 22 F.2d at 397-398; *Globe-Union*, 103 F.2d at 728.

To be sure, the variations among the different courts' admissibility standards undermines any suggestion that Congress adopted one particular formulation when it enacted the 1952 Patent Act. The most natural inference therefore is that Congress adopted the prevailing understanding that R.S. 4915 was governed by administrative-review principles—including limitations on presenting new evidence in court, and a deferential standard of review. In giving effect to that intent, this Court should adopt the standard that best comports both with the administrative-law rules that prevailed in 1952, and with the rule that prevails today—namely, that new evidence is not admissible in judicial-review proceedings if the applicant had a reasonable opportunity to present it to the agency.

3. Respondent also relies (Br. 25-27) on dicta in this Court's decisions stating that R.S. 4915 permitted introduction of evidence not contained in the administrative record. These decisions did not concern the nature of an R.S. 4915 action, however, and the Court had no occasion to address

the circumstances under which new evidence would be admissible.

In *Butterworth* v. *United States ex rel. Hoe*, 112 U.S. 50 (1884), the Court considered whether the Secretary of the Interior had statutory authority to review a decision made by the Commissioner of Patents in an interference proceeding. *Id.* at 52, 55. The Court held that the Secretary lacked such authority because Congress had provided "express appeals from the [Commissioner's] decision"—*i.e.*, the direct appeal provided in Rev. Stat. § 4911 (1878)—and, "in cases where technical appeals are not given, other modes of review by judicial process"—*i.e.*, an action under R.S. 4915. *Butterworth*, 112 U.S. at 63. In passing, the Court described an R.S. 4915 proceeding as being "heard upon all competent evidence adduced, and upon the whole merits," *id.* at 61; but the Court had no occasion to discuss the circumstances in which new evidence would be admissible in such a case.

In *Gandy* v. *Marble*, 122 U.S. 432 (1887), the Court held that an R.S. 4915 action was a stage in "the application for the patent," and therefore was subject to a statutory timeliness rule governing applications not prosecuted for two years. *Id.* at 439-440. The Court reiterated *Butterworth*'s description of the R.S. 4915 proceeding, but only to explain that an R.S. 4915 suit remained part of the application process even though it was an original action. *Ibid.*

In re Hien, 166 U.S. 432 (1897), is even further afield, as it did not involve a proceeding under R.S. 4915. In holding that direct appeals of Patent Office decisions under R.S. 4911 could be subject to a 45-day time limit, the Court emphasized that "[t]he one [R.S. 4915] is in the exercise of original, the other [R.S. 4911] of appellate, jurisdiction." *Id.* at 439. Again in dicta, the Court quoted *Butterworth*'s description of R.S. 4915.

In *Hoover*, *supra*, the Court held that R.S. 4915 was available to anyone denied a patent, regardless of the ground of rejection. 325 U.S. at 83. The Court's statement that an R.S. 4915 proceeding "may include evidence not presented in the Patent Office," *ibid.*, did not address the circumstances in which such evidence is admissible.

In sum, although this Court's pre-1952 decisions recognized that new evidence could *sometimes* be introduced in R.S. 4915 proceedings, they did not meaningfully clarify the circumstances under which such evidence could be admitted, much less suggest that such evidence was admissible *without limitation*. Any inference that the 1952 Congress intended to ratify a purported rule of unlimited admissibility is particularly unlikely given *Morgan*'s characterization of R.S. 4915 actions as suits to "set aside" administrative determinations, 153 U.S. at 124, and given the many intervening appellate decisions that had limited the introduction of new evidence and had applied a deferential standard of review.

4. Finally, respondent relies (Br. 31-32) on statements made during the congressional hearings preceding the Patent Act's 1927 reenactment. Respondent views those statements as establishing that Congress understood R.S. 4915 to authorize a "de novo" proceeding. Even if witness statements could shed meaningful light on Congress's intent or its pre-APA understanding of the term "de novo," see Gov't Br. 39-40, the testimony on which respondent relies does not help him. Several witnesses simply stated that R.S. 4915 permitted new evidence, and others expressed an understanding of R.S. 4915 that supports the government's position. See *To Amend Section 52 of the Judicial Code and Other Statutes Affecting Procedure in Patent Office: Hearing on H.R. 6252 and H.R. 7087 Before the House Comm. on Patents*, 69th Cong., 1st Sess. 21 (1926) (state-

ment of Charles Howson) (R.S. 4915 permitted applicant to "make up a record in addition to that he *has been enabled to furnish* the examiners in the Patent Office.") (emphasis added).

CONCLUSION

For the foregoing reasons and those stated in our opening brief, the judgment of the court of appeals should be vacated and the case remanded for further proceedings.

Respectfully submitted.

DONALD B. VERRILLI, JR.
Solicitor General

NOVEMBER 2011

SUPPLEMENTAL BRIEF

No. 10-1219

In the Supreme Court of the United States

DAVID J. KAPPOS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR, UNITED STATES PATENT AND TRADEMARK OFFICE, PETITIONER

v.

GILBERT P. HYATT

ON PETITION FOR A WRIT OF CERTIORARI TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

SUPPLEMENTAL BRIEF FOR THE PETITIONER

DONALD B. VERRILLI, JR.
Solicitor General
Counsel of Record
Department of Justice
Washington, D.C. 20530-0001
SupremeCtBriefs@usdoj.gov
(202) 514-2217

TABLE OF AUTHORITIES

Cases: Page

American Hoist & Derrick Co. v. *Sowa & Sons, Inc.*, 725 F.2d 1350 (Fed. Cir.), cert. denied, 469 U.S. 821 (1984) 3, 7

Microsoft Corp. v. *i4i Ltd. P'ship*, No. 10-290 (June 9, 2011) ..... *passim*

Morgan v. *Daniels*, 153 U.S. 120 (1894) 3, 4, 5

RCA v. *Radio Eng'g Labs., Inc.*, 239 U.S. 1 (1934) 3, 4, 5

Statutes and rule:

Administrative Procedure Act, 5 U.S.C. 701 *et seq.* 5

Patent Act of 1952, 35 U.S.C. 1 *et seq.*:

35 U.S.C. 145 ..... 2, 4, 5, 6, 7

35 U.S.C. 282 ..... 2, 3, 5, 6

Rev. Stat. § 4915 (1878) 2, 4, 5

Sup. Ct. R. 15.8 1

In the Supreme Court of the United States

No. 10-1219

DAVID J. KAPPOS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR, UNITED STATES PATENT AND TRADEMARK OFFICE, PETITIONER

v.

GILBERT P. HYATT

ON PETITION FOR A WRIT OF CERTIORARI TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

SUPPLEMENTAL BRIEF FOR THE PETITIONER

Pursuant to Rule 15.8 of the Rules of this Court, the Solicitor General, on behalf of petitioner, the Under Secretary of Commerce for Intellectual Property and Director of the United States Patent and Trademark Office (PTO), files this supplemental brief to address the effect on this case of *Microsoft Corp.* v. *i4i Ltd. Partnership*, No. 10-290 (June 9, 2011). The petition for a writ of certiorari urged this Court to hold the petition pending the Court's decision in *Microsoft*. The petition explained that both cases involve judicial review of challenges to the PTO's disposition of patent applications, and both therefore implicate principles of deference to administrative authority and expertise.

The questions presented in this case concern (1) the circumstances in which a plaintiff who brings suit under 35 U.S.C. 145 to challenge the PTO's denial of a patent may introduce evidence not considered by the agency, and (2) the standard of review that applies when such evidence is introduced. See Pet. I. The Federal Circuit held that the plaintiff in a Section 145 action may introduce any new evidence of patentability that is admissible under the Federal Rules of Evidence, even if the applicant failed without cause to present the evidence to the agency. The court further held that, when new evidence is introduced, the district court should engage in de novo review of the issues to which that evidence pertains. See Pet. App. 2a.

After the government filed its reply brief in this case, the Court issued its decision in *Microsoft*. The Court in *Microsoft* held that a party challenging the validity of a patent in the context of an infringement suit must establish invalidity by clear and convincing evidence, even when the challenger proffers evidence of invalidity that the PTO did not consider when it granted the patent. That decision reinforces the government's contention in this case that the Federal Circuit's construction of 35 U.S.C. 145 is an unjustified departure from established administrative-review principles and from the historical understanding of proceedings under Section 145's predecessor, Rev. Stat. § 4915 (1878) (R.S. 4915). This Court should therefore grant the petition for a writ of certiorari.

A. 1. In *Microsoft*, this Court addressed the standard of proof that applies when the defendant in an infringement suit contends that the relevant patent is invalid. The Court held that the defendant bears the burden of establishing invalidity by clear and convincing evidence, even when the relevant evidence was not considered by the PTO. Slip op. 5-6. The Court explained that in enacting Section 282 of the

Patent Act of 1952, which provides that a "patent shall be presumed valid," 35 U.S.C. 282, Congress had adopted "what, until that point, had been a common-law presumption based on 'the basic proposition that a government agency such as the [PTO] was presumed to do its job.'" *Microsoft*, slip op. 3 (quoting *American Hoist & Derrick Co.* v. *Sowa & Sons, Inc.*, 725 F.2d 1350, 1359-1360 (Fed. Cir.), cert. denied, 469 U.S. 821 (1984) (*American Hoist*)). The Court further explained that the common-law presumption of validity had been "authoritative[ly]" explicated in *RCA* v. *Radio Engineering Laboratories, Inc.*, 293 U.S. 1, 8 (1934), and that the Court in *RCA* had required an accused infringer to establish the invalidity of the patent at issue by "more than a dubious preponderance." *Microsoft*, slip op. 14-15; see *RCA*, 293 U.S. at 7-8. The Court stated that "[f]or nearly 30 years, the Federal Circuit has interpreted [Section] 282" in accordance with *RCA*, and that Congress has "allowed the Federal Circuit's correct interpretation * * * to stand." *Microsoft*, slip op. 19-20. Accordingly, the Court affirmed the Federal Circuit's interpretation of Section 282. *Id.* at 17; see *American Hoist*, 725 F.2d at 1359-1360.

Under the Court's decision in *Microsoft*, challenges to granted patents will continue to be adjudicated in light of the administrative-deference principles identified by this Court in *RCA* and in *Morgan* v. *Daniels*, 153 U.S. 120, 124-125 (1894). See Pet. 11-12. The decision thus confirms that the ruling below will create an unjustified asymmetry between judicial review of patent grants and review of patent denials. This Court has long recognized that the two types of challenges are "closely" related. See *Morgan*, 153 U.S. at 123; *RCA*, 293 U.S. at 9. Both are in essence attacks on the PTO's disposition of a patent application, see *Morgan*, 153 U.S. at 124, and both require the court to review the

"various factual determinations" made by PTO examiners with expertise in the relevant fields, *Microsoft*, slip op. 2. Invalidity challenges and Section 145 actions therefore implicate common principles of administrative deference that should inform the nature and scope of judicial review in both contexts. See *Morgan*, 153 U.S. at 124-125; *RCA*, 293 U.S. at 7-9; Pet. 29-31.

The decision below, however, creates an anomalous regime in which the PTO's decision to *grant* a patent receives deference even when the challenger presents new evidence of invalidity, but the PTO's decision to *deny* a patent receives no deference whenever new evidence is introduced. That inconsistency is particularly unjustified because a party challenging a granted patent often will have had no opportunity to present evidence of invalidity to the PTO, see *Microsoft*, slip op. 18, while an unsuccessful patent applicant who brings a Section 145 action will generally have had the opportunity—and the obligation, see Pet. 14—to present evidence of patentability to the agency examiner. This Court's review is warranted to correct that disparity, and to ensure that administrative-law principles are applied consistently whenever the PTO's disposition of a patent application is challenged in court.

2. The Court in *Microsoft* read *RCA* to hold "without qualification" that a heightened standard of proof applies whenever the defendant in an infringement suit challenges the validity of an issued patent. *Microsoft*, slip op. 10-11. The Court rejected Microsoft's argument that *RCA* and its progeny should be limited to their precise facts, and that Congress should be viewed as having implicitly codified "unstated limitations on the heightened standard of proof." *Id.* at 11-12. Similarly, the Court in *Morgan* interpreted R.S. 4915 (Section 145's predecessor) to authorize an action for judicial review of the Patent Office's decision to deny a

patent, and the Court held that review of that agency decision would be conducted under a deferential standard. 153 U.S. at 123-125.

The court of appeals in this case concluded that, because *Morgan* did not involve the introduction of new evidence, it was merely "a case about what standard of review ought to apply when" the record is "exactly the same record that was before the Patent Office." Pet. App. 23a. But the *Morgan* Court did not announce any such limits on its description of R.S. 4915 as a suit to "set aside" an agency's decision. 153 U.S. at 124. Just as this Court in *Microsoft* construed Section 282 as incorporating the heightened-evidence requirement that was announced "without qualification" in *RCA*, see *Microsoft*, slip op. 11, the court of appeals should have interpreted Section 145 in a manner consistent with *Morgan*'s unqualified description of R.S. 4915 as a provision for judicial review of agency action.

3. The defendant in *Microsoft* argued in the alternative that "a preponderance standard must at least apply where the evidence before the factfinder was not before the PTO during the examination process." Slip op. 14. In rejecting that contention, the Court observed, *inter alia*, that "a standard of proof that would rise and fall with the facts of each case" would be "unusual and impractical." *Id.* at 16. The Court "assume[d]" that Congress "would have said so expressly" if it had intended to adopt "a variable standard of proof that must itself be adjudicated in each case." *Ibid.*

The court of appeals' interpretation of Section 145, however, creates just such a variable regime. Under the Federal Circuit's approach, Section 145 functions as a judicial-review proceeding subject to the Administrative Procedure Act, 5 U.S.C. 701 *et seq.*, when the plaintiff does not rely on new evidence; but when new evidence is introduced, the district court must engage in de novo review of any issues

to which that evidence pertains. Pet. App. 30a-31a. The text of Section 145 provides no support for that interpretation, and the court of appeals suggested no reason why Congress would have intended the standard of proof to "rise and fall with the facts of each case." Cf. *Microsoft*, slip op. 15-16. The Federal Circuit's interpretation of Section 145 is especially unlikely because that approach, by affording a more favorable standard of review to patent applicants who introduce new evidence in judicial proceedings, effectively rewards disappointed applicants for withholding evidence from the PTO. It also encourages even those applicants who presented all available material evidence to the PTO during the examination process to attempt to create new evidence purely for the purpose of presenting it to the district court and obtaining de novo review. See Pet. 28-29.

B. The Court should grant plenary review in this case because vacating the decision below and remanding for further consideration in light of *Microsoft* would be unlikely to advance resolution of the dispute. In holding that the clear-and-convincing-evidence standard applies when the defendant in an infringement suit contests the validity of an issued patent, the Court in *Microsoft* did not overturn Federal Circuit precedent, but rather confirmed the interpretation of Section 282 that had long prevailed within that circuit. As explained above, there is no sound textual, historical, or policy reason for giving disappointed patent applicants—particularly those who fail without cause to present relevant evidence to the PTO—a more favorable standard of review when they attack the agency's decision than is available to defendants in infringement suits who contest a patent's validity. The en banc Federal Circuit apparently viewed that disparity to be justified, however, because it issued its decision in this case against the backdrop of its

longstanding precedent requiring that all invalidity challenges be established by clear and convincing evidence. See *American Hoist*, 725 F.3d at 1359-1360. In addition, the first question presented in this case, which concerns the extent to which new evidence is admissible in a Section 145 proceeding, has no direct analogue in *Microsoft*. It therefore would be preferable for this Court to grant plenary review of both questions presented rather than to remand this case for further consideration in light of *Microsoft*.

* * * * *

For the foregoing reasons, and those stated in the petition and in the government's reply brief, the petition for a writ of certiorari should be granted.

Respectfully submitted.

DONALD B. VERRILLI, JR.
Solicitor General

JUNE 2011

SUPPLEMENTAL BRIEF

AND
BRIEFS

JUN 14 2011
OFFICE OF THE CLERK

No. 10-1219

IN THE
Supreme Court of the United States

DAVID J. KAPPOS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR, UNITED STATES PATENT AND TRADEMARK OFFICE,
Petitioner,

v.

GILBERT P. HYATT,
Respondent.

On Petition for a Writ of Certiorari to the United States Court of Appeals for the Federal Circuit

SUPPLEMENTAL BRIEF FOR RESPONDENT

GREGORY L. ROTH
5712 Parkwest Circle
La Palma, California 90623
(714) 723-6871

AARON M. PANNER
Counsel of Record
KELLOGG, HUBER, HANSEN, TODD, EVANS & FIGEL, P.L.L.C.
1615 M Street, N.W.
Suite 400
Washington, D.C. 20036
(202) 326-7900
(apanner@khhte.com)

June 14, 2011

Library of Congress
Law Library

TABLE OF CONTENTS

Page

TABLE OF AUTHORITIES ii

ARGUMENT 1

CONCLUSION 5

TABLE OF AUTHORITIES

Page

CASES

Butterworth v. United States ex rel. Hoe, 112 U.S. 50 (1884) 3

Microsoft Corp. v. i4i LP, No. 10-290, 2011 WL 2224428 (U.S. June 9, 2011) 1, 2, 3, 4, 5

Radio Corp. of Am. v. Radio Eng'g Labs., Inc., 293 U.S. 1 (1934) 1

STATUTES AND RULES

Patent Act (35 U.S.C.):

35 U.S.C. § 141 3

35 U.S.C. § 144 3

35 U.S.C. § 145 .....2, 3, 4, 5

35 U.S.C. § 282 ..... 1, 2

Rev. Stat. § 4915 3

Sup. Ct. R. 15.8 1

Pursuant to this Court's Rule 15.8, respondent submits this supplemental brief to address the impact of this Court's decision in *Microsoft Corp. v. i4i LP*, No. 10-290, 2011 WL 2224428 (June 9, 2011), on the government's petition for certiorari, which the government asked to be held for *Microsoft*. The Court's holding that a "clear and convincing" standard of proof applies under § 282 when an accused infringer challenges the validity of an issued patent has no direct bearing on either of the two questions presented and therefore does not provide a basis for vacatur and remand of the Federal Circuit's decision. If anything, that decision confirms that the government's petition should be denied.

1. *Microsoft*'s holding is provision-specific, involving the proper interpretation of the statutory presumption of validity. *See* 35 U.S.C. § 282. Relying on the Court's "authoritative" interpretation of the common-law presumption of validity in *Radio Corp. of America v. Radio Engineering Laboratories, Inc.*, 293 U.S. 1 (1934), the Court found that the "common-law presumption . . . reflected the universal understanding" that the presumption "encompassed . . . a heightened standard of proof," 2011 WL 2224428, at *6-*7. "Whatever the significance of a presumption in the abstract, basic principles of statutory construction require us to assume that Congress meant to incorporate 'the cluster of ideas' attached to the common-law term it adopted." *Id.* at *7.

Neither § 282 nor the presumption of validity of an issued patent is at issue in this case. Furthermore, while the government suggested that the decision in *Microsoft* might "shed light on the proper disposition of this case" by elaborating "the application of administrative-review principles to the PTO's patent-

ing decisions," Pet. 31, the decision does not include any such elaboration. To the contrary, this Court expressly avoided either relying on or commenting on the application of generic principles of administrative deference to PTO decisions. *See* 2011 WL 2224428, at *12 ("We find ourselves in no position to judge the comparative force of these policy arguments."). The opinion thus adds no force to (indeed, as discussed below, is inconsistent with) the government's argument that the long-standing interpretation of § 145 should be changed to conform to the government's understanding of "fundamental principles of administrative law." Pet. 10.

2. *Microsoft*'s approach to statutory construction bolsters the Federal Circuit's conclusion that § 145 permits the introduction of evidence that was not before the PTO, consistent with the Federal Rules of Evidence and Civil Procedure. *See* App. 2a. This Court's analysis in *Microsoft* began with the language of the statute; finding that the language did not, by its express terms, address the standard of proof, this Court relied on the long history of judicial application of the presumption of validity that preceded the adoption of § 282 to construe the statute. This Court's conclusion was based on its recognition that, "by the time Congress enacted § 282 . . . , the presumption of patent validity had long been a fixture of the common law" with a "settled meaning." 2011 WL 2224428, at *7.

In the case of § 145, the statutory text provides a much stronger indication of the proper resolution of the admission-of-evidence question (correctly) decided by the Federal Circuit. The term "civil action" in § 145, the remaining language of the provision – which authorizes the district court to "adjudge that

[the] applicant is entitled to receive a patent . . . as the facts in the case may appear" – and the contrast with provisions that provide for an on-the-record "appeal," *see* 35 U.S.C. §§ 141, 144, all demonstrate that § 145 allows an applicant to introduce new evidence.

Any uncertainty remaining after reading this language in isolation would, moreover, be dispelled by the long legislative history of § 145 and its predecessors. The nature of the action provided under § 145 has had "an established meaning traceable to the mid-19th century." *Microsoft*, 2011 WL 2224428, at *8 n.7. This Court noted in 1884 (citing several older cases from the lower courts) that the "bill in equity" authorized by R.S. § 4915 was not "confined to the case as made in the record of that office, but is prepared and heard upon all competent evidence adduced, and upon the whole merits." *Butterworth v. United States ex rel. Hoe*, 112 U.S. 50, 61 (1884). This Court repeatedly reiterated that understanding, which is likewise reflected in the uniform decisions of the lower courts. *See* Br. in Opp. 17 & n.8. That history leaves no room for doubt that Congress meant to endorse that understanding of the statute when it adopted revised R.S. § 4915 in 1927 and the recodified § 145 in 1952. *See id.* at 18-20; App. 12a-18a.

There is no basis in this Court's cases for any special limitation on the admission of evidence in actions under § 145; nor does the government even cite any pre-1952 lower court cases to support the strict limitation on the introduction of new evidence that it seeks to impose. *See* Br. in Opp. 21-22. "Squint as [one] may," *Microsoft*, 2011 WL 2224428, at *8, none of the cases that the government cites supports limit-

ing an applicant to evidence that could not have been presented to the Patent Office in the first instance.

3. With respect to the second question presented, *Microsoft* does not affect the Federal Circuit's reaffirmation that, when new evidence is introduced in an action under § 145, a district court must make factual determinations *de novo* – a settled standard that (as we have noted, *see* Br. in Opp. 28-29) the government did not ask the Federal Circuit to change. Furthermore, *Microsoft* illustrates and provides support for the distinction drawn by the Federal Circuit between a governing standard and the weight to be afforded to evidence. As we have explained, *see id.* at 29-30, the Federal Circuit noted that the district court can, in deciding factual questions *de novo* on a new evidentiary record, consider "the proceedings before and findings of the Patent Office in deciding what weight to afford an applicant's newly-admitted evidence." App. 28a; *cf.* App. 31a ("Because the court must determine the weight and import of . . . new evidence, we have held that the district court in a § 145 action must make de novo fact findings with respect to factual issues to which the new evidence relates."). "Should the facts of a particular case cast suspicion on new evidence that an applicant failed to introduce before the Patent Office, the district court in a § 145 action would be within its discretion to give that evidence less weight." App. 28a-29a.

Microsoft, analogously, holds that the standard of proof that applies when an accused infringer challenges the validity of an issued patent does not resolve what weight a fact-finder should give to particular evidence. While the clear-and-convincing standard applies irrespective of whether evidence of invalidity was considered by the PTO, "new evidence

supporting an invalidity defense may 'carry more weight' in an infringement action than evidence previously considered by the PTO." 2011 WL 2224428, at *10 (citation omitted). The government is free to argue in cases under § 145 that new evidence should be given lesser weight in particular circumstances.

Because the Federal Circuit left it open to district courts to weigh new evidence in an action under § 145 in light of the prior proceedings before the PTO, the second question presented in the government's petition does not warrant review.

CONCLUSION

The petition for a writ of certiorari should be denied.

Respectfully submitted,

GREGORY L. ROTH
5712 Parkwest Circle
La Palma, California 90623
(714) 723-6871

AARON M. PANNER
Counsel of Record
KELLOGG, HUBER, HANSEN, TODD, EVANS & FIGEL, P.L.L.C.
1615 M Street, N.W.
Suite 400
Washington, D.C. 20036
(202) 326-7900
(apanner@khhte.com)

June 14, 2011

AMICUS CURIAE BRIEF

No. 10-1219

IN THE

Supreme Court of the United States

DAVID J. KAPPOS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR, UNITED STATES PATENT AND TRADEMARK OFFICE,

Petitioner,

v.

GILBERT P. HYATT,

Respondent.

ON WRIT OF CERTIORARI TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

BRIEF FOR *AMICUS CURIAE* AMERICAN INTELLECTUAL PROPERTY LAW ASSOCIATION IN SUPPORT OF RESPONDENT

VERNON M. WINTERS
Counsel of Record
GREENBERG TRAURIG LLP
153 Townsend Street,
8th Floor
San Francisco, CA 94107
(415) 655-1300
wintersv@gtlaw.com

WILLIAM G. BARBER
PRESIDENT
AMERICAN INTELLECTUAL
PROPERTY LAW ASSOCIATION
241 18th Street, Suite 700
Arlington, VA 22202
(703) 415-0780

Attorneys for Amicus Curiae,
American Intellectual Property Law Association

October 25, 2011

238806

COUNSEL PRESS

(800) 274-3321 • (800) 359-6859

TABLE OF CONTENTS

Page

TABLE OF CONTENTS..... i

TABLE OF APPENDICES iv

TABLE OF CITED AUTHORITIES v

STATEMENT OF INTEREST 1

SUMMARY OF ARGUMENT..... 2

ARGUMENT..... 6

I. The law appropriately permits a district court to receive and assess evidence in a § 145 action without being hobbled by the government's proposed restrictions on new evidence..... 6

A. The positive law does not reflect the government's proposed changes..... 6

1. This Court's jurisprudence has not imposed or even suggested those restrictions..... 6

2. There was no settled practice in the regional appellate courts for Congress to adopt..... 11

Table of Contents

Page

3. The government's imprecise, amorphous proposed change would invite intrusive and expansive collateral litigation. 12

B. The policy rationales that the government identifies to support its non-statutory argument are not compelling. 14

1. The government's proposed change would upset settled expectations in the patent community. 15

2. The government's proposed change would have effects beyond patent law – or would create a patent-specific standard. 18

3. Administrative exhaustion principles do not nestle comfortably in § 145's statutory structure. 20

4. The professed concern that applicants will "game" the system by reserving evidence ignores current law. 23

II. The law appropriately provides for the district court's *de novo* assessment of the factual issues raised in the PTO that the new evidence affects. 25

Table of Contents

	Page
A. *De novo* assessment is the positive law	26
1. *De novo* proceedings follow from the statutory text	26
2. *De novo* proceedings follow from this Court's precedent	27
3. *Morgan v. Daniels* (1894), upon which the government heavily relies, did not resolve the issue	28
B. It is appropriate for the law to continue to permit the district court's *de novo* review	30
1. Deferential review would upset settled expectations in the patent community	30
2. The asserted "asymmetry" problem is illusory	32
3. The government's "variable standard of review" argument provides a solution in search of a problem	34
CONCLUSION	36

TABLE OF APPENDICES

Page

APPENDIX A — RELEVANT STATUTES 1a

TABLE OF CITED AUTHORITIES

Page

CASES:

Aktieselskabet AF 21. November 2001 v. Fame Jeans Inc., 525 F.3d 8 (D.C. Cir. 2008) 18

Alza Corp. v. Andrx Pharm., LLC, 603 F.3d 935 (Fed. Cir. 2010) 21, 22

Barrett Co. v. Koppers Co., 22 F.2d 395 (3d Cir. 1927) 12

Brand v. Miller, 487 F.3d 862 (Fed. Cir. 2007) 31

Burlington Indus., Inc. v. Quigg, 822 F.2d 1581 (Fed. Cir. 1987) 16, 31

Butterworth v. Hoe, 112 U.S. 50 (1884) ..... *passim*

CAE, Inc. v. Clean Air Eng'g, Inc., 267 F.3d 660 (7th Cir. 2001) 18-19

Cal. Research Corp. v. Ladd, 356 F.2d 813 (D.C. Cir. 1966) 12

California v. Green, 399 U. S. 149 (1970) 16

Cited Authorities

Page

Christianson v. Colt Indus. Op. Corp.,
486 U.S. 800 (1981) 17

Comm'r v. Schleier,
515 U.S. 323 (1995) 16

Consol. Aluminum Corp. v. Foseco Int'l Ltd.,
910 F.2d 804 (Fed. Cir. 1990) 24

Dickinson v. Zurko,
527 U.S. 150 (1999) ..... *passim*

eBay, Inc. v. MercExchange, LLC,
547 U.S. 388 (2006) 20

Eccles v. Peoples Bank of Lakewood Village,
333 U.S. 426 (1948) 16, 22, 33

Engine Mfrs. Assn. v. South Coast Air Quality Mgmt. Dist.,
541 U.S. 246 (2004) 26

Fed. Commc'ns Comm'n v. WJR, The Goodwill Station,
337 U.S. 265 (1949) 14

Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.,
535 U.S. 722 (2002) 15, 30, 31, 33

Cited Authorities

Page

Florida Power & Light Co. v. Lorion,
470 U.S. 729 (1985) 23

Fregeau v. Mossinghoff,
776 F.2d 1034 (Fed. Cir. 1985) 30, 34

Gillette Co. v. "42" Prod. Ltd.,
435 F.2d 1114 (9th Cir. 1970) 19

Gould v. Quigg,
822 F.2d 1074 (Fed. Cir. 1987) 7, 16, 30

Goya Foods Inc. v. Tropicana Prod., Inc.,
846 F.2d 848 (2d Cir. 1988) 19

Graham v. John Deere Co.,
383 U.S. 1 (1966) 21, 22

Holmes Group, Inc. v. Vornado Air Circulation Sys., Inc.,
535 U.S. 826 (2005) 18, 20

Hoover v. Coe,
325 U.S. 79 (1945) ..... *passim*

Hyatt v. Kappos,
625 F.3d 1320 (Fed. Cir. 2010) 25, 31

In re Gartside,
203 F.3d 1305 (Fed. Cir. 2000) 31

Cited Authorities

Page

In re Lueders,
111 F.3d 1569 (Fed. Cir. 1997) 31

In re Newman,
763 F.2d 407 (Fed. Cir. 1985) 30

Kellogg Co. v. Toucan Golf, Inc.,
337 F.3d 616 (6th Cir. 2003) 18

Kewanee Oil Co. v. Bicron Corp.,
416 U.S. 470 (1974) 33

Kingsdown Med. Consultants, Ltd. v. Hollister Inc.,
863 F.2d 867 (Fed. Cir. 1988) 24

Knutson v. Gallsworthy,
164 F.2d 497 (D.C. Cir. 1947) 12

Mazzari v. Rogan,
323 F.3d 1000 (Fed. Cir. 2003) 16, 31

McNary v. Haitian Refugee Ctr., Inc.,
498 U.S. 479 (1991) 10

MedImmune, Inc. v. Genentech, Inc.,
549 U.S. 118 (2007) 20

Microsoft Corp. v. i4i Ltd. P'ship,
564 U.S. ___, 131 S. Ct. 2238 (2011) 9, 32, 34

Cited Authorities

Page

Minn. Mining & Mfg. Co. v. Carborundum Co.,
155 F.2d 746 (3d Cir. 1946) 11

Molins PLC v. Textron, Inc.,
48 F.3d 1172 (Fed. Cir. 1995) 13

Morgan v. Daniels,
153 U.S. 120 (1894) 10, 28, 30

Newman v. Quigg,
681 F. Supp. 16 (D.D.C. 1988)..... 17

Newman v. Quigg,
877 F. 2d 1575 (Fed. Cir. 1989)..... 16

Newman v. Quigg,
923 F.2d 868 (Fed. Cir. 1990)..... 17

Noah's, Inc. v. Nark, Inc.,
728 F.2d 410 (8th Cir. 1984) 19

PHC, Inc. v. Pioneer Healthcare, Inc.,
75 F.3d 75 (1st Cir. 1996)..... 19

Price v. Symsek,
988 F.2d 1187 (Fed. Cir. 1993) 21, 34

Rasmusson v. SmithKline Beecham Corp.,
413 F.3d 1318 (Fed. Cir. 2005) 29

Cited Authorities

Page

Schilling v. Schwitzer-Cummins Co.,
142 F.2d 82 (D.C. Cir. 1944) 12

Smith v. City of Jackson, Miss.,
544 U.S. 228 (2005) 18

Standard Cartridge Co. v. Peters Cartridge Co.,
77 F. 630 (6th Cir. 1896) 12

Tagg Bros. & Moorhead v. United States,
280 U.S. 420 (1930) 23

Takeda Pharm. Co., Ltd. v. Doll,
561 F.3d 1372 (Fed. Cir. 2009) 16

Taylor v. Fed. Nat. Mortg. Ass'n,
374 F.3d 529 (7th Cir. 2004) 14

Therasense, Inc. v. Becton, Dickinson, and Co.,
649 F.3d. 1276, 2011 WL 2028255 (Fed. Cir. 2011). . 13, 24

Titanium Metals Corp. of Am. v. Banner,
778 F.2d 775 (Fed. Cir. 1985) 16

TriMed, Inc. v. Stryker Corp.,
608 F.3d 1333 (Fed. Cir. 2010) 21

Vas-Cath Inc. v. Mahurkar,
935 F.2d 1555 (Fed. Cir. 1991) 21

Page

Velsicol Chem. Corp. v. Monsanto Co.,
579 F.2d 1038 (7th Cir. 1978) 12

Warner-Jenkinson Co. v. Hilton Davis Chem. Co.,
520 U.S. 17 (1997) 15, 30, 33

Western Elec. Co. v. Fowler,
177 F. 224 (7th Cir. 1910)..... 12

White v. Illinois,
502 U.S. 346 (1992) 16, 22

STATUTES:

15 U.S.C. 1071(b) 18, 19

15 U.S.C. 1071(b)(1) 18, 1935

U.S.C. 141 ..... *passim*

35 U.S.C. 145 ..... *passim*

35 U.S.C. 146 10

35 U.S.C. 288 24

Rev. Stat. 4915 (1878) 6, 8, 11

Page

RULES:

Fed. Cir. L. R. 47.8(b) 17

Fed. R. Civ. P. 1 9

Fed. R. Civ. P. 2 9

Fed. R. Ev. 101 9

Fed. R. Ev. 102 9

Supreme Court Rule 37(3)(a) 1

Supreme Court Rule 37.6 1

OTHER AUTHORITIES:

2 Anthony William Deller,
Walker on Patents: Deller's Ed.,
(1937 ed.) 12

3 *McCarthy, Trademarks And Unfair Competition*
§ 21.20 (4th ed. 2010) 19

H.R. Rep. No. 97-312 (1981) 17

Trademark Trial and Appeal Board Manual of
Procedure §§ 102.1 & 311.02(b) (3rd ed. 2011) 19

STATEMENT OF INTEREST

Amicus curiae American Intellectual Property Law Association ("AIPLA") is a national bar association of approximately 16,000 members engaged in private and corporate practice, in government service, and in the academic community. AIPLA represents a wide and diverse spectrum of individuals, companies, and institutions involved directly or indirectly in the practice of patent, trademark, copyright, and unfair competition law, as well as other fields of law affecting intellectual property.[1] AIPLA has no stake in the parties to this litigation or in this litigation's outcome other than its interest in seeking correct and consistent interpretation of the law as it relates to intellectual property issues. Therefore, AIPLA offers a balanced perspective on intellectual property enforcement issues.[2]

---

1. *Amicus curiae* certifies that no counsel for a party authored this brief in whole or in part, and that no person or entity, other than amicus, its members, or its counsel, has made any monetary contribution to the preparation or submission of this brief. After reasonable investigation, AIPLA believes that (i) no member of its Board or Amicus Committee who voted to file this brief, or any attorney in the law firm or corporation of such a member, represents a party to this litigation in this matter, (ii) no representative of any party to this litigation participated in the authorship of this brief, and (iii) no one other than AIPLA, or its members who authored this brief and their law firms or employers, made a monetary contribution to the preparation or submission of this brief. *See* Supreme Court Rule 37.6.

2. The parties' counsel have consented to the filing of this brief. Mr. Hyatt filed a general consent letter with the Court, and Mr. Kappos's counsel provided a letter of consent, filed herewith. *See* Supreme Court Rule 37(3)(a).

SUMMARY OF ARGUMENT

An applicant dissatisfied with the final decision of the United States Patent and Trademark Office ("PTO") to reject claims in a patent application has by statute two alternative and mutually exclusive paths for judicial assessment of that decision. The applicant can file an *appeal* with the Federal Circuit under 35 U.S.C. § 141; that appeal will be limited to the facts and arguments presented to the PTO and hence the appellate court's assessment of the evidence is deferential. Or, instead, the applicant can bring a *civil action* in the district court under 35 U.S.C. § 145; there both the applicant and the PTO may introduce new evidence and the trial court's assessment of the issues to which the new evidence relates is under existing law *de novo*.

Although § 145 actions, as "civil actions," are necessarily subject to the limits imposed on all civil actions by the Federal Rules of Evidence, the Federal Rules of Civil Procedure, and traditional principles of equity, in none of this Court's prior analyses of § 145 or its predecessor did this Court impose the additional limitations that the government now seeks. Indeed, the reported § 145 appellate cases consistently reflect that the district court receives new evidence without objection by the government, and that the government itself often introduces new evidence.

Now, however, the government proposes two new limitations not found in this Court's prior jurisprudence or in the nearly 30 years of § 145 jurisprudence that the Federal Circuit has carefully developed. First, the government proposes that the district court cannot

consider evidence that the parties had a reasonable opportunity to introduce in the PTO but did not. Second, the government urges that even if the district considers new evidence, it must have a "thorough conviction" that the PTO erred in order to disturb the PTO's conclusions, even though the PTO did not consider the new evidence.

These new restrictions do not find support in this Court's deep-rooted § 145 jurisprudence or in the Federal Circuit's case law from the last thirty years. The only support for the government's position appears in *some* case law from *some* regional appellate courts, before the Federal Circuit's creation and at a time when the law on these issues was in disarray. Some decisions allowed the evidence; some allowed it but gave it lesser weight; and others disallowed it, under a patchwork of different standards. That disarray proves the point. The Federal Circuit was created to bring clarity and stability to patent law issues, which it has done in the § 145 area.

Nor do the government's asserted policy rationales ring true, given the clarity of this Court's and the Federal Circuit's case law. The government's policy arguments ignore the important principle, emphasized in this Court's patent jurisprudence, that the inventing community's settled expectations ought not lightly to be disturbed. Instead, the government in the main turns to administrative exhaustion principles. But those do not nestle comfortably in § 145's structure. The statute allows the district court to consider new evidence and to assess the evidence upon the whole record, as this Court has confirmed. In short, the statutory structure inherently dilutes, if not rejects *ab initio*, administrative exhaustion notions, instead entrusting the district court to make its own decision.

In setting forth its position, the government fails to reconcile how its new § 145 procedure would also impact upon other areas of law, notably trademark appeals where there is a similar statute. The government's proposal would either require upending established law in other areas where there are similarly worded statutes, or create a different law for patents than for other substantive areas thereby violating this Court's admonition to avoid such patent-specific treatment of general legal principles. Both potentials support rejecting the government's proposal.

The government's brief issues dire warnings about applicants having an incentive to game the system by reserving the presumably most material information for the district court. Existing law provides a surfeit of severe penalties for intentionally failing to disclose material information to the PTO. Those draconian penalties include potentially rendering unenforceable not just the patent but even, in certain circumstances, the entire patent family, in addition to creating antitrust/unfair competition liability and a basis for a crime/fraud waiver to the lawyer-client privilege. Under-disclosure is not a problem the PTO faces.

Finally, the government's brief urges that the same standard ought to govern judicial assessment of both the grant and the denial of a patent application. Although linguistically similar, substantively these circumstances are quite disparate. For example, the grant of a patent application confers rights so potentially significant that this Court has spoken repeatedly of the "patent monopoly" they create. The denial of a patent application, by contrast, confers no such rights.

The statutory text, this Court's deep-rooted construction of it, the Federal Circuit's careful and consistent application of this Court's jurisprudence, and sound policy all point one way, and firmly so:

1. The plaintiff in a § 145 action should continue to be allowed to introduce new evidence even if that evidence could have been presented to the PTO in the first instance, subject only to the limits imposed in all civil actions by the Federal Rules of Evidence, the Federal Rules of Civil Procedure, and traditional principles of equity; and

2. When new evidence is introduced under § 145, the district court may continue to decide *de novo* the factual questions to which the evidence pertains, without giving deference to the prior decision of the PTO.[3]

---

3. The Court's second *certiorari* question is directed to whether the district court may decide *de novo* the factual questions to which new evidence pertains, when new evidence is presented. AIPLA does not interpret that question to be addressed to the broader issue of whether the introduction of new evidence requires *de novo* review of each factual question even if that new evidence does not pertain to a particular factual question. AIPLA thus expresses no opinion on that broader issue. In addition, since this Court's *certiorari* grant, §§ 141 and 145 were amended by Pub L. 112-29, enacted Sept. 16, 2011. The amendments did not affect the statutory text relevant to the *certiorari* questions this Court posed and this case arose under the previous law, so citations to these sections are not under the newly revised statutes.

ARGUMENT

I. The law appropriately permits a district court to receive and assess evidence in a § 145 action without being hobbled by the government's proposed restrictions on new evidence.

By its plain terms, a § 145 proceeding is a "civil action" brought by a patent applicant that grants the district court authority to "adjudge that such applicant is entitled to receive a patent for his invention, as specified in any of his claims involved in the decision of the Board of Patent Appeals and Interferences, as the facts in the case may appear."[4] As confirmed by jurisprudence for over a century from this Court and for nearly thirty years from the Federal Circuit, that statutory grant is free of the strictures that the government would now impose. The government's arguments, whether grounded in law or policy, provide no reason to cabin the district court's statutory authority.

A. The positive law does not reflect the government's proposed changes.

1. This Court's jurisprudence has not imposed or even suggested those restrictions.

In case law that stretches back for more than a century regarding § 145 and its predecessor statute, Revised Statutes § 4915 (1878), this Court has recognized

4. 35 U.S.C. § 145.

the right to introduce new evidence in the district court.[5] In none of them did this Court impose the additional, novel, and non-textual qualifications on that right that the government now purports to identify.

Most recently, this Court recognized in *Zurko* that only § 145 civil actions, as opposed to § 141 appeals, "permit[] the disappointed applicant to present to the court evidence that the applicant did not present to the PTO."[6] Importantly, there this Court taught that the presence of such new or different evidence necessarily transformed the district judge's job from simply reviewing the facts as the PTO found them, which is the function the Federal Circuit serves in a § 141 appeal, to finding the facts in the first instance: "The presence of such new or different evidence *makes a factfinder of the district judge.*"[7]

That description of the judicial function in a § 145 action reinforces this Court's prior such descriptions.

---

5. *Dickinson v. Zurko*, 527 U.S. 150, 164 (1999); *Hoover v. Coe*, 325 U.S. 79, 83 (1945); *Butterworth v. Hoe*, 112 U.S. 50, 61 (1884). Section 145 is the current embodiment of a statutory provision that has authorized a judicial remedy for decisions of the PTO since 1836, when Congress first created an agency responsible for examining patents. Although Congress amended various other aspects of § 145's predecessor during the 19th and early 20th centuries, the language defining the proceeding has remained essentially unchanged. *See* GOV'T'S OPENING BR. at 4-5 (summarizing the statute's history).

6. *Zurko*, 527 U.S. at 164 (emphasis supplied) (citing *Gould v. Quigg*, 822 F.2d 1074, 1077 (Fed. Cir. 1987)).

7. *Id.* (emphasis supplied; citation omitted).

Some 50 years earlier, this Court unanimously explained in *Hoover* that

> [i]t is evident that *alternative rights of review are accorded an applicant*,—one by appeal to the [Federal Circuit's predecessor], the other by bill in equity filed in one of the federal district courts. In the first the hearing is summary and solely on the record made in the [PTO]; in the other *a formal trial is afforded on proof which may include evidence not presented in the [PTO]*.[8]

And in 1884, this Court also drew those same distinctions in *Butterworth*, the first case in which it discussed § 145's predecessor, R.S. § 4915. There, this Court explained, again without dissent, that the statute authorized

> a proceeding in a court of the United States having original equity jurisdiction under the patent laws, according to the ordinary course of equity practice and procedure. *It is not a technical appeal* from the [PTO], like that authorized in section 4911, confined to the case as made in the record of that office, *but is prepared and heard upon all competent evidence adduced, and upon the whole merits*.[9]

In sum, in an unbroken string of case law dating back more than a century and a quarter, this Court has

---

8. *Hoover*, 325 U.S. at 83 (emphasis and brackets supplied; citations omitted).

9. *Butterworth*, 112 U.S. at 61 (emphasis and brackets supplied).

described § 145 or its predecessor statute as "permit[ting] the disappointed applicant to present to the court evidence that the applicant did not present to the [PTO]," that the "proof . . . may include evidence not presented in the [PTO]," that the case is to be both "prepared and heard upon *all competent evidence* adduced and *upon the whole merits*" – and that "[t]he presence of such new or different evidence makes a factfinder of the district judge." Section 145 actions, as "civil actions," are necessarily subject to the limits imposed on all civil actions by the Federal Rules of Evidence, the Federal Rules of Civil Procedure, and traditional principles of equity.[10] But in none of this Court's prior analyses of § 145 or its predecessor did this Court impose the additional limitations that the government now seeks.

The government's response to this line of deep-rooted, unbroken precedent is to assert, in effect, that this Court did not mean what it said – that the issue has remained open for more than a century because this case's precise factual circumstances had not previously been presented.[11] That argument is like the one recently made and unanimously rejected in another patent case, *Microsoft v. i4i*.[12] There, as here, "nearly a century of case law from this Court" had articulated a rule on a patent issue (there, that invalidity had to be shown by clear and convincing

---

10. *See* Fed. R. Ev. 101 & 102; Fed. R. Civ. P. 1 & 2.

11. GOV'T'S OPENING BR. at 4 (discussing *Zurko*) & 33-34 (discussing *Butterworth* and *Hoover*).

12. *Microsoft Corp. v. i4i Ltd. P'ship*, 564 U.S. ___, 131 S. Ct. 2238 (2011).

evidence).[13] There, as here, the petitioner argued that the rule applied only in the narrow factual circumstances in which this Court had explained the rule.[14] There, this Court unanimously rejected the petitioner's argument: "Squint as we may, we fail to see the qualifications that [the petitioner] purports to identify in our cases."[15] The qualifications in the law that the government purports to identify are likewise absent here and should be rejected.

The government's argument relies very heavily on *Morgan v. Daniels*, 150 U.S. 120 (1894).[16] But the Court did not there impose the limitations that the government now seeks. Indeed, the proceeding in *Morgan* is now governed by a separate statute, 35 U.S.C. § 146, which specifically allows the parties to introduce new evidence. *Morgan* is thus poor authority for the proposition that in a § 145 action there are patent-law-specific limits on what evidence the district court may consider when adjudicating entitlement to a patent.

Finally, the government's cramped view of the judicial authority that § 145 confers is in tension with the "well-settled presumption favoring interpretations of statutes that allow judicial review of administrative action . . . ."[17] The government's proposal hobbles, rather than enables, judicial review of administrative action.

---

13. *Id.* at 2245.

14. *Id.* at 2247.

15. *Id.*

16. *E.g.*, GOV'T'S OPENING BR. at 16-18 & 31-34.

17. *McNary v. Haitian Refugee Ctr., Inc.*, 498 U.S. 479, 496 (1991) (citations omitted).

2. There was no settled practice in the regional appellate courts for Congress to adopt.

In seeking to exclude evidence from the district court's "adjud[ication] . . . as the facts in the case may appear," the government posits that before § 145's passage in 1952 there was a "settled" judicial construction of its predecessor statute in the regional appellate courts, and that Congress implicitly adopted that construction in enacting § 145.[18]

Not so. Judicial construction of § 145 in the lower appellate courts was not uniform before 1952, as the government's brief concedes in a footnote.[19] In point of fact, it was in disarray. Some circuits allowed new evidence even if not presented to the PTO. For example, the Third Circuit, which encompassed the then-commercially significant and sophisticated states of Delaware and Pennsylvania, refused in a 1946 case to exclude such evidence because to do so "would be to change the nature of an R.S. Section 4915 proceeding and to rewrite the statute."[20] Consistent with the Third Circuit's approach in that case, the Seventh Circuit once cited a leading patent treatise published in 1937 that explained that "[i]t appears that, in general, evidence not previously presented in the

---

18. GOV'T'S OPENING BR. at 30 ("settled"), 35 n.8 ("consensus"), and 35 n.8 ("prevailing").

19. *Id.* at 35 n.8 (conceding a "lack of uniformity") & 37 n.9 (conceding that courts in various circuits allowed new evidence when no party objected to it).

20. *Minn. Mining & Mfg. Co. v. Carborundum Co.*, 155 F.2d 746, 748 (3d Cir. 1946).

[PTO] proceeding was not excluded from consideration for that reason, if otherwise admissible. Deller's Walker on Patents, 970, 3197 (1937 ed.)."[21]

Other decisions admitted the new evidence but discounted it because it had not been introduced below.[22] Some excluded it, but did so based on a variety of standards that included: estoppel[23]; bad faith[24]; intent to suppress[25]; or even mere negligence.[26] Given this patchwork, it would not have been possible for Congress implicitly to have adopted a settled standard, because one did not exist.

3. The government's imprecise, amorphous proposed change would invite intrusive and expansive collateral litigation.

The government proposes that § 145 be interpreted to allow new evidence only if its proponent had "no

---

21. *Velsicol Chem. Corp. v. Monsanto Co.*, 579 F.2d 1038, 1043 (7th Cir. 1978) (emphasis supplied).

22. *E.g., Western Elec. Co. v. Fowler*, 177 F. 224, 228-229 (7th Cir. 1910); *Standard Cartridge Co. v. Peters Cartridge Co.*, 77 F. 630, 638-639 (6th Cir. 1896).

23. *Barrett Co. v. Koppers Co.*, 22 F.2d 395, 397 (3d Cir. 1927).

24. *Knutson v. Gallsworthy*, 164 F.2d 497, 508-509 (D.C. Cir. 1947).

25. *Schilling v. Schwitzer-Cummins Co.*, 142 F.2d 82, 85 (D.C. Cir. 1944).

26. *Cal. Research Corp. v. Ladd*, 356 F.2d 813, 820-821 (D.C. Cir. 1966).

reasonable opportunity to present it to the PTO."[27] As an initial matter, the government's brief provides no guidance about the specific or even the general parameters of what constitutes a "reasonable opportunity." The phrase is inherently imprecise and raises a host of questions.

Consider just two examples. Suppose an applicant's counsel, guided by the Federal Circuit's admonitions in case law and the government's as *amicus curiae* in a recent case against larding the PTO's records with excessive materials,[28] makes the reasoned judgment, discussed with the applicant, that the existing record suffices to prove a point, but that judgment proves incorrect. Would the "reasonable opportunity" standard require discovery about those attorney-client communications or about counsel's reasons for not submitting the information? Given that the applicant was trying to comply with appellate guidance, is that a "reasonable opportunity"?

Or suppose, as is quite common, that an applicant's budgetary constraints prevented him from searching for art to respond to a PTO objection. Suppose further that later, in § 145 litigation, after the application had become more commercially important, those budgetary

---

27. *E.g.*, GOV'T'S OPENING BR. § III.

28. *See, e.g., Molins PLC v. Textron, Inc.*, 48 F.3d 1172, 1183-1184 (Fed. Cir. 1995) (affirming finding of inequitable conduct in part because the applicant submitted too many references); *Therasense, Inc. v. Becton, Dickinson & Co.*, 649 F.3d 1276, 2011 WL 2028255 at *9 (Fed. Cir. 2011) (*en banc*) (disapproving of the practice by which "patent prosecutors regularly bury PTO examiners with a deluge of prior art references, most of which have marginal value.") (citing *amicus curiae* brief of United States).

constraints were no longer present, and that important, dispositive art is thereby discovered. Did the applicant have in those circumstances a "reasonable opportunity" to present it? If so, why should a private applicant's fluctuating budget issues determine the important public question of whether that applicant is entitled to a patent by preventing the district court from considering new and important art?

"Reasonable opportunity" is an inherently imprecise phrase – one that is absent from § 145's text, this Court's prior guidance about its contours, and decades of Federal Circuit jurisprudence. The phrase does, however, appear elsewhere in federal statutes and case law, and its presence invariably causes protracted litigation in both the district court and the relevant federal appellate court over whether a given set of facts is within or without its boundaries.[29] There is no good reason in law, logic, or policy to engraft that imprecise, resource-draining requirement onto § 145.

B. The policy rationales that the government identifies to support its non-statutory argument are not compelling.

The government advances various policy rationales for the new, non-statutory regime that it seeks. None offer a compelling reason to depart from the statute's text, this Court's prior guidance, or settled case law regarding whether new evidence can be introduced in a § 145 civil action.

---

29. *See, e.g., Taylor v. Fed. Nat. Mortg. Ass'n*, 374 F.3d 529, 534-535 (7th Cir. 2004); *Fed. Commc'ns Comm'n v. WJR, The Goodwill Station*, 337 U.S. 265, 283 (1949).

1. The government's proposed change would upset settled expectations in the patent community.

As this Court has wisely and without dissent counseled in both *Festo* and *Warner-Jenkinson*, "courts must be cautious before adopting changes that disrupt the settled expectations of the inventing community."[30] This important principle, not mentioned in the government's brief, applies with special force here because the Federal Circuit, since shortly after its creation in 1982, has consistently allowed new evidence to be introduced in § 145 actions. In doing so, it has not imposed or even suggested the limitations on the parties' use of that evidence or the district court's consideration of it that the government now seeks to impose.

For example, in 1985, the Federal Circuit cited *Hoover* and other cases from this Court to explain that in a § 145 action "the parties are entitled to submit additional evidence," without the limitations the government now seeks.[31] Indeed, there the district court had allowed a new expert's declaration and a new theory – without, insofar as the opinions disclose, objection from the government.[32] Such jurisprudence continues unbroken into

---

30. *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 535 U.S. 722, 739 (2002) (citing *Warner-Jenkinson Co. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 28 (1997)).

31. *Fregeau v. Mossinghoff*, 776 F.2d 1034, 1036-1037 (Fed. Cir. 1985).

32. *Id.* at 1036.

this century.[33] As that case law's roots strengthened and deepened over the last three decades, the law recognized and acknowledged that § 145 actions confer "a powerful advantage over the patent examiner and the Board" precisely because the court can consider evidence not before the PTO – including, importantly, live witness testimony, which this Court has described as "'the greatest legal engine ever invented for the discovery of truth.'"[34] (Indeed, this Court long ago acknowledged the "treacherous" nature of deciding legal "issues of public moment" on the basis of a paper record rather than through testimony presented in open court.[35]) In one of those § 145 cases, the government, in stark contrast with its current position,[36] engaged an expert in the district

---

33. *See, e.g.*, *Titanium Metals Corp. of Am. v. Banner*, 778 F.2d 775, 777-778 (Fed. Cir. 1985) (new expert testimony without objection from the government); *Gould v. Quigg*, 822 F.2d 1074, 1076 (Fed. Cir. 1987) (both the applicant and the government introduced new evidence); *Burlington Indus., Inc. v. Quigg*, 822 F.2d 1581, 1584 (Fed. Cir. 1987) (government cross-examined the applicant's trial witnesses); *Newman v. Quigg*, 877 F.2d 1575, 1579 (Fed. Cir. 1989) (government engaged expert for new tests); *Mazzari v. Rogan*, 323 F.3d 1000, 1004-1005 (Fed. Cir. 2003) (allowing new experts and prior art references); *Takeda Pharm. Co., Ltd. v. Doll*, 561 F.3d 1372, 1374 (Fed. Cir. 2009) (allowing new expert declaration).

34. *White v. Illinois*, 502 U.S. 346, 356 (1992) (quoting *California v. Green*, 399 U.S. 149, 158 (1970)).

35. *Eccles v. Peoples Bank of Lakewood Village*, 333 U.S. 426, 434 (1948).

36. *Cf. Comm'r v. Schleier*, 515 U.S. 323, 334 n.7 (1995) ("In view of the Commissioner's differing interpretations of her own regulations, we do not accord her present litigating position any special deference.").

court to conduct extensive tests, which cost more than one hundred thousand dollars, on an embodiment of the patent and to testify and introduce exhibits about those tests.[37]

It is correct, as explained above in § I(A)(2), that before the Federal Circuit's creation, the § 145 jurisprudence about whether new evidence could be introduced was in disarray in the regional appellate courts (albeit not in this Court). That prior disarray underscores the point. In creating the Federal Circuit, Congress noted the "disuniformity" in the regional appellate courts's treatment of patent issues.[38] In particular, Congress observed that certain core issues were "too dependent upon geography . . . to make effective business planning possible."[39] Congress created the Federal Circuit "'to reduce the widespread lack of uniformity and uncertainty of legal doctrine that exist in the administration of patent law.'"[40] The Federal Circuit has brought clarity and certainty to this area of the law, in a manner that reflects fidelity to the statutory text and to this Court's precedent. Generations of inventors and investors in the patent community have acted on the

---

37. *Newman v. Quigg*, 681 F.Supp. 16, 19-21 (D.D.C. 1988) (§ 145 trial), *aff'd*, 877 F.2d 1575. After Mr. Newman lost his appeal, he litigated the reasonableness of the government's $103,015.48 in § 145 expenses conducting those tests. A bankruptcy court discharged that debt and the parties jointly dismissed the appeal to the Federal Circuit from the judgment awarding those costs. *Newman v. Quigg*, 923 F.2d 868 (Fed. Cir. 1990) (non-precedential decision; *see* Fed. Cir. L. R. 47.8(b)).

38. H.R. Rep. No. 97-312, at 20-21 (1981).

39. *Id.* at 20-22.

40. *Christianson v. Colt Industries Operating Corp.*, 486 U.S. 800, 813 (1988) (quoting H.R. Rep. 97-312, at 23 (1981)).

assumption that the clarity and stability will continue. Those settled expectations are best left undisturbed.

2. The government's proposed change would have effects beyond patent law – or would create a patent-specific standard.

The government's new rule might also disturb the trademark community's settled expectations, because § 145 has a trademark analog with the same material language and a similar purpose: 15 U.S.C. § 1071(b). It also provides that a person "dissatisfied" with the PTO's decision "may . . . have remedy by a civil action" and that the "court may adjudge that an applicant is entitled to [the intellectual property right] . . . as the facts in the case may appear."[41] It is generally appropriate to interpret statutes with the same material language and similar purposes to have the same meaning.[42] Appellate courts from around the country have interpreted § 145's trademark law analog to allow new evidence to be introduced in the district court, without the government's new limitations.[43]

---

41. 15 U.S.C. § 1071(b)(1). Appendix A hereto compares the text of the analogous patent and trademark stautes.

42. *E.g.*, *Smith v. City of Jackson, Miss.*, 544 U.S. 228, 233 (2005); *Holmes Group, Inc. v. Vornado Air Circulation Sys., Inc.*, 535 U.S. 826, 829-830 (2005).

43. *Aktieselskabet AF 21. November 2001 v. Fame Jeans Inc.*, 525 F.3d 8, 13 (D.C. Cir. 2008) ("the court may consider . . . new evidence that [was] not before the [Trademark Trial and Appeal Board] TTAB") (brackets supplied); *Kellogg Co. v. Toucan Golf, Inc.*, 337 F.3d 616, 623 (6th Cir. 2003) ("A disappointed party may present new evidence before the district court that was not presented to the TTAB") (citing *Zurko*); *CAE, Inc. v. Clean*

The substantial body of trademark law, especially when read together with this Court's prior pronouncements regarding § 145, the statute's predecessor, and settled Federal Circuit law in the § 145 context, counsels towards a construction of § 145 by this Court that allows district courts to consider new evidence, regardless whether the evidence could have been introduced below.

The government may argue that § 145 and its trademark analog, § 1071(b), should be construed differently despite the fact that their text, as is relevant here, is the same (*see* Appendix A). But that argument would fly in the face of

---

Air Eng'g, Inc., 267 F.3d 660, 673 (7th Cir. 2001) (§ 1071(b)(1) "allows the parties to request additional relief and to submit new evidence"); *PHC, Inc. v. Pioneer Healthcare, Inc.*, 75 F.3d 75, 80 (1st Cir. 1996) ("the Board's findings can be challenged in a civil action in district court through new evidence"); *Goya Foods Inc. v. Tropicana Prod., Inc.*, 846 F.2d 848, 853 (2d Cir. 1988) ("additional cross-examination and presentation of additional testimony is permitted"(quotation omitted)); *Noah's, Inc. v. Nark, Inc.*, 728 F.2d 410, 410 (8th Cir. 1984) (affirming district court's consideration of "additional evidence introduced by the parties"); *Gillette Co. v. '42' Prod. Ltd.*, 435 F.2d 1114, 1117 (9th Cir. 1970) (§ 1071(b)(1) "provides the dissatisfied party with a trial *de novo* and the opportunity to present new evidence"); *see generally 3 McCarthy, Trademarks And Unfair Competition* § 21.20 (4th ed. 2010).

Indeed, there are additional compelling justifications for the introduction of additional evidence and *de novo* review in §1071(b) actions. For example, a dissatisfied opposer or applicant in a §1071(b) action often adds claims relating to use of the mark (*e.g.*, trademark infringement, fair use, and the like), which the Trademark Trial and Appeal Board has no authority to adjudicate as its jurisdiction governs solely the registration of marks. *See generally* Trademark Trial and Appeal Board Manual of Procedure §§ 102.1 & 311.02(b) (3rd ed. 2011).

the established statutory construction rules for similarly worded statutes.[44] That argument, if accepted, would create the type of patent-only judicial standards that this Court has strongly counseled against.[45]

3. Administrative exhaustion principles do not nestle comfortably in § 145's statutory structure.

The government's main argument is that the principles underlying the doctrine of administrative exhaustion counsel that § 145 be construed to allow new evidence only when the applicant did not have a reasonable opportunity to present the evidence below.[46] This thesis can be tested with negative evidence: the absence of a condition when, if the thesis were true, that condition would be present. (This methodology was memorably employed in the Sherlock Holmes classic, "The Adventure of Silver Blaze," where Mr. Holmes knew a fact was true because a dog did not bark.) Tellingly, § 145 has been on the books since 1952, but the government's brief cites no case holding that administrative exhaustion principles, long a feature of federal law, apply to § 145.

---

44. *See* note 42, *supra*.

45. *E.g.*, *eBay, Inc. v. MercExchange, LLC*, 547 U.S. 388 (2006) (disapproving of patent-specific permanent injunction standards); *MedImmune, Inc. v. Genentech, Inc.*, 549 U.S. 118 (2007) (disapproving of patent-specific declaratory judgment standards); *Holmes Group*, 535 U.S. 826 (disapproving of patent-specific appellate jurisdiction standards).

46. Gov't's Opening Br. at 14-21.

There is a good reason for that half-century absence of any such case in the § 145 jurisprudence: administrative exhaustion principles do not mesh comfortably with the structure of a § 145 civil action in the district court. The government describes those principles as allowing the agency to: correct its own errors; apply its expertise and the statute in the first instance; and develop the factual background on which decision should be based.[47] But as this Court confirmed in *Zurko* (and in *Hoover* and *Butterworth* before it), a § 145 civil action contemplates an expanded factual record and a more robust judicial toolset when compared to a § 141 appeal – including, importantly, live testimony subject to cross-examination, which is not available in PTO proceedings. The import of the parties' ability to present, and district court's ability to assess, live testimony cannot be overstated, because most validity issues rest on issues of fact, either directly or because the question of law rests on underlying questions of fact.[48] Indeed, most patent law questions are resolved according to the understanding of the hypothetical person

---

47. GOV'T'S OPENING BR. at 22.

48. Obviousness by its terms depends on underlying questions of fact. *E.g.*, *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966). Anticipation is a question of fact, *e.g.*, *TriMed, Inc. v. Stryker Corp.*, 608 F.3d 1333, 1343 (Fed. Cir. 2010), as are written description, *e.g.*, *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1563 (Fed. Cir. 1991), the factors underlying the legal question of enablement, *e.g.*, *Alza Corp. v. Andrx Pharm., LLC*, 603 F.3d 935, 940 (Fed. Cir. 2010), and the factors underlying the legal determination of priority of invention, *e.g.*, *Price v. Symsek*, 988 F.2d 1187, 1190 (Fed. Cir. 1993). Many patent issues involve questions about what a reference teaches, and "'what a reference teaches is a question of fact.'" *TriMed*, 608 F.3d at 1341) (citation omitted).

of ordinary skill in the art at the time of the invention, which is itself a question of fact.[49]

The proposition that live testimony can and often does shed light on and resolve questions of fact requires no citation, although this Court's precedent confirms the proposition.[50] From the perspective of reliably assessing the issues of public moment that patent rights potentially implicate, § 145 actions offer a superior vehicle for resolution of the fact questions that are the basis of most validity issues, the PTO's asserted expertise notwithstanding.[51] Thus, § 145's statutory structure inherently dilutes, if not rejects in the first instance, the policy concerns that the government identifies.

Indeed, the government's proposed change could lead to perverse results. For example, suppose an applicant chose not to present evidence below because it was not relevant, or was only marginally so, to the issues before the PTO. Suppose further that that evidence turns out to bear trenchantly on the credibility of a key witness testifying in the § 145 action and, absent the government's proposed rule, that evidence would be otherwise admissible. Under the government's proposed rules, this dispositive evidence would be beyond the district court's consideration. That result is not tenable, particularly given that filing a patent application strips potential trade secret protection of any trade secrets thereby disclosed.[52]

---

49. *E.g.*, *Graham*, 383 U.S. at 17; *Alza*, 603 F.3d at 940.

50. *See White*, 502 U.S. at 356; *Eccles*, 333 U.S. at 434.

51. *See Eccles*, 333 U.S. at 434.

52. *See* notes 81 & 82 and accompanying text, *infra*.

That the government's thesis is not correct can also be tested by examining the government's cited authority. It holds that under traditional administrative exhaustion principles, "[w]hen material evidence that was previously unavailable is brought to the court's attention, the proper course is usually 'to remand to the agency for additional investigation or explanation.'"[53] But that authority is outside of the § 145 context. None of this Court's § 145 jurisprudence has suggested such a procedure, and manifestly § 145 does not contemplate it. The disconnect between that procedure and the procedure § 145 contemplates points firmly away from, not towards, the relevance of administrative exhaustion principles.

This is not to say that administrative exhaustion principles have no place in judicial analysis of PTO decisions. They do – but they apply in the alternate path that § 141 provides: an appeal to the Federal Circuit, instead of a civil action in the district court.[54]

4. The professed concern that applicants will "game" the system by reserving evidence ignores current law.

The government's brief also darkly warns that if this Court affirms the existing rule, applicants will "game" the system by reserving helpful evidence for the district court

---

53. GOV'T'S OPENING BR. at 22 (citing *Florida Power & Light Co. v. Lorion*, 470 U.S. 729, 744 (1985); *Tagg Bros. & Moorhead v. United States*, 280 U.S. 420, 444-445 (1930)).

54. *Cf. Zurko*, 527 U.S. at 152 (APA review standards apply in § 141 actions).

or even by "creat[ing] new evidence later."[55] As an initial matter, the warning is counterfactual. The Federal Circuit has for decades allowed new evidence in a § 145 action, and the government cites no evidence to show or even suggest that applicants have gamed the system. There is a reason for that lack of proof. Existing law provides severe potential penalties for intentionally not disclosing relevant information to the PTO. Intentional failure to disclose required information can under certain circumstances render the entire patent (or even an entire patent family) unenforceable.[56] But the problems that breach of that duty can create do not end there. Intentional nondisclosure can have further calamitous collateral effects, including creating liability for antitrust and unfair competition claims, liability for attorneys' fees under the exceptional case law, and creating a crime or fraud exception to the lawyer-client privilege.[57] Indeed, case law recognizes that the threat of unenforceability for an intentional failure to disclose – called the "atomic bomb" of patent law – can sometimes serve to swing the balance too far, towards over-disclosure.[58]

---

55. GOV'T'S OPENING BR. at 29-30 (brackets supplied).

56. An inequitable conduct finding can endanger a substantial portion of a company's patent portfolio. Unlike validity defenses, which are claim-specific, 35 U.S.C. § 288, inequitable conduct regarding any single claim makes the entire patent unenforceable, *Kingsdown Med. Consultants, Ltd. v. Hollister Inc.*, 863 F.2d 867, 877 (Fed. Cir. 1988), and indeed can extend from a single patent to render unenforceable other related patents and applications in the same technology family. *See, e.g., Consol. Aluminum Corp. v. Foseco Int'l Ltd.*, 910 F.2d 804, 808-812 (Fed. Cir. 1990).

57. *Therasense*, 649 F.3d 1276, 2011 WL 2028255 at *8.

58. *Id.* at *9.

In other words, given settled law and accepted judicial recognition of its practical effect on the very concern that the government identifies, the argument that applicants would try to "game" the system by intentionally withholding evidence from the PTO in order to present it in a § 145 action is not compelling.

The government's warning is also illogical even absent present penalties for intentional non-disclosure. If a patent application is potentially commercially significant enough to warrant the extra expense that a § 145 entails, the fact of its extra value would provide an especially compelling reason to disclose evidence to the PTO in the first instance – to optimize the chances of the PTO granting it.[59] To argue the contrary is like arguing that death penalty defendants have a greater incentive than other criminal defendants to withhold evidence for a later *habeus corpus* petition.

II. The law appropriately provides for the district court's *de novo* assessment of the factual issues raised in the PTO that the new evidence affects.

Like its arguments about the first *certiorari* question, the government's arguments on this second question, whether grounded in cases or policy, provide no reason to effect a dramatic change in course.

---

59. *Hyatt v. Kappos*, 625 F.3d 1320, 1337 (Fed. Cir. 2010) (*en banc*) (opinion below).

A. *De novo* assessment is the positive law.

1. *De novo* proceedings follow from the statutory text.

"Statutory construction must begin with the language employed by Congress and the assumption that the ordinary meaning of that language accurately expresses the legislative purpose."[60] The government's proposed limitations are not consistent with the statutory text and the legislative purpose it expresses, as a single example demonstrates.

Suppose a § 145 plaintiff introduces new evidence in the district court, and that the nature of that evidence is such that under a *de novo* standard the applicant would win but under a deferential standard he would lose. If the government's proposed limitations were correct, they would find support in the statutory text. But they do not. To the contrary, § 145 empowers the district court to "adjudge that such applicant is entitled to receive a patent for his invention, . . . *as the facts in the case may appear.*"[61] The statutory command that the district judge assess the "facts in the case" as they "may appear" implies an assessment of the facts as a whole, not an assessment in which some of the facts are viewed through a deferential lens and others accorded weight only insofar as they can overcome the force of that deference. Indeed, the statute refers to "the decision of the Board of Patent Appeals

---

60. *Engine Mfrs. Assn. v. South Coast Air Quality Mgmt. Dist.*, 541 U.S. 246, 252 (2004) (internal quotation marks and citation omitted).

61. 35 U.S.C. § 145 (emphasis supplied).

and Interferences" in the clause immediately before the command that the district court adjudge the issues "as the facts in the case may appear."[62] If Congress had intended the deference to that Board decision that the government now proposes, one would have expected the statute to mention it in a phrase such as "as the facts in the case, *with deference to the Board's findings*, may appear." But it does not. Instead, § 145 directs the district court to "adjudge" the issues "as the facts in the case may appear" to the court, unencumbered by the strictures that deferential review would impart.

2. *De novo* proceedings follow from this Court's precedent.

In addition to the statutory text, the logic of this Court's prior guidance in *Butterworth* sheds useful light. Based on that logic, such review is *de novo*. This Court there described an action under § 145's predecessor – in specific contrast to § 141's predecessor – as being "prepared and heard upon all competent evidence adduced *and upon the whole merits*."[63] Consideration of the "whole merits" implies a lack of deference, because where deference is applied, the whole merits of the facts before the court are not considered. Rather, the new facts are assessed only to see whether they can overcome the presumption that the PTO's decision was correct, under whatever level of deference is being applied.

This is not to say that the district court must, or indeed would be expected to, entirely disregard the PTO's

62. *Id.*

63. *Butterworth*, 112 U.S. at 61 (emphasis supplied).

findings on the issues to which the new evidence offered by the parties relates. The PTO's factual findings constitute relevant information, together with the newly offered evidence available to the district court as it undertakes its duty to adjudicate the facts on the complete record established in the § 145 action. To give one example: if an inventor submitted a declaration during prosecution (for example, to explain prior art), that inventor's credibility may be impeached either at deposition or at the trial of a § 145 action. In that circumstance, the district court would be able to consider the PTO's expertise and relevant findings along with the factual and credibility evidence developed through the inventor's testimony and cross-examination in its own fact findings.

3. *Morgan v. Daniels* (1894), upon which the government heavily relies, did not resolve the issue.

The government's brief argues at length that this Court's 1894 opinion in *Morgan v. Daniels* resolves the second *certiorari* question, which asks whether under § 145, which was passed in 1952, a district court may decide *de novo* fact questions to which new evidence pertains.[64] The argument is not compelling.

As an initial matter, it ignores *Morgan*'s limitations. There, the parties submitted the case to the trial court without any additional evidence.[65] In those circumstances, which are not presented by the second *certiorari* question, this Court concluded that deferential review was

64. *Morgan*, 153 U.S. 120; GOV'T'S OPENING BR. at 16-18.

65. *Morgan*, 153 U.S. at 122.

appropriate because it involved "a controversy between two individuals over a question of fact which has once been settled by a special tribunal, entrusted with full power in the premises."[66]

In contrast, the second *certiorari* question presumes new evidence, which means that the questions of fact to which the new evidence relates have not been "settled" but have merely been initially explored on an incomplete record. The second *certiorari* question raises an issue that *Morgan* did not begin to approach: given that the statute entrusts the district court with full power to "adjudge . . . [the case] as the facts in the case may appear," is any level of deference warranted where there is new evidence, such that the fact disputes affected by the new evidence cannot fairly said to have been settled?

On that question, this Court's later guidance is more illuminating. As this Court observed in *Hoover*, the statutory scheme contemplates "alternative rights" – those provided by § 141, and those provided by § 145.[67] It is settled that the former provides for deferential review.[68] There is no reason in law, logic, or policy to import deferential review into § 145 and thereby conflate the two. To the contrary, as this Court observed in *Butterworth* when contrasting the predecessors to § 141 and § 145, a § 145 action is "prepared and heard upon all competent

66. *Id.* at 124.

67. *Hoover*, 325 U.S. at 83 (emphasis supplied; citations omitted).

68. *E.g., Rasmusson v. SmithKline Beecham Corp.*, 413 F.3d 1318, 1320 (Fed. Cir. 2005) (PTO's factual findings upheld if supported by substantial evidence).

evidence adduced *and upon the whole merits*."[69] That is a distinction that the case law from this Court and from the Federal Circuit have preserved.

B. It is appropriate for the law to continue to permit the district court's *de novo* review.

1. Deferential review would upset settled expectations in the patent community.

As with the first *certiorari* question, the government's brief on the second does not address this Court's unanimous and wise counsel that "courts must be cautious before adopting changes that disrupt the settled expectations of the inventing community."[70] The Federal Circuit has long referred to the *de novo* nature of a § 145 civil action when the parties submit new evidence.

It did so at least twice in 1985, shortly after its creation.[71] And again two years later.[72] Indeed, the Federal Circuit emphatically made the point in a different decision in 1987. Quoting this Court's opinion in *Hoover*, the circuit wrote that trial *de novo* was a well-established § 145 right: "The right to a fresh look by a court of general jurisdiction, upon refusal by the Commissioner to grant a patent, has

---

69. *Butterworth*, 112 U.S. at 61 (emphasis supplied).

70. *Festo*, 535 U.S. at 739 (citing *Warner-Jenkinson*, 520 U.S. at 24).

71. *Fregeau*, 776 F.2d at 1038; *In re Newman*, 763 F.2d 407, 408-409 (Fed. Cir. 1985).

72. *Gould*, 822 F.2d at 1076-1077 (citing *Fregeau*, 776 F.2d at 1038; *Morgan*, 150 U.S. at 125).

long been established."[73] Noting that "[t]he district court conducted a full trial of the issues, a resource not available to the PTO," the circuit emphatically concluded that "[i]f the evidence adduced before the district court led to a decision different from that reached by the PTO, that is not contrary to the legislative purpose of section 145 *de novo* review. Indeed, it is in fulfillment of that purpose."[74] That consistent holding continued into the 1990s, and continues into the jurisprudence of this century as well.[75] Insofar as AIPLA is aware, no published Federal Circuit decision is to the contrary. Likewise, the dissenting opinion in the Federal Circuit *en banc* opinion cited to no such authority.[76]

Given the Federal Circuit's consistent precedent over the course of nearly three decades, it would be appropriate to apply here the important principle that the government's brief does not mention: the settled expectations of the patent community are best left undisturbed, and to do otherwise "risk[s] destroying the legitimate expectations of inventors in their property."[77]

---

73. *Burlington Indus., Inc. v. Quigg*, 822 F.2d at 1584.

74. *Id.* at 1584.

75. *In re Lueders*, 111 F.3d 1569, 1577 n.15 (Fed. Cir. 1997); *Brand v. Miller*, 487 F.3d 862, 867-868 (Fed. Cir. 2007); *Mazzari*, 323 F.3d at 1005; *In re Gartside*, 203 F.3d 1305, 1313 (Fed. Cir. 2000).

76. *Hyatt*, 625 F.2d at 1341-1358 (Dyk, J., dissenting).

77. *Festo*, 535 U.S. at 739.

2. The asserted "asymmetry" problem is illusory.

The government's brief observes that, as this Court confirmed without dissent in *Microsoft*, a patent cannot be invalidated absent clear and convincing evidence, even if the PTO did not consider the asserted evidence.[78] From that settled law, the government's brief repeatedly leaps to the conclusion that deferential review is required to produce "symmetry" between the standards of proof to invalidate a granted patent and the standards of proof to reverse the Board's denial of a patent application.[79] Although the argument has superficial linguistic appeal (it frames the issue as symmetry between the government's grant and its denial of a patent application), the argument does not withstand scrutiny.

As an initial matter, the government's argument cherry picks. When a party challenges the validity of a patent in district court proceedings, the admissibility of the evidence used to challenge that patent does not turn on whether the PTO considered it or had a reasonable opportunity to uncover it. To the contrary, the admissibility of that evidence is subject only to the limits imposed in all civil actions by the Federal Rules of Evidence, the Federal Rules of Civil Procedure, and traditional principles of equity.[80] But the government's response to the first *certiorari* question is that evidence is *not* admissible if the applicant could have presented it

78. Gov't's Opening Br. at 26.

79. *Id.* at 26-28.

80. *See* n.10, *supra*.

to the Board. If the government's requested symmetry were appropriate, the government's answer to the first *certiorari* question would have been the exact opposite: that, as in district court validity proceedings, the evidence is admissible subject to the normal judicial constraints.

The government's inconsistency serves to reveal that the symmetry that it seeks is not appropriate in the first instance. When the government grants a patent, it thereby grants a bundle of rights that this Court has repeatedly referred to as the "patent monopoly."[81] By contrast, when the government denies the grant of a U.S. patent on a patent application, no government rights are thereby conferred. The government's brief provides no reason to treat these two disparate circumstances the same. In addition, by filing a patent application, an applicant loses the trade secret protection of any of the information disclosed by the application.[82] Those trade secrets may represent valuable commercial rights that the applicant could reasonably choose to maintain as trade secrets and to forgo patent protection.[83] Given that filing the application necessarily entails relinquishing potentially important rights, the additional protection provided by the district court's *de novo* assessment of factual issues affected by new evidence is entirely appropriate.[84]

---

81. *E.g.*, *Festo*, 535 U.S. at 727; *Warner-Jenkinson*, 520 U.S. at 24.

82. *Kewanee Oil Co. v. Bicron Corp.*, 416 U.S. 470, 493 (1974) (noting the differences between the two areas of law).

83. *Id.* at 493-494 (Marshall, J., concurring).

84. *See Eccles*, 333 U.S. at 434.

Indeed, even on its own terms, the government's position does not achieve symmetry between the standards governing judicial assessment of the grant and the denial of a patent. To disturb the PTO's decision to grant a patent requires clear and convincing evidence.[85] The government urges that to disturb the PTO's decision to deny a patent, error should be established "by testimony which in character and amount carries thorough conviction."[86] But the government's brief omits that the "thorough conviction" standard has been likened to the "beyond a reasonable doubt" standard – and specifically distinguished from and contrasted with the "clear and convincing" standard.[87] The government's requested standard thus would still not achieve the symmetry that it says is appropriate.

3. The government's "variable standard of review" argument provides a solution in search of a problem.

As explained above, the decision below confirmed standards that flow from the statutory text, based on more than a century of this Court's jurisprudence and nearly three decades of Federal Circuit jurisprudence. Nonetheless, the government's brief urges this Court to replace it because, it argues, under such law the standard of review would "rise and fall with the facts of each case."[88]

---

85. *Microsoft*, 131 S. Ct. at 2242.

86. GOV'T'S OPENING BR. at 31.

87. *Price*, 988 F. 2d at 1193-1194; *but see Fregeau*, 776 F.3d at 1037-1038.

88. GOV'T'S OPENING BR. at 45.

Specifically, the government notes the settled law that if the parties in a § 145 civil action simply submit the PTO's record for the district court's review, the district will apply a deferential standard; but if either party submits new evidence, it will apply a *de novo* standard.[89] The "solution" the government proposes is to change the law so that the "thorough conviction" standard applies in all § 145 actions, regardless whether either of the parties introduce new evidence.[90]

This is a solution in search of a problem. As this Court long ago explained in *Butterworth*, and later confirmed in *Hoover* and *Zurko*, the alternatives currently reflected in § 141 and § 145 provide entirely different and mutually exclusive methods for applicants to seek judicial assessment of the PTO's decisions. If an applicant wishes simply to submit the record in the PTO without new evidence, there is a statute designed specifically for such assessment: § 141. But if the applicant has new evidence, § 145 provides for an alternative: a civil action in the district court. The government provides no reason why an applicant who seeks judicial review of the PTO record would avoid the statute designed for such review, and no evidence that dissatisfied applicants do so.

---

89. *Id.* at 44.

90. *Id.*

CONCLUSION

The limitations that the government proposes to place on the district court's power in a § 145 civil action are not supported by the statute's text, this Court's case law, the Federal Circuit's case law, analogous case law in the trademark context, or sound policy. An opinion from this Court confirming the Federal Circuit's analysis of the two *certiorari* questions is warranted. The Federal Circuit's analysis of those issues was right.

Respectfully submitted,

VERNON M. WINTERS
Counsel of Record
GREENBERG TRAURIG LLP
153 Townsend Street, 8th Floor
San Francisco, CA 94107
(415) 655-1300
wintersv@gtlaw.com

WILLIAM G. BARBER
PRESIDENT
AMERICAN INTELLECTUAL
PROPERTY LAW ASSOCIATION
241 18th Street, Suite 700
Arlington, VA 22202
(703) 415-0780

Attorneys for Amicus Curiae, American Intellectual Property Law Association

October 25, 2011

APPENDIX

APPENDIX A — RELEVANT STATUTES

35 U.S.C. § 145

An applicant ***dissatisfied with the decision*** of the Board of Patent Appeals and Interferences in an appeal under section 134(a) of this title may, unless appeal has been taken to the United States Court of Appeals for the Federal Circuit, ***have remedy by civil action*** against the Director in the United States District Court for the District of Columbia if commenced within such time after such decision, not less than sixty days, as the Director appoints. ***The court may adjudge*** that such applicant is entitled to receive a patent for his invention, as specified in any/of his claims involved in the decision of the Board of Patent Appeals and Interferences, ***as the facts in the case may appear***, and such adjudication shall authorize the Director to issue such

15 U.S.C. § 107(b)

Whenever a person authorized by subsection (a) of this section to appeal to the United States Court of Appeals for the Federal Circuit is ***dissatisfied with the decision*** of the Director or Trademark Trial and Appeal Board, said person may, unless appeal has been taken to said United States Court of Appeals for the Federal Circuit, ***have remedy by a civil action*** if commenced within such time after such decision, not less than sixty days, as the Director appoints or as provided in subsection (a) of this section. ***The court may adjudge*** that an applicant is entitled to a registration upon the application involved, that a registration involved should be canceled, or such other matter as the issues in the proceeding require, ***as the facts in the case may appear***. Such adjudication

patent on compliance with the requirements of law. All the expenses of the proceedings shall be paid by the applicant.

shall authorize the Director to take any necessary action, upon compliance with the requirements of law. However, no final judgment shall be entered in favor of an applicant under section 1(b) [15 USC 1051(b)] before the mark is registered, if such applicant cannot prevail without establishing constructive use pursuant to section 7(c) [15 USC 1057(c)].

AMICUS CURIAE BRIEF

RECORD
AND
BRIEFS

No. 10-1219

In the
Supreme Court of the United States

DAVID J. KAPPOS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR, PATENT AND TRADEMARK OFFICE,
Petitioner,

v.

GILBERT P. HYATT,
Respondent.

On Writ of Certiorari to the United States Court of Appeals for the Federal Circuit

BRIEF OF AMICUS CURIAE IEEE-USA IN SUPPORT OF NEITHER PARTY

CHRIS J. KATOPIS
Counsel of Record
1308 Clifton Street, N.W.
Washington, D.C. 20009
Tel. (202) 200-9490
chriskatopis@gmail.com

Counsel for Amicus Curiae
IEEE-USA

September 6, 2011

Becker Gallagher · Cincinnati, OH · Washington, D.C. · 800.890.5001

Library of Congress
Law Library

QUESTIONS PRESENTED

When the United States Patent and Trademark Office (PTO) denies an application for a patent, the applicant may seek judicial review of the agency's final action through either of two avenues. The applicant may obtain direct review of the agency's determination in the Federal Circuit under 35 U.S.C. § 141. Alternatively, the applicant may commence a civil action against the Director of the PTO in federal district court under 35 U.S.C. § 145. In a § 145 action, the applicant may in certain circumstances introduce evidence of patentability that was not presented to the agency. The questions presented are as follows:

1. Whether the plaintiff in a Section 145 action may introduce new evidence that could have been presented to the agency in the first instance.

2. Whether, when new evidence is introduced under Section 145, the district court may decide *de novo* the factual questions to which the evidence pertains, without giving deference to the prior decision of the PTO.

TABLE OF CONTENTS

QUESTIONS PRESENTED i

TABLE OF CONTENTS ii

TABLE OF AUTHORITIES iv

STATEMENT OF INTEREST OF *AMICUS CURIAE* 1

SUMMARY OF ARGUMENT 3

ARGUMENT 5

I. The Proper Construction of Patent Act § 145 Permits an Inventor to Introduce New Evidence During a Civil Action and its De Novo Judicial Review. 5

A. Statutory Construction of § 145 7

B. Intra-PTO Procedures Do Not Follow the APA Adjudicatory Model, so Some Recourse to *De Novo* Review on an Open Record is Necessary 11

C. Well-Established Canons of Statutory Construction Require that the term "Civil Action" Must Be Afforded a Single, Uniform Meaning Throughout the Patent Act 13

D. The Government's Interpretation of "Civil Action" Would Reduce § 145 to a Superfluity 17

II. The APA Itself Exempts § 145 "Special Statutory Review" From Closed-Record, Deferential Review 19

A. The Judicial Review Chapter of the APA Carves § 145 Out of the APA Closed-Record, Deferential Review Scheme ... 20

B. The APA Cannot Restrict an Inventor's Civil Action, Because the Board's Procedures Place the Board within the APA's Exceptions to § 706 21

III. The PTO and the Patent System Will Both be Harmed by a Restrictive and Narrow Interpretation of § 145 Limiting Scope and Nature of Review 22

CONCLUSION 28

TABLE OF AUTHORITIES

CASES

Atlantic Cleaners & Dyers, Inc. v. United States, 286 U.S. 427, 52 S.Ct. 607, 76 L.Ed. 1204(1932) 15

Bilski v. Kappos, 130 S.Ct. 3218 (2010) 2, 17

Brooke Group Ltd. v. Brown & Williamson Tobacco Corp., 509 U.S. 209, 113 S.Ct. 2578, 125 L.Ed.2d 168 (1993) 16

Butterworth v. Hoe, 112 U.S. 50 (1884) 10

Coffin v. Ogden, 85 U.S. 120, 18 Wall. 120 (1874) 14

Corley v. United States, 556 U. S. ___, ___ (2009) 17

Department of Revenue of Ore. v. ACF Industries, Inc., 510 U.S. 332, 114 S.Ct. 843, 127 L.Ed.2d 165 (1994) 15

Dickinson v. Zurko, 527 U.S. 150 (1999) 10, 19, 20, 21, 27

Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co., 535 U.S. 722 (2002) 2

Gayler v. Wilder, 10 How. 496 (1850) 14

Graham v. John Deere Co. of Kansas City,
383 U.S. 1 (1952) 5

Hague v. Committee for Industrial Organization,
307 U.S. 496 (1939) 17

Helvering v. Stockholms Enskilda Bank,
293 U.S. 84 (1934) 15

Hoover v. Coe,
325 U.S. 79 (1945) 10

Hyatt v. Doll,
576 F.3d 146 1274 (Fed. Cir. 2009) 18, 23

Hyatt v. Kappos,
625 F.3d 1320 (Fed. Cir. 2010) 4, 6, 27

In re Portola Packaging Inc,
110 F.3d 786 (Fed. Cir. 1997) 24

In re Ruschig,
379 F.2d 990 (CCPA 1967) 12

Koki v. Dudas,
556 F. Supp. 2d 41 (D.D.C. 2008) 18

Mazzari v. Rogan,
323 F.3d 1000 (Fed. Cir. 2003) 10

MGM Studios, Inc. v. Grokster, Ltd.,
545 U.S. 913 (2005) 2

Morgan v. Daniels,
153 U.S. 120 (1894) 8

Peyton v. Rowe,
391 U.S. 54 (1968) 11

Ramaprakash v. Federal Aviation Admin.,
346 F.3d 1121 (D.C. Cir. 2003) 13

SEC v. Chenery Corp.,
318 U.S. 80 (1943) 9

Stanford v. Roche Molecular Systems, Inc.,
131 S.Ct. 2188 (2011) 2

Sullivan v. *Stroop*,
496 U.S. 478 (1990) 16

Universal Camera Corp. v. Labor Bd.,
340 U.S. 474 (1951) 27

CONSTITUTION

U. S. Const., Art. I, § 8, cl. 8 5

STATUTES

5 U.S.C. §§ 555, 556, and 557 13

5 U.S.C. § 703 ..... 4, 19, 20

5 U.S.C. § 706 ..... *passim*

35 U.S.C. § 1, *et seq.* 5

35 U.S.C. § 2(b)(2)(A) 23

35 U.S.C. § 102 5

35 U.S.C. § 103 5

35 U.S.C. § 112 5

35 U.S.C. § 131 5

35 U.S.C. § 141 ..... *passim*

35 U.S.C. §§ 141-144 ..... 8, 9

35 U.S.C. § 143 ..... 8, 9

35 U.S.C. § 144 9

35 U.S.C. § 145 ..... *passim*

35 U.S.C. § 154 14

35 U.S.C. § 281 ..... 14, 16

35 U.S.C. § 291 14

35 U.S.C. § 297 ..... 14, 16

35 U.S.C. § 302 23

35 U.S.C. § 303 25

35 U.S.C. § 317 15

35 U.S.C. § 559 ..... 20, 21

Act of July 4, 1836, ch. 357, § 16, 5 Stat. 117 6

Act of March 2, 1861, ch. 88, § 2, 12 Stat. 246 6

LEGISLATIVE MATERIALS

H.R. 1249, 112th Cong. § 9 (2011) 11, 21

S. 23, 112th Cong. § 8 (2011) 11, 21

REGULATIONS

37 C.F.R. § 1.56 (1992) 22

37 C.F.R. § 41.50(b) 12

RULES

Sup. Ct. R. 37.6 1

PTO Rule 56 23

OTHER AUTHORITIES

Br.for the Director of the United States Patent and Trademark Office on Rehearing en Banc 2010 WL 2625006 *40 n.11 (C.A. Fed.) (May 3, 2010) 26

Br. of Amicus Curiae Fédération Internationale Des Conseils En Propriété Industrielle in Support of Neither Party on Rehearing en Banc, 2010 WL 2625004 at *10 (C.A.Fed.)(Apr. 7, 2010) 25

http://www.uspto.gov/ip/boards/bpai/procedures/rules/memorandum_roundtable_two_week_follow_up_030510.pdf 26

Industrial Property Law N° 9279/96 OF 14th MAY 1996 (Published on 15th May, 1996) (Brazil) . . 6

U.S. Patent and Trademark Office: Operations and Fiscal Year Year 2003 Budget: Before the H. Judiciary Subcomm. On Courts, the Internet, and Intellectual Property, 107th Cong. 7 (2002) (prepared statement of the Under Secretary of Commerce and Director of the USPTO) 26

USPTO ANNUAL PERFORMANCE AND ACCOUNTABILITY REPORT: FISCAL YEAR 2010, http://www.uspto.gov/ip/boards/bpai/procedures/rules/memorandum_roundtable_two_week_follow_up_030510.pdf 26

WEBSTER'S NEW INTERNATIONAL DICTIONARY OF THE ENGLISH LANGUAGE 492 (G. & C. Merriam Co.) (2d ed. 1948) 6, 10

Whitmer and Crall, *Is A § 145 Action More A "Trial" in the District Court or an Appeal in a Circuit Court?* The Federal Circuit Answers in Favor of Trial, INTELL. 23 PROP. & TECH. L.J. 15, 18 (2011) 23

STATEMENT OF INTEREST OF *AMICUS CURIAE*[1]

IEEE-USA is an organizational unit of The Institute of Electrical and Electronics Engineers, Inc. (IEEE), a New York-based not-for-profit, which is the world's leading educational and scientific association for the advancement of technology. IEEE-USA supports the nation's prosperity and competiveness by fostering technological innovation for the benefit of all, including more than 200,000 engineers, scientists, and allied professionals who are U.S. members of the IEEE.

As part of its mission, IEEE-USA seeks to ensure that U.S. patent and copyright law serves to promote the progress of science and the useful arts consistent with the principles set forth by our Nation's Founders. IEEE's U.S. members serve on the "front line" of the United States copyright and patent system. Our membership includes inventors and software authors who create and use cutting-edge technology, who research and publish professional articles and journals, and who develop published standards that form the bases of widely adopted and critical technologies. In addition, IEEE-USA members are more than merely scientists and research engineers,

---

[1] Pursuant to Supreme Court Rule 37.6, counsel listed on the cover states that this brief was authored by *amicus curiae* and reviewed by counsel, and that counsel for a party did not author this brief in whole or in part. Nor did counsel for a party make a monetary contribution intended to fund the preparation or submission of the brief. In addition, all parties have consented to the filing of this *amicus* brief, and their consent letters are on file with the Clerk's office.

they are also entrepreneurs and employees of firms that acquire, license, and market patented works.

IEEE-USA recognizes that the promotion of progress requires a delicate balance of these group interests, and IEEE-USA consistently speaks for that balance. When a decision threatens to disrupt the nation's intellectual property system, IEEE-USA respectfully believes that it has the experience and perspective to aid the Court as it interprets the law to achieve the constitutional directive of promoting progress. It has done so previously as an *amicus* in *Stanford v. Roche Molecular Systems, Inc.*, 131 S.Ct. 2188 (2011), *Bilski v. Kappos*, 130 S.Ct. 3218 (2010), *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 535 U.S. 722 (2002), and *MGM Studios, Inc. v. Grokster, Ltd.*, 545 U.S. 913 (2005), suggesting balanced approaches consistent with those adopted by the Court.

IEEE-USA recognizes the important role of judicial review, as established by Congress in the 1836 Patent Act, as a check on the PTO's judgment, procedural regularity, and patent quality. First, this case raises crucial questions concerning the nature and scope of a civil action pursuant to the Act and an inventor's rights upon judicial review. The Patent Act provides a statutory basis for a disappointed patent applicant to introduce new evidence, and to have the evidence reviewed *de novo* by a district court. Second, the case will help define the PTO Director's ultimate rule-making authority under the Administrative Procedure Act (APA), especially concerning patent application examination processes and judicial review. This case deals with important substantive and procedural questions regarding inventors' rights and patent law,

areas of law important to IEEE-USA's members and the innovation ecosystem for scientists, engineers, entrepreneurs, and investors.

SUMMARY OF ARGUMENT

More than 175 years ago, Congress established a statutory framework permitting a disappointed inventor to obtain judicial review of a rejected patent application. This statutory framework authorizes a dual-track judicial review of the PTO's decision to reject a patent claim, with either an appeal to the Federal Circuit or a civil action in district court. All through this 175-year period, inventors have been permitted to introduce new evidence before the district court, as part of the civil action authorized by § 145 and its predecessors. The plain language of § 145, using such words as "civil action" and "as the facts may appear," draws a sharp contrast with §§ 141-144 and 5 U.S.C. § 706, which provide for "appeal" to the Federal Circuit on a "record" provided by the PTO. This Court and others federal courts have consistently concluded that the Patent Act permits the introduction of new evidence as part of a civil action, limited only by the Federal rules of procedure and evidence as they apply in any other civil action.

IEEE-USA believes that the scope and nature of a § 145 civil action should be left *status quo*. First, the long-standing interpretation of the Patent Act is supported by the plain text of the statute, the vast mainstream of canons and methodologies of interpretation employed by this Court, and a panoply of federal case law. Second, the PTO's procedures are inconsistent with the provisions of Chapter 5 of the Administrative Procedure Act (the provisions that

govern intra-agency adjudications. Thus § 706 is not always a good fit for review, and § 145 judicial review must provide a corresponding relief mechanism. Third, § 703 of the judicial review provisions of the APA carves out § 145 from the reach of closed-record, deferential review under § 706. Fourth, the consequences of narrowing the scope and nature of judicial review pursuant to a § 145 civil action are likely to have very negative and damaging effects on PTO operations and patent quality, in light of the whole of the patent system.

Accordingly, IEEE-USA asks this Court to reaffirm that an inventor in a § 145 action may introduce new evidence that could have been presented to the agency in the first instance. Second, when new evidence is introduced under § 145, the district court may decide *de novo* the factual questions to which the evidence pertains, without giving deference to the prior decision of the PTO.

The long-standing interpretation of § 145 of the Patent Act concerning the admissibility of evidence, as held by the Federal Circuit in *Hyatt en banc*, should remain in effect. Likewise the Court must permit the *de novo* review of an adverse Board decision, as advocated in Judge Newman's conclusion in her concurrence.

ARGUMENT

I. The Proper Construction of Patent Act § 145 Permits an Inventor to Introduce New Evidence During a Civil Action and its De Novo Judicial Review.

The U.S. Congress enacted the Patent Act, 35 U.S.C. §§ 1 *et seq.*, (the Act) to establish the rights of patent grantees and the procedures surrounding the patent examination and review process, pursuant to its authority under the Patent Clause, U. S. CONST., Art. I, § 8, cl. 8. In the course of the PTO's examination, a patent applicant must, *inter alia*, comply with the necessary statutory criteria to merit the grant of a patent.

The Patent Act provides that "[a] person shall be entitled to a patent unless," § 102, the claimed invention lacks novelty or is obvious in view of the prior art, *id.* at §§ 102 and 103. Section 131 states that the PTO "shall cause an examination to be made of the application," *id.* §131. The key questions of patentability, such as non-obviousness pursuant to § 103 and "written description" under § 112 ¶ 1, are largely factual inquiries. *Graham v. John Deere Co. of Kansas City*, 383 U. S. 1, 17, 18, (1952) ("[T]he scope and content of the prior art are . . . determined; differences between the prior art and the claims at issue are . . . ascertained.") The PTO's determination of patentability often hinges on evidence proffered by the inventor and reviewed by the PTO, as the agency decision-maker.

More than a century before the 1946 enactment of the Administrative Procedure Act (APA), Congress

established judicial review of adverse PTO decisions through § 145's predecessor statutes. The *Hyatt en banc* opinion, parties, and *amici* describe the history of the Acts of Congress which gave rise to the modern § 145. *Hyatt v. Kappos*, 625 F.3d 1320, 1327 – 1330 (Fed. Cir. 2010). In 1836, Congress implemented a variety of major reforms to the U.S. patent system, including establishing the PTO and providing disappointed inventors the judicial review of a PTO adverse determination through the use of a "bill in equity" "whenever a patent on application shall have been refused on an adverse decision of a board of examiners." Act of July 4, 1836, ch. 357, § 16, 5 Stat. 117. Congress continued to provide the judicial review of adverse decisions of the PTO through subsequent enactments. The 1839 Patent Act expanded the "bill in equity" to address "all cases where patent are refused for any reason whatever, either by the Commissioner of Patents or by the Chief Justice of the District of Columbia." Act of March 2, 1861, ch. 88, § 2, 12 Stat. 246. The modern version of the statutory grant providing PTO judicial review may be traced to when Congress enacted the modern §145, as part of the 1952 Patent Act. At this juncture, in enacting the 1952 Patent Act, Congress used the term "civil action," in drafting § 145, *in lieu* of the term "bill in equity."[2]

---

[2] The leading contemporary U.S. dictionary at that time of the 1952's Act enactment provided the following definition for "civil action" as "[a]n action, suit, or proceeding to enforce the private rights or redress the private wrongs of an individual, that is, one not involving a criminal proceeding." WEBSTER'S NEW INTERNATIONAL DICTIONARY OF THE ENGLISH LANGUAGE 492 (G. & C. Merriam Co.) (2d ed. 1948). This authority was available to lawmakers enacting the 1952 Act, at the time. While some may read the term "civil action" narrowly, it simply means non-

A. Statutory Construction of § 145.

The Patent Act represents the manifestation of Congress' legislative will, *inter alia*, concerning the design and structure of the patent system. The Act provides disappointed inventors a dual-track for judicial review of adverse decisions of the PTO: first, §§ 141-144 provide appellate review by the U.S. Court of Appeals for the Federal Circuit; and, second, § 145 provides for a "civil action" in district court. The Patent Act's text provides no express limitations on a disappointed inventor pursuing relief through § 145 from either introducing new evidence at the district court or obtaining its *de novo* review. Further, no conventional methodology of statutory construction leads to this conclusion. This task requires neither a strict nor a lenient construction of the Patent Act, merely a reasonable one.[3]

---

criminal. Readers should be mindful that U.S. Patent Law historically has provided for the civil enforcement of patent rights. In contrast, other nations, such as Brazil, provide criminal sanctions for the violation of patent rights. (Art. 99 of the INDUSTRIAL PROPERTY LAW N° 9279/96 OF 14th MAY 1996 (Published on 15th May, 1996), Title V – Crimes Against Industrial Property - Brasil Patent Act, Article 183 – "A crime is committed against a patent of invention or a utility model patent by he who . . . [infringes] invention, without authorization of the patentee.")

[3] Section 145 is a remedial statute, as it provides judicial review from an adverse agency action. Many courts have applied the well-established canons permitting the liberal interpretation of remedial statutes.

This "water-and-oil" separation relationship between § 145 and the APA essentially codifies administrative law practices long held by this Court. In *Morgan v. Daniels*, 153 U. S. 120 (1894), the Court explained that the objective of an action under Revised Statutes § 4915 (1878) (R.S. 4915), § 145's predecessor, was to "set aside" the determination made by the "executive department . . . charged with the administration of the patent system." *Id.* at 124. In essence, Congress' plan was permitting the set aside of a defective decision of an executive branch agency.

The statutory language is quite clear that a § 145 civil action is not an "appeal" or "review" in the APA sense, but a *de novo* civil action on an open record. Nothing in the plain text of § 145 displaces the ordinary meaning of the term "civil action" in the way suggested by the PTO. Rather, a comparison of the text of § 145 against § 141-144 and 5 U.S.C. § 706(2), which govern a direct appeal to the Federal Circuit, shows the "oil from water" separation and contrast:

- Sections 141-144 repeatedly use the words "appeal" and "review." In contrast, § 145 never uses either "appeal" or "review" except to *contrast* appeal to the Federal Circuit. Section 145 instead provides "remedy by civil action." This difference in language shows that Congress intended § 145 to be a trial court, *de novo* proceeding, while appeal to the Federal Circuit is to be conducted on "appeal" rules.

- The scope of subject matter is different. Section 143 states that the Director of the PTO shall submit in writing "the grounds for the decision of the PTO" and the court shall "address all the issues

involved in the *appeal*." Section 143 aligns Federal Circuit review with the standard *Chenery* rule, which confines a court to review of the agency's grounds.[4] In contrast, § 145 obligates the district court to "*adjudge* ... as the facts in the case may appear," opening the proceeding to all relevant issues. (emphasis added).

- The relief is different. Section 144 only gives the Federal Circuit power to reverse the PTO's current grounds, essentially a *vacatur* with leave to the PTO to re-reject on new grounds. (This is discussed further in Section I.B of this brief starting at page 15.) Section 144 aligns with the power to "set aside" agency action in § 706(2). In contrast, § 145 gives the district court the power to "authorize the Director to issue such patent"—relief that is unavailable under § 141-44 or § 706(2). This different relief calls for a deeper review, on an open record.

- Sections 143 and 144 provide that the PTO is to deliver a closed record to the Federal Circuit, parallel to § 706 which confines an APA review to "the whole record or those parts of it cited by a party." In contrast, § 145 has no stated limit on the record, and invites proof of all "facts as they may appear." The contrasting language implies that the record is open to both the PTO and to the inventor.

---

[4] *SEC v. Chenery Corp.*, 318 U.S. 80, 95 (1943) ("an administrative order cannot be upheld unless the grounds upon which the agency acted in exercising its powers were those upon which its action can be sustained.")

This Court has frequently recognized that the difference in statutory language creates a difference in procedure—the record is open, and the standard of review is *de novo*, to a preponderance of the evidence. *Dickinson v. Zurko*, 527 U.S. 150, 164 (1999) (Section 145 "permits the disappointed applicant to present to the court *evidence that the applicant did not present to the PTO* . . . . The presence of such new or different evidence *makes a factfinder of the district judge*.") (emphasis added); *Hoover v. Coe*, 325 U.S. 79, 83 (1945) ("a formal trial is afforded on proof which may include *evidence not presented* in the Patent Office') (emphasis added); *Butterworth v. Hoe*, 112 U.S. 50, 61 (1884) ("This means a proceeding in a court of the United States having original equity jurisdiction under the patent laws, according to the *ordinary course of equity practice and procedure* . . . [it is] *not confined to the case made in the record* of that office, but it is prepared to be heard upon *all competent evidence* adduced, and *upon the whole merits.*")(emphasis added); *Mazzari v. Rogan*, 323 F.3d 1000, 1004-05 (Fed. Cir. 2003) ("A section 145 review . . . affords the applicant an opportunity to *present additional evidence* or argue the previous evidence afresh" and "[i]f the parties *choose to* present additional evidence to the district court . . . the district court would make *de novo* factual findings.") (emphasis added).

The modern version of §145 is largely unchanged since 1836, even though the successive statutes have been repeatedly amended to track system-wide changes in legal vocabulary, to substitute "civil action" for "bill in equity," and to track reorganizations of the federal court systems, and the like. The U.S. Congress is currently contemplating a significant reform of the Patent Act, which would amend § 145 to have these

cases heard in the U.S. District Court for the Eastern District of Virginia. (H.R. 1249, 112th Cong. § 9 (2011), S. 23, 112th Cong. § 8 (2011)). In view of a century of Congressional acquiescence to courts' consistent interpretations of this statute, that *status quo* should not be disturbed.

Finally, § 145 is a remedial statute, as it provides judicial review from an adverse agency action. Remedial statutes are to be liberally construed. *Peyton v. Rowe*, 391 U.S. 54, 64 (1968).

B. Intra-PTO Procedures Do Not Follow the APA Adjudicatory Model, so Some Recourse to *De Novo* Review on an Open Record is Necessary

PTO proceedings are necessarily very different than proceedings in other agencies. PTO proceedings are not a gradual winnowing and narrowing of issues through an adversarial process between trained advocates. Rather, PTO proceedings have been analogized to the carnival game of "Whack-a-Mole": the resolution of one ground of rejection merely causes the examiner to raise a new one, like a mole popping out of a new hole. Inventors are at the mercy of the PTO's constant shifts in position—and those shifts persist to the final stage of proceedings.[5] The notion of "evidence that could have been presented" is all but meaningless at the PTO: inventors often have *no notice* of the issues during the open-record phase of PTO proceedings.

---

[5] David Pressman, *Patent It Yourself*, at 339 13th ed. (Nol Press 2008).

Some part of this procedural deviation is a necessary evil, because of the PTO's unique role as a guardian of the public interest in an ex *parte* allocation of private rights. Because of this guardian role, the PTO frequently raises "new grounds of rejection" under 37 C.F.R. § 41.50(b), *injecting new evidence* adverse to the inventor, at the *very last stage* of agency proceedings, *after the intra-agency record is closed* to new evidence in favor of the inventor. Evidence for the pervasive aspects of this PTO practice is found in its appeal statistics indicating that in no less than 20%, and as much as 60%, of all cases decided by the Board, "new grounds of rejection" are invoked at the end of the appeal proceeding.[6] Because of the PTO's anomalous, asymmetric procedures, the law must provide the counterbalance of an open record, and consequently, *de novo* review.

The deviation from conventional APA Chapter 5 adjudication does not end with appeal. The law permits the PTO to reopen new issues *adverse to the inventor* at every phase. This includes the Board, despite statements and authority to the contrary. For example, in *In re Ruschig*, 379 F.2d 990, 992–93 (CCPA 1967), after an inventor's successful appeal to the Court of Customs and Patent Appeals, the PTO reopened prosecution, and re-rejected it, and on the

---

[6] Ron D. Katznelson, Comments submitted to OMB under the Paperwork Reduction Act on USPTO appeal rules, (Nov. 17, 2008), at 5. http://bitly.com/PRA-Appeal (Figure 3 showing under the headings "remand" and "modified" the flow of Board decisions invoking new grounds of rejection which are 20% of Board decisions. In addition, parts of decisions under the "Reversal in full" heading (40%) are later rejected by the examiner under new grounds.)

second trip to the CCPA, the court affirmed the PTO's power to do so. When intra-agency adjudications do not fit into the normal APA Chapter 5 mold, limited § 706 review is a poor fit.

Inventors are at the mercy of procedures that depart from the normal "winnowing" model of adjudication contemplated by 5 U.S.C. §§ 555, 556, and 557, procedures that asymmetrically prejudice inventors during intra-agency procedures. Some of these departures are necessary, some persist simply because agencies tend to "fall into grooves . . . and when they get into grooves, then God save you to get them out."[7] In § 145, Congress merely provided a procedural counterbalance by providing broader judicial review.

C. Well-Established Canons of Statutory Construction Require that the term "Civil Action" Must Be Afforded a Single, Uniform Meaning Throughout the Patent Act

The term "civil action" appears no fewer than ten times throughout the current Patent Act. The Act provides no express definition for the term. Accordingly the choice is either that the term "civil action" has one single, standard, uniform meaning throughout the Patent Act; or, in the alternative, the term "civil action" has multiple, and sometimes

---

[7] *Ramaprakash v. Federal Aviation Admin.*, 346 F.3d 1121, 1122 (D.C. Cir. 2003) (Roberts, J.), *quoting* Learned Hand, Hearings to Study Senate Concurrent Resolution 21 Before a Subcommittee of the Senate Committee on Labor and Public Welfare, 82nd Cong., 1st Sess. 224 (1951).

contradictory meanings throughout the Patent Act. The latter proposition is a legal infirmity that violates well-established methodologies of statutory construction.

The Patent Act must be construed as a whole. *Coffin v. Ogden*, 85 U.S. 120, 124, 18 Wall. 120, 124 (1874) (*citing Gayler v. Wilder*, 10 How. 496 (1850)) ("The whole [Patent] act is to be taken together and construed in the light of the context. The meaning of these sections must be sought in the import of their language, and in the object and policy of the legislature in enacting them.") The Patent Act uses the term "civil action" no fewer than ten distinct times, including

> *Section 154. Appeal of Patent Term Adjustment Determination.* An applicant dissatisfied with a determination made by the Director under paragraph (3) shall have remedy by a civil action against the Director filed in the United States District Court for the District of Columbia . . . .
>
> *Section 281. Remedy for infringement of patent.* A patentee shall have remedy by civil action for infringement of his patent.
>
> *Section 291. Interfering patents.* The owner of an interfering patent may have relief against the owner of another by civil action . . . .
>
> *Section 297. Improper and Deceptive Invention Promotion.* Any customer who enters into a contract with an invention promoter and who is found by a court to have been injured by any

> material false or fraudulent statement or representation, or any omission of material fact, by that invention promoter may recover in a civil action against the invention promoter . . . .; and
>
> *Section 317(b). Inter partes reexamination prohibited.* Once a final decision has been entered against a party in a civil action arising in whole or in part under section 1338 of title 28 . . . .

In each of the circumstances, a plaintiff seeks various remedies in federal court through a civil action. For the following reasons, it is obvious that the scope and nature of each district court civil action, *inter alia*, the introduction of new evidence, cannot vary from section to section.

The Patent Act is not an ink-blot where a term's meaning is in the eye of the beholder. The Court's methodology for interpreting statutes has warned against interpreting the identical term within the same act from having two different meanings. *Department of Revenue of Ore. v. ACF Industries, Inc.*, 510 U.S. 332, 342, 114 S.Ct. 843, 849, 127 L.Ed.2d 165 (1994) ("the 'normal rule of statutory construction' [means] that 'identical words used in different parts of the same act are intended to have the same meaning.'") (*quoting Helvering v. Stockholms Enskilda Bank*, 293 U.S. 84, 87 (1934) (*quoting Atlantic Cleaners & Dyers, Inc. v. United States*, 286 U.S. 427, 433, 52 S.Ct. 607, 609, 76 L.Ed. 1204 (1932). ('there is a natural presumption that identical words used in different parts of the same act are intended to have the same meaning.")); *see*

also Brooke Group Ltd. v. Brown & Williamson Tobacco Corp., 509 U.S. 209, 230, 113 S.Ct. 2578, 2591, 125 L.Ed.2d 168 (1993) ("We adhere to 'the normal rule of statutory construction that identical words used in different parts of the same act are intended to have the same meaning.'") (*quoting Sullivan* v. *Stroop*, 496 U.S. 478, 484 (1990) (internal quotations omitted)). In the alternative, two identical terms within the same statute may have different meanings based on some special qualifying text or, in unusual cases, some extrinsic or intrinsic support, such as legislative history. None is present here in connection with the Patent Act's use of "civil action."

We must be mindful that where the Patent Act provides for a plaintiff's introduction of new evidence and *de novo* review in a statute via a term in one particular section, then widely used canons of interpretation require that it must be used consistently throughout, unless otherwise so drafted. The Court's methodology for interpreting statutes has warned against interpreting a term within the same act having two separate meanings, without some special qualifying text or, in unusual cases, some extrinsic or intrinsic support, such as legislative history. None is present here in connection with the Patent Act's invocations of "civil action."

In the present instance, we can merely examine two instances of the Patent Act's use of "civil action" to compare against the alleged meaning in § 145. Congress uses the term "civil action" in a broad sense, including patent infringement cases in the federal district court, § 281, and against unscrupulous invention promotion fraudsters, § 297. The Patent Act provides that these federal district court proceedings

will permit the plaintiff to introduce new evidence without qualification and be afforded *de novo* review. Once again, the true commonality of the use of "civil action" in the Patent Act is in the sense of an open-record district court proceeding.

In light of a reading of the Patent Act as a whole, any interpretation of "civil action" pursuant to § 145 in the narrow and limited sense is illogical and inappropriate. A proper construction will neither preclude a plaintiff's introduction of new evidence nor prevent its *de novo* review. Any other reading is entirely inconsistent with these other Patent Act provisions and the respective meanings of "civil action" therein. It is a fatal legal infirmity and in violation of this Court's long-accepted statutory construction methodology.

D. The Government's Interpretation of "Civil Action" Would Reduce § 145 to a Superfluity

Recently in *Bilski v. Kappos*, 130 S.Ct. 3218 (2011), this Court adopted one of two statutory constructions by resort to a traditional canon of statutory interpretation, by rejecting a construction that "would violate the canon against interpreting any statutory provision in a manner that would render another provision superfluous . . . [t]his established rule of statutory interpretation cannot be overcome by judicial speculation as to the subjective intent of various legislators in enacting the subsequent provision." *Id.* at 3229 (*citing Corley v. United States*, 556 U. S. ___, ___ (2009); *Hague v. Committee for Industrial Organization*, 307 U. S. 496, 529–530 (1939)). Through the Patent Act's §§ 141 and 145, Congress provides

dual-track judicial review avenues for an inventor disappointed by an adverse PTO decision. The PTO's narrow and limited reading of § 145 precluding the introduction of new evidence would essentially create a duplicative judicial review process. This is because the inventor would be limited to essentially the same scope of evidence and nature of judicial review available on appellate review. As Judge Newman noted in her concurrence to the *en banc* opinion, "The statutory plan is designed to differ from such a duplicative procedure, not to create it." *Hyatt* at 1338 (Newman, J., concurring). *See Koki v. Dudas*, 556 F. Supp. 2d 41, 47 (D.D.C. 2008) ("render[ing] an appeal under section 145 nearly indistinguishable from a direct appeal to the Federal Circuit . . . would render the purpose of the statute duplicative and meaningless.")

The interpretative defect in reading §§ 141 and 145 as duplicative and redundant may also be illustrated by the ensuing impractical and illogical results for an inventor pursuing litigation. In the event that an inventor's choice of judicial review afforded under § 145 in the district court (where the record is closed and a *de novo* proceeding is unavailable). Simply put, no inventor would ever utilize the district court avenue if it were found to be redundant and duplicative. An inventor will always be better off pursuant to § 141 by seeking appellate review at the Federal Circuit, for example § 141 does not require payment of costs. Likewise, in the patent system, time is truly of the essence. The pursuit of a circuitous, time consuming civil action on a closed record will offer no benefit over a § 141 direct appeal. Worse, the extended delay will result in the term of a patent being truncated. An inventor will refrain from seeking the most time-

consuming and circuitous avenue, unless all other options are unavailable. Hence § 145 would be a redundant option, and thus statutorily meaningless. This resulting illogical and absurd consequence arising from the litigation dilemma is obvious and forbids such a reading of the statute.

Any proper reading of the APA must neither pursue a slavish adhesion to an abstract theory of law nor misconstrue the statute in an effort to tackle alleged policy or operational issues. Here, Congress has in fact crafted a statutory plan permitting a dual-track judicial review process that entails a different scope and nature for each track. Congress' intent must be respected and is consistent with the teachings of this Court.

II. The APA Itself Exempts § 145 "Special Statutory Review" From Closed-Record, Deferential Review

Congress established a special statutory review procedure for judicial review of a PTO adverse decision more than one hundred years before the Administrative Procedure Act (APA), 5 U.S.C. §§ 500 *et seq*. Several statutory provisions and holdings of this Court have noted that § 145 falls within the statutory carve-out from the closed-record, deferential review provisions of § 706.

In *Zurko*, the Court construed the APA's statutory plan for the review of agency fact finding. However, *Zurko* expressly *distinguished* § 145 civil actions from § 706/§ 141 appellate review by noting that § 145 "permits the disappointed applicant to present to the court evidence that the applicant did not present to the

PTO" and that "[t]he presence of such new or different evidence makes a factfinder of the district judge." *Zurko*, 527 U.S. at 164.

A. The Judicial Review Chapter of the APA Carves § 145 Out of the APA Closed-Record, Deferential Review Scheme

The APA preserves statutory review mechanisms – including those that, allow for trial *de novo*, such as § 145. 5 U.S.C. § 703 provides that where an agency is subject to a *sui generis* "special statutory review," the form of that review prevails, and that § 706 serves only as an interstitial "catch all" for issues that had not been reviewable before 1946:

> § 703. Form and venue of proceeding.
> The form of proceeding for judicial review is the *special statutory review* proceeding relevant to the subject matter in a court specified by statute . . . in a court of competent jurisdiction . . . .

5 U.S.C. § 703 (emphasis added).

Section 145 provides a full "civil action," so the fallback of limited, closed-record, deferential review of § 706 simply does not apply.

Furthermore, the APA's savings clause expressly provides that nothing in the judicial review provisions of the APA "limit[s] or repeal[s] additional requirements imposed by statute or otherwise recognized by law." 5 U.S.C. § 559. In the present case, the operative APA provision contemplating a procedure "otherwise recognized by law" is § 145. As

noted in the Federal Circuit's opinion, § 145 has been reenacted without material change since before 1946, and thus § 559 leaves previous procedure in place.

B. The APA Cannot Restrict an Inventor's Civil Action, Because the Board's Procedures Place the Board within the APA's Exceptions to § 706

In *Zurko*, the Court reasoned that the APA had several purposes and goals, including (1) maintaining a uniform approach to judicial review of administrative action and (2) bringing uniformity to a full field of variation and diversity. A conclusion permitting a § 145 plaintiff to introduce new evidence and to obtain its *de novo* review are consistent with those goals. Under the Patent Act, all § 145 civil actions will be heard in a single venue – presently the U.S. District Court for District of Columbia.[8] Accordingly the Patent Act's provision of a single venue preserves a uniform approach to judicial review of the PTO Board, and other important administrative law goals. Further, permitting an inventor to introduce new evidence in district court pursuant to § 145 serves an important administrative purpose. It will incentivize the PTO's examining corps and the Board to have more thorough and robust procedures for identifying *all* grounds of rejection *early* during prosecution. It will

---

[8] We observe that the U.S. Congress is currently contemplating a significant reform of the Patent Act, which would amend § 145 to have these cases heard in the U.S. District Court for the Eastern District of Virginia. (H.R. 1249, 112th Cong. § 9 (2011), S. 23, 112th Cong. § 8 (2011)). No legislative action has been directed to amending the definition of "civil action" or altering the related procedures.

level the playing field between the Board and the district court. This will enhance the PTO's thoroughness and competency. By permitting an inventor the opportunity to receive early notice of the grounds of rejection and introduce the same quantum of evidence sooner, rather than later, the record will be more inclusive and may even eliminate some costly §145 actions.

III. The PTO and the Patent System Will Both be Harmed by a Restrictive and Narrow Interpretation of § 145 Limiting Scope and Nature of Review

Foreclosing an inventor from introducing new evidence in a § 145 civil action not only violates the statutory scheme, but has practical effects that are burdensome and harmful to the patent system, to PTO operations, and to patent quality. Restricting the scope and nature of a district court civil action would require inventors overwhelm the PTO with evidence and materials, and sharply increase costs for many of the thousands of inventors per year who do *not* bring § 145 actions. Further, such a restriction would disturb decades of expectations and reliance by the bar, bench, and agency regarding proper procedures during the application process.

IEEE-USA and its members neither condone inventor misconduct nor gamesmanship at the PTO. On appeal, we advocate a balanced approach allowing new evidence pursuant to § 145, provided it is subject to checks and balances, such as the Federal rules of evidence and civil procedure. Further, in some instances the PTO may be able to regulate its practitioners and guard against the true bad actors

(*See* 35 U.S.C. § 2(b)(2)(d); PTO Rule 56; 37 C.F.R. § 1.56(1992))). However, a categorical or a bright line preclusion of new evidence that "could" have been presented in a civil action is unworkable for the innovation ecosystem because it requires impossible inventor foresight, immense prophylactic expense, and complexity. Balance often requires good judgment. As the Federal Circuit original three-judge *Hyatt* panel acknowledged, "beyond a certain point, how much more evidence to submit is in large part a determination for which a patentee and his agents must use good judgment." *Hyatt v. Doll,* 576 F.3d 146, 1274 (Fed. Cir. 2009)(*vacated*). Practitioners note a variety of reasons that a plaintiff pursuing state of the art technology may justifiably seek the introduction of new evidence, including:

> later-discovered prior-art, testimony of an expert on the person of ordinary skill in the art, and/or experimental test that could have been run while the application was before the PTO but was foregone in the hope that the test expense could have been avoided.

Whitmer and Crall, *Is A § 145 Action More A "Trial" in the District Court or an Appeal in a Circuit Court?* The Federal Circuit Answers in Favor of Trial, INTELL. 23 PROP. & TECH. L.J. 15, 18 (2011). As previously stated, a major goal of IEEE-USA is ensuring that the system offers the correct balance.

This fear has been realized. Several previous well-meaning law changes have had the unintended consequence of inventors flooding the PTO with prophylactic evidence, sometimes requiring a Congressional remedy. It is akin to an issue which

required Congress to address in the mid-2000s. For example, patent reexamination is an administrative proceeding whereby the PTO will re-examine a granted patent's validity in light of any newly arising question, grounded on evidence of patentability. (*see* 35 U.S.C. §§ 302 *et seq*.) In 1997, in *In re Portola Packaging Inc*, 110 F.3d 786 (Fed. Cir. 1997) the Federal Circuit interpreted the reexamination statute to provide that a prior art reference cited during ordinary prosecution of a patent application could not be used to attack the issued patent in a subsequent reexamination. *Id.* at 791.

Because *Portola* effectively insulated a patent from attack, the patent bar reacted by filing numerous, as many as hundreds, of prior art references during initial patent application. This severely impacted the patent system and the PTO and resulted in a series of Congressional hearings. The U.S. House Judiciary Committee heard testimony about this practice, considered legislative amendments, and reported the following:

> This court-imposed standard has frustrated members of the public. It has also lead to abuse by patent agents and lawyers who are gaming the system in place. Earlier this Spring . . . the Subcommittee heard testimony that some applications may include *hundreds of prior art references*, knowing that the PTO examiner has only a few precious hours to review the application before she is required to make a decision on its grant. Therefore, a weak patent application may be prepared in a fashion so that the resulting patent would likely be insulated from subsequent review through reexamination

> even if there was a "smoking gun" bearing on its validity. This frustrates the goals of Congress behind the [Patent] statutes . . .

House Rep. 107-120, Substantial New Question of Patentability in Reexamination Proceeding, 1st Sess., 107th Cong., June. 28, 2001 (emphasis added). The problem of applicants overwhelming the PTO with evidence submissions was addressed by a Congressional amendment to 35 U.S.C. § 303 in 2002. It hence discouraged applicants from overwhelming the PTO with prior art references to insulate oneself from the threat of a reexamination.

The consequence of adopting a closed-record, deferential standard for § 145 civil action will incentivize inventors to file a large amount of evidence—*sometimes hundreds of prior art references*—in anticipation of a new ground of rejection popping up in the Board's decision. Inventors will inevitably file more evidence, including costly affidavits. This will increase the size and expense of applications. The burdens on the PTO will mount, as it will result in patent examiners having more evidence to review in the precious time allotted for each application. As other *amici* have noted, "this will place extreme strain on the PTO and cause unnecessary delay." *Br. of Amicus Curiae Fédération Internationale Des Conseils En Propriété Industrielle in Support of Neither Party on Rehearing en Banc*, 2010 WL 2625004 at *10 (C.A.Fed.)(Apr. 7, 2010).

The obvious connection between PTO operations and patent quality are well-known. In 2002, the then-Under Secretary and PTO Director testified regarding the impending PTO operational and workload crisis

before a House of Representatives Judiciary Subcommittee:

> The increasing volume and complexity of our workload poses serious issues for the USPTO. Some might even use the word "crisis." . . . I believe that the challenges the USPTO faces today while similar to the situations in the mid-1960s and early 1980s, are on a much larger scale . . . .

U.S. Patent and Trademark Office: Operations and Fiscal Year Year 2003 Budget: Before the H. Judiciary Subcomm. On Courts, the Internet, and Intellectual Property, 107th Cong. 7 (2002) (prepared statement of the Under Secretary of Commerce and Director of the USPTO).

The "front-end" of the § 145 civil action review issue may appear modest. The PTO explains that on average fewer than 10 such cases are filed per year *See Br. for the Director of the United States Patent and Trademark Office on Rehearing en Banc* 2010 WL 2625006 *40 n.11 (Fed. Cir.) (May 3, 2010). However, the "back-end" of the problem is that annually more than 400,000 new patent applications are filed with the PTO. *See* USPTO ANNUAL PERFORMANCE AND ACCOUNTABILITY REPORT: FISCAL YEAR 2010 at 126 available online at http://www.uspto.gov/about/stratplan/ar/2010/USPTOFY2010PAR.pdf (hereinafter APAR-2010). A judicial change to long-standing and relied upon procedures would likely have a modest impact on judicial economy since the current system results in a tiny number of §145 actions. However, because of the disparity in numbers of applications to number of § 145 actions, even a small

change in inventor prophylactic behavior will have a much larger effect on PTO workload, stifle PTO operations, and erode patent quality.

In response to those who wish to disturb the long-standing conclusion of this Court and the Federal Circuit's interpretation of § 145 to preclude a plaintiff from introducing new evidence or prevent a *de novo* hearing upon judicial review, they must carefully consider the likely consequences arising from the whole of the Patent Act. If any change is needed to § 145, it is best addressed by Congress, in light of the impact on the patent system as a whole. Of course, the nature of the district court proceeding and review of newly introduced evidence can easily be moderated by the Federal Circuit and this Court, *Zurko* at 164 ("nothing in this opinion prevents the Federal Circuit from adjusting the standard of review where necessary"), and subject to the Federal Rules of Evidence and Federal Rules of Civil Procedure. *Hyatt*, 625 F.3d at 1338.

Opponents should see no flaw in leaving such matters in the hands of the judiciary. This Court has observed, "[i]t cannot be too often repeated that judges are not automata. The ultimate reliance for the fair operation of any standard is a judiciary of high competence and character and the constant play of an informed professional critique upon its work." *Universal Camera Corp. v. Labor Bd.*, 340 U.S. 474, 489 (1951). It is certain the district court judges can properly review actions of the PTO and manage a plaintiff's evidentiary considerations based on the long-standing and proper interpretation of §145.

CONCLUSION

For the foregoing reasons, the IEEE-USA therefore respectfully asks this Court to preserve a 175-year-old *status quo*: in a § 145 civil action, an inventor should be permitted to introduce new evidence, and obtain *de novo* review of an adverse PTO Board decision.

Respectfully submitted,

Chris J. Katopis
Counsel of Record
1308 Clifton Street, N.W.
Washington, D.C. 20009
Tel. (202) 200-9490
chriskatopis@gmail.com

Counsel for Amicus Curiae
IEEE-USA

AMICUS CURIAE BRIEF

RE
AND
BRIEFS

No. 10-1219

In the Supreme Court of the United States

DAVID J. KAPPOS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR, PATENT AND TRADEMARK OFFICE,

Petitioner,

v.

GILBERT P. HYATT,

Respondent.

On Writ of Certiorari to the United States Court of Appeals for the Federal Circuit

BRIEF OF *AMICI CURIAE* INTEL CORP., YAHOO! INC., MICROSOFT CORP., AND NVIDIA CORP. IN SUPPORT OF PETITIONER

LAUREN A. DEGNAN
Fish & Richardson P.C.
1425 K Street, N.W.
Suite 1100
Washington, D.C. 20005
(202) 783-5070

JOHN A. DRAGSETH
Counsel of Record
Fish & Richardson P.C.
60 So. 6th Street · Suite 3200
Minneapolis, MN 55402
(612) 335-5070
dragseth@fr.com

Counsel for Amici Curiae

[Additional counsel listed on inside cover]

2011 – Bachman Legal Printing ■ (612) 339-9518 ■ 1-800-715-3582 ■ Fax (612) 337-8053

Library of Congress
Law Library

TINA M. CHAPPELL
Intel Corporation
M/S: OC2-157
4500 South Dobson Road
Chandler, AZ 85248

DAVID M. SIMON
Intel Corporation
M/S: RNB 4 150
2200 Mission College Blvd.
Santa Clara, CA 95054

KEVIN T. KRAMER
Yahoo! Inc.
701 First Avenue
Sunnyvale, CA 94089
(408) 349-3300

HORACIO E. GUTIÉRREZ
Microsoft Corporation
Intellectual Property Group
One Microsoft Way
Redmond, WA 98052
(425) 882-8080

DAVID M. SHANNON
NVIDIA
2701 San Tomas Expressway
Santa Clara, CA 95050
(408) 486-2000

Counsel for Amici

TABLE OF CONTENTS

Page

TABLE OF AUTHORITIES iv

INTEREST OF THE AMICI CURIAE 1

SUMMARY OF THE ARGUMENT 2

ARGUMENT 3

I. District Courts Can Preclude New Evidence That Reasonably Should Have Been Introduced at the PTO, Whether Under Administrative Law Standards or Standards Governing Normal Civil Actions 3

II. The Prevailing Judicial Practice Before and After 1952 Supports Excluding Unreasonably Late Evidence 9

III. Fast-Paced Innovation Requires Prompt Patentability Decisions, Not a Standard That Sanctions Gamesmanship and Delay 14

CONCLUSION 21

TABLE OF AUTHORITIES

Page(s)

CASES

Allen v. McCurry,
449 U.S. 90 (1980) 6

American Steel Foundries v. Robertson,
262 U.S. 209 (1923) 5

Ariad Pharma., Inc. v. Eli Lilly & Co.,
598 F.3d 1336 (Fed. Cir. 2010) (*en banc*)..... 15

Atchison, Topeka & Santa Fe Ry. v. Hercules.,
146 F.3d 1071, 1074 (9th Cir. 1998) 10

Barrett Co. v. Koppers Co.,
22 F.2d 395 (3d Cir. 1927)..... 9, 10

Boucher Inventions, Ltd. v. Sola Elec. Co.,
131 F.2d 225, 227 (D.C. Cir. 1942) 11, 12

Butler v. Shaw,
21 F. 321, 327 (C.C.D. Mass. 1884) 12

Butterworth v. United States,
112 U.S. 50 (1884) 5, 12

Chandler v. Roudebush,
425 U.S. 840 (1976) 13

Consolo v. Federal Mar. Comm'n,
383 U.S. 607 (1966) 5

Fregeau v. Mossinghoff,
776 F.2d 1034 (Fed. Cir. 1985)..... 4

Forest Grove School Dist. v. T.A.,
129 S. Ct. 2484 (2009) 13

Gandy v. Marble,
122 U.S. 432 (1887) 6

Garcia v. United States,
469 U.S. 70 (1984) 5

TABLE OF AUTHORITIES - continued

Page(s)

Globe-Union, Inc. v. Chicago Tel. Supply Co.,
103 F.2d 722 (7th Cir. 1939) 11

Graham v. John Deere Co.,
383 U.S. 1 (1966) 15

Greene v. Beidler,
58 F.2d 207 (2d Cir. 1932)..... 11

Hyatt v. Boone,
146 F.3d 1348 (Fed. Cir. 1998)..... 17

Hyatt v. Dudas
492 F3.d 1365 (Fed. Cir. 2007)..... 18

Hyatt v. Kappos,
576 F.3d 1248 n.2 (Fed. Cir. 2009) 18

Hyatt v. Kappos,
625 F.3d 1320 (Fed. Cir. 2010) (*en banc*)..... 4, 9

In re Squire,
22 F. Cas. 1015 (C.C.E.D. Mo. 1877) 12

Kelly v. Robinson,
479 U.S. 36 (1986) 5

Kirschke v. Lamar,
426 F.2d 870 (8th Cir. 1970) 9, 11

Kirschke v. Lamar,
300 F. Supp. 146 (W.D. Mo. 1969) 11

Knutson v. Gallsworthy,
164 F.2d 497 (D.C. Cir. 1947) 12

Lidell v. Smith,
345 F.2d 491 (7th Cir. 1965) 6

McCaughn v. Hershey Chocolate Co.,
283 U.S. 488 (1931) 5

TABLE OF AUTHORITIES - continued

Page(s)

McKart v. United States,
395 U.S. 185 (1969) 5

Microsoft Corp. v. i4i,
131 S. Ct. 2238 (2011) 3, 15

Minnesota Mining & Mfg. v. Carborundum Co.,
155 F.2d 746 (3d Cir. 1946) 11

Montana v. United States,
440 U.S. 147 (1979) 6, 7

Morgan v. Daniels,
153 U.S. 120 (1894) 3, 4

Robertson v. Cooper,
46 F.2d 766 (4th Cir. 1931) 18

Sandvik Aktiebolag v. Samuels,
1991 WL 25774 (D.D.C. Feb. 7, 1991) 18

Schilling v. Scwitzer-Cummins Co.,
142 F.2d 82 (D.C. Cir. 1944) 10

Watson v. Allen,
274 F.2d 87 (D.C. Cir. 1959) 18

Whipple v. Miner,
15 F. 117 (C.C.D. Mass. 1883) 12

STATUTES

5 U.S.C. § 552 13
5 U.S.C. § 552a 13
5 U.S.C. § 554 13
7 U.S.C. § 2032 13
28 U.S.C. § 636 13
35 U.S.C. § 145 ..... passim

TABLE OF AUTHORITIES - continued

Page(s)

35 U.S.C. § 154 16
37 C.F.R. § 1.113 19
37 C.F.R. § 41.39(a)(2) 20
37 C.F.R. 1.701(a) 16
37 C.F.R. 1.702(e) 16
R.S. 4915 ..... passim

OTHER

Manual of Patent Examining Procedure 706.07 19

Manual of Patent Examining Procedure 1207.03 20

Petitioner's Brief (Pet. Br.) 5, 7

U.S. Patent & Trademark Office: Performance and Accountability Report, Fiscal Year 2010 (available at http://www.uspto.gov/about/stratplan/ar/2010/USPTOFY2010PAR.pdf) 7, 14

U.S. Patent & Trademark Office, ex Parte Appeals Dashboard, June 2011 (http://www.uspto.gov/ip/boards/bpai/dashboards/exappls/2011_ex_parte_appeals_jun_2011.pdf (last accessed Sept. 5, 2011)) 7, 15

INTEREST OF THE AMICI CURIAE[1]

The Amici are technology companies that fund extensive research and development, that each own many hundreds or thousands of patents, and that appear as both plaintiffs and defendants in patent suits. Such companies depend on timely action on patentability decisions (whether issuance or denial) so as to make business decisions and set their expectations. Cases such as this—where the applicant filed his application over sixteen years ago and started this Section 145 action over seven years ago, while claiming priority back several decades—are the opposite of a timely final decision. This case and others like it impede the ability of members of the public to order their affairs, and thereby harm innovation in the United States economy. For these reasons, the Amici have a central interest in this case.

---

[1] Counsel for the parties have consented in writing to the filing of this brief—Mr. Hyatt's letter of consent has been filed with the Clerk, and counsel for Mr. Kappos has provided a separate written consent. Pursuant to Rule 37.6, no counsel for either party had any role in authoring this brief in whole or in part, and no party other than the named *Amici* has made any monetary contribution toward the preparation and submission of this brief.

SUMMARY OF THE ARGUMENT

Gilbert Hyatt filed his initial patent application in 1975. It should have issued in due course, run its term, and expired over a decade ago. But he waited 20 years to introduce the current set of claims, ignored multiple requests by the examiner for the relevant information, and ultimately delayed for 9 years in presenting the evidence that he now alleges is the difference-maker for patentability. The Federal Circuit's decision permits and indeed encourages such needless delay, providing opportunities for gaming the system, even though Section 145 does not otherwise support such a result, and case law and good policy reject it.

On the statute, this Court has indicated that actions under Section 145 are to be evaluated and judged according to traditional administrative law principles. In any event, courts can preclude evidence like that offered by Hyatt, whether using such principles or the Federal Circuit's approach of looking to traditional civil actions. Specifically, traditional civil actions provide common law tools for managing cases—in addition to the Rules of Civil Procedure and Rules of Evidence recognized by the Federal Circuit. Either way, district courts can exclude unreasonably late evidence.

On the case law, although this Court has not addressed the issue, the decisions before and after Section 145's enactment in 1952 held—consistent with typical district court practice on preclusion—that a party cannot introduce, in the district court, evidence that it reasonably could have provided to the PTO. Congress implicitly adopted the prevailing case law when it enacted Section 145.

And on good policy, the Government's proposed standard is plainly sensible and proper. It is fair to applicants; it prevents gaming the system; it leads to better patent quality and faster issuance of patents, and conserves scarce PTO and judicial resources. The Federal Circuit's standard, on the other hand, encourages delay and gamesmanship; offers no motivation to improve patent quality, and likewise imposes no deterrent to act in good faith and to use candor while working with the PTO. For these reasons, the Amici write in support of the Government's proposed standard.

ARGUMENT

I. District Courts Can Preclude New Evidence That Reasonably Should Have Been Introduced at the PTO, Whether Under Administrative Law Standards or Standards Governing Normal Civil Actions

A. "Congress has charged the United States Patent and Trademark Office (PTO) with the task of examining patent applications, and issuing patents if 'it appears that the applicant is entitled to a patent under the law.'" *Microsoft Corp. v. i4i*, 131 S. Ct. 2238, 2242 (2011) (citations omitted). This foundational charge led the Court in *Morgan v. Daniels* to frame the issue of review under R.S. 4915—Section 145's predecessor—by noting that the action is one to "set aside the action of one of the executive departments of the government," 153 U.S. 120, 124 (1894). As this Court explained, because "the one charged with the administration of the patent system had finished its investigations and made its determination," its decision "control[s] upon that question of fact" unless the contrary is proven

by a "thorough conviction," *id.* at 125—consistent with an understanding that general rules for reviewing agency action apply.[2] The early Federal Circuit similarly acknowledged that "[i]n view of the history of the sections, it cannot seriously be contended that a § 145 action is other than one to overturn the board's decision." *Fregeau v. Mossinghoff*, 776 F.2d 1034, 1037 (Fed. Cir. 1985).

Just as R.S. 4915 gives dissatisfied patent applicants a right to review of PTO determinations by a "bill in equity," Section 145 provides for a "civil action" that has been interpreted as being a bill in equity. Both provide that a court "may adjudge that such applicant is entitled . . . to receive a patent." They are also similar in what they *do not* provide: a standard for introducing evidence, or the evidentiary standard for the action. Although both direct courts to act "as the facts in the case may appear," neither says at which point those facts must enter the record nor when it is proper for a court to preclude admission of particular evidence.

Despite much attention given to it, the legislative history is unhelpful. The Federal Circuit relied on hearing testimony of individuals—not on committee reports, not on marked-up bills, not even on statements from actual members of Congress. *See Hyatt v. Kappos*, 625 F.3d 1320, 1328-30 (Fed. Cir. 2010) (*en banc*). Unsurprisingly, this Court has found such statements to be unhelpful in discerning the intent of the broader Congress. *E.g., Kelly v. Robinson*, 479 U.S. 36 (1986) (declining "to accord

---

[2] While *Morgan* was an "interference" case, and such cases are now handled under Section 146, both Sections 145 and 146 trace back to R.S. 4915, so the prior case law applies to both.

any significance to ... statements" made in hearings); *Garcia v. United States*, 469 U.S. 70, 76 (1984) (similar); *McCaughn v. Hershey Chocolate Co.*, 283 U.S. 488 (1931).

When a statute provides for agency review but does not define its scope, standard principles govern and provide due respect for the expertise of the agency. *E.g., Consolo v. Federal Mar. Comm'n*, 383 U.S. 607, 619 n.17 (1966). Such principles reflect the need for a party to exhaust its arguments at the agency. *See McKart v. United States*, 395 U.S. 185, 193 (1969). Had Congress meant to exclude Section 145 review from the administrative procedures it had enacted just six years earlier, one would expect it to have been clear about it. Thus, as the government explains, Section 145's enactment left the standard principles of agency review intact. *See* Pet. Br. at 21-24.

Moreover, this Court has recognized that the civil review of PTO actions is not truly afresh, but is subject to the regulations that govern PTO practice—i.e., applicants cannot avoid PTO regulations merely by shifting venue. For example, in *American Steel Foundries v. Robertson*, the Court interpreted Section 145's analogue in trademark cases and commented that such actions are, "in fact and necessarily, a part of the application for the patent," 262 U.S. 209, 213 (1923) (*quoting Butterworth v. United States*, 112 U.S. 50 (1884) ("[T]he decision of the court on a bill in equity becomes equally [with the direct appeal from the Patent Office] the decision of the Patent Office, and ... is therefore clearly a branch of the application for the patent, and to be governed by the rule of laches and delay declared by section 4894 to be attendant upon the application.")));

see also Gandy v. Marble, 122 U.S. 432 (1887). Similarly, Hyatt cannot avoid PTO rules for introducing evidence to support his case simply by transferring venue to district court.

B. However, even if one accepts the Federal Circuit's approach of looking to evidentiary limits in general civil actions, it does not follow that unreasonably late evidence is admissible. In looking to only rule-based limits in civil actions—the Federal Rules of Civil Procedure (FRCP) and the Federal Rules of Evidence (FRE)—the Federal Circuit overlooked common law maxims that support excluding evidence in Section 145 actions where such evidence reasonably should have been provided to the PTO. Specifically, the common law preclusion rules of res judicata, issue preclusion, and law of the case are based, not on the FRCP or FRE, but on common law notions that courts may manage their dockets to reduce unnecessary judicial work and ensure fairness to the parties. *See Lidell v. Smith*, 345 F.2d 491, 493 (7th Cir. 1965) (res judicata principles come from maxims of common law); *see also Allen v. McCurry*, 449 U.S. 90, 94 (1980) (res judicata serves to conserve judicial resources, encourage reliance on adjudication, and relieve parties from fighting multiple lawsuits); *Montana v. United States*, 440 U.S. 147, 153-54 (1979) ("To preclude parties from contesting matters that they have had a full and fair opportunity to litigate protects their adversaries from the expense and vexation attending multiple lawsuits, conserves judicial resources, and fosters reliance on judicial action by minimizing the possibility of inconsistent decisions.").

These common law maxims closely mirror the Government's proposed standard for the late introduction of evidence in this case. For example, res judicata applies to issues that a litigant could have raised in a prior action, while the Government's standard blocks new evidence if the applicant had a reasonable opportunity to provide the evidence in the PTO. *Compare Montana*, 440 U.S. at 153 (parties precluded on issues for which they had a "full and fair opportunity to litigate") *with* Pet. Br. at 42-46. The effect is different—preclusion of an entire issue from a final judgment based on a full opportunity to be heard, versus preclusion of evidence because of a reasonable opportunity to introduce the evidence—but the common law rationale is the same.

Such similarity is expected because the same practical concerns that limit new issues in regular civil actions also animate Section 145 preclusion of unreasonably late new evidence. For example, excluding late evidence that a party had a "full and fair opportunity" to present earlier conserves valuable judicial resources in all civil actions, including Section 145 actions. Courts are an enormously expensive, and limited, governmental resource that should not be required to first decide issues that could have been decided more economically, and often more competently, before. District courts need appropriate tools to control their dockets when parties have had reasonable opportunities to raise issues and evidence, and preclusion is a necessary and appropriate tool.

Additionally, the desire for the Government to have repose as a litigant is no different than for a private litigant. As recently recognized by the administration, PTO resources are a scarce

commodity, with a backlog over one million pending patent applications and over 20,000 pending Patent Board actions. *See* U.S. Patent & Trademark Office: Performance and Accountability Report, Fiscal Year 2010, at 128 (available at http://www.uspto.gov/about/stratplan/ar/2010/USPTOFY2010PAR.pdf); U.S. Patent & Trademark Office, ex Parte Appeals Dashboard, June 2011 (http://www.uspto.gov/ip/boards/bpai/dashboards/exappls/2011_ex_parte_appeals_jun_2011.pdf (last accessed Sept. 5, 2011)). The time of PTO examiners should not be wasted, nor should the time of Government lawyers who are required to defend Section 145 actions.

The public—though not allowed to participate in *ex parte* patent prosecution—also deserves finality, so that it can determine whether it needs to avoid a certain technology or is free to practice it, and so that PTO resources are not diverted from deserving applicants to delaying applicants. Indeed, the public interest here is more acute than it is in general civil litigation because PTO proceedings decide property rights that can be used directly against members of the public. The present case is a perfect example, where the public has been waiting decades for Hyatt's patent to issue and start running its term—but the case has been delayed time and again while diligent applicants have been pushed aside.

That Congress has provided two judicial routes for patent applicants does not bless an approach that lets applicants withhold evidence, any more than a right to file multiple civil actions "*de novo*" in normal civil litigation frees a party from arguments and evidence it presented or should have presented in prior suits. The belated introduction of new evidence

in Section 145 actions should be like that in civil litigations that have a prior history (and are thus subject to preclusion), and not to civil actions that are fresh and new, as the Federal Circuit presumed.

II. The Prevailing Judicial Practice Before and After 1952 Supports Excluding Unreasonably Late Evidence

A. Although this Court has not previously addressed a district court's ability to limit unreasonably late evidence in Section 145 actions, numerous appellate courts ruled, before and after 1952, that plaintiffs "are estopped to offer evidence which was wholly within their possession and control at the [PTO] proceeding and which they withheld from that proceeding." *Barrett Co. v. Koppers Co.*, 22 F.2d 395, 397 (3d Cir. 1927); *see Kirschke v. Lamar*, 426 F.2d 870, 872-75 (8th Cir. 1970).[3] Each party "is expected to produce all the testimony he has on [an] issue" and "[i]f for some reason of his own [he] withhold[s] evidence which is available [and that] he can produce at will but does not [], then he must be regarded as having abandoned that evidence in its bearing on the issue under trial." *Barrett*, 22 F.2d at 397. As the Third Circuit cogently explained:

> The law gave the plaintiffs a day in court on the issue of priority. That was the day the interference was heard and if they chose not to avail themselves of their full rights but to gamble on the decision by giving only a part, and the weaker part, of the evidence they

[3] There is no dispute that Sections 145 and 146 were a codification of prior R.S. 4915, and that any prevailing pre-1952 case law interpretation would apply to those sections. *See, e.g., Hyatt*, 625 F.3d at 1330.

> had in hand, they did it at their own risk. After losing on such evidence ..., they cannot come into a District Court and say, now for the first time we shall tell the true story ...

Id.

Indeed, by deliberately choosing to tell only half the story and then later insisting that justice demands he be heard in full, a plaintiff "comes very close to trifling with the court's processes." *Id.* This familiar preclusion principle is applied in civil actions to prevent "what otherwise would be a train of futile appeals" if parties were allowed to withhold evidence in one proceeding only to propound it in a later proceeding. *Id.* (hearing late submitted evidence by a plaintiff that "purposefully keep [the PTO] in the dark" is tantamount to 'assisting the plaintiff[] to profit by [his] own technical wrongdoing").[4]

Despite some "variegated terminology," courts that have faced this issue have followed *Barrett*'s common sense reasoning and standard almost universally. *See, e.g., Kirschke*, 426 F.2d at 872-75 ("[A] deliberate, intentional, or willful withholding . . . of evidence from [the PTO], whether attended by reprehensible motives or not, whether it be for tactical or other reasons, justifies exclusion of such

---

[4] Such case-to-case preclusion rules are also consistent with a court's ability to exclude evidence within a particular action, such as when the evidence is produced after discovery deadlines to the prejudice of an opponent. *E.g., Atchison, Topeka and Santa Fe Ry. Co. v. Hercules Inc.*, 146 F.3d 1071, 1074 (9th Cir. 1998) (noting that district courts have inherent power to control their dockets even where a particular Rule of Civil Procedure did not apply).

evidence."); *Schilling v. Scwitzer-Cummins Co.*, 142 F.2d 82, 85 (D.C. Cir. 1944) (affirming a district court that excluded evidence that was "wholly within [the applicant's] possession and control" and was withheld); *Boucher Inventions, Ltd. v. Sola Elec. Co.*, 131 F.2d 225, 227 (D.C. Cir. 1942), *cert. denied*, 318 U.S. 770 (1943) (practice under R.S. 4915 "contemplates a full disclosure to that office, so far as is reasonably possible."); *Globe-Union, Inc. v. Chicago Tel. Supply Co.*, 103 F.2d 722 (7th Cir. 1939) ("[A]ll pertinent evidence, actually available, should be submitted in the first instance."); *Greene v. Beidler*, 58 F.2d 207, 209-10 (2d Cir. 1932) (similar).[5]

The common thread throughout these cases is the premise that "full disclosure, so far as is reasonably possibly" is necessary for the proper operation of administrative processes. *Kirschke*, 426 F.2d at 872 (*quoting Kirschke v. Lamar*, 300 F. Supp. 146 (W.D. Mo. 1969)). Although Section 145 generally permits introduction of new evidence, it "must not [ ] be read in a vacuum," or it threatens the viability of the PTO procedures. *Id.* at 874. It "does not mean that a party can have free rein to look the other way at the [PTO] proceeding and then throw all its evidentiary eggs into the judicial

---

[5] The Government has identified a Third Circuit case—*Minnesota Mining & Manufacturing v. Carborundum Co.*, 155 F.2d 746 (3d Cir. 1946)—that refused to exclude evidence that was available to the applicant at the Patent Office. Pet. Br. at 35 n.8. But in *Minnesota Mining*, the evidence was testimonial and the statute had specifically referred to the ability of applicants to take "further testimony" in the district court—an issue that is not present here. *See id.* at 748. In any event, *Minnesota Mining* is perhaps most conspicuous by its singularity.

basket." *Id.* Precluding such unreasonably late evidence is fair, moreover, as it does not "exclude the presentation of evidence, which previously had not been procurable or which had become known after the interference proceeding," *Globe-Union*, 103 F.2d at 728. In short, these many courts recognized the logic in a rule that allows district courts to manage Section 145 actions to be fair to the applicant, the PTO, and the public, and to encourage efficient prosecution of patent applications and management of the court's own docket.

B. The Federal Circuit's standard is contrary to these prevailing regional circuit cases because it would admit evidence with no limits relating to whether the evidence should have been produced in the PTO. Numerous cases blocked new evidence that such an unbounded standard would allow. *See, e.g., Boucher Inventions*, 131 F.2d at 227 (blocking evidence suppressed or withheld by the applicant); *Knutson v. Gallsworthy*, 164 F.2d 497, 508-509 (D.C. Cir. 1947) (recognizing that new evidence can be introduced in an R.S. 4915 action, but noting that a party is nonetheless blocked from introducing evidence it withheld form the PTO). The Federal Circuit provided no cogent rationale for adopting a rule that differed from the one these other courts applied.

The cases the Federal Circuit cited (625 F.3d at 1333) as allowing introduction of new evidence do not make that introduction limitless—and indeed do not even address the point. *See Butterworth*, 112 U.S. at 56 (simply noting that the R.S. 4915 action was one in equity under ordinary equity procedures, but not addressing the limitations available to a district court to exclude unreasonably late evidence); *In re*

Squire, 22 F. Cas. 1015, 1016 (C.C.E.D. Mo. 1877) (similar); *Butler v. Shaw*, 21 F. 321, 327 (C.C.D. Mass. 1884) (similar); *Whipple v. Miner*, 15 F. 117, 118 (C.C.D. Mass. 1883) (similar). Likewise, casual references to "*de novo*" review in cases under Section 145 merely indicate that the district court is to view the evidence afresh, but those decisions, like this Court's decisions, say nothing about what evidence is to be permitted.[6] And the Federal Circuit's reliance on *Chandler v. Roudebush*, for the proposition that "civil action" language in the statute brings with it FRCP/FRE review misses the mark because the Title VII action there was an action that was intended to parallel private employment suits that had wide-open introduction of evidence, 425 U.S. 840, 863 (1976).

C. Congress is presumed to understand and adopt prevailing administrative or judicial interpretation of a statute when it re-enacts a statute without substantive changes. *See Forest Grove School Dist. v. T.A.*, 129 S. Ct. 2484, 2492 (2009). And it did so in codifying R.S. 4915 into Sections 145 and 146, when the case law was in harmony around the Government's proposed standard, other cases found preclusion on more egregious facts but did not set separate standards, and tellingly, no circuit called for the Federal Circuit's standard permitting patent applicants to introduce evidence they could have and should have allowed the PTO to consider first. Accordingly,

---

[6] Section 145 does not expressly provide for *de novo* trials. When Congress intends a truly *de novo* trial or review, it generally provides for one by using those express terms. *See, e.g.*, 5 U.S.C. §§ 552, 552a, 554; 7 U.S.C. § 2032; 28 U.S.C. § 636.

Congress must have approved of allowing district court's the discretion to exclude unreasonably late evidence in section 145 actions, as the Government's proposed standard does.

III. Fast-Paced Innovation Requires Prompt Patentability Decisions, Not a Standard That Sanctions Gamesmanship and Delay

Prompt, sound decisions about patentability are crucial in this era of fast-paced innovation. The decisions that companies make today about the technologies and platforms on which they will base their future products drive investment, create jobs, and keep America competitive in an increasingly global market. Such decisions are complicated by the fact that the PTO lacks the resources to keep pace with today's innovation, resulting in a lag of years for patentability decisions.

A standard that encourages applicants to present evidence when it is reasonably available not only promotes and rewards innovation but also facilitates decisions by an over-burdened PTO and produces higher quality patents. A standard that sanctions delay in producing evidence is wasteful and inconsistent with technological advancement.

A. First, the early disclosure of evidence avoids wasting PTO resources. Allowing an applicant to hold back known evidence makes the decision of the PTO potentially wrong and, therefore, wasteful. Such actions would take resources away from the PTO's examination of other pending patent applications and frustrate the PTO's efforts to reduce its backlog of one million pending patent applications and over 20,000 appeals at the Patent Board. *See*

U.S. Patent & Trademark Office: Performance and Accountability Report, Fiscal Year 2010, at 128 (available at http://www.uspto.gov/about/stratplan/ar/2010/USPTOFY2010PAR.pdf); U.S. Patent & Trademark Office, ex Parte Appeals Dashboard, June 2011 (http://www.uspto.gov/ip/boards/bpai/dashboards/exappls/2011_ex_parte_appeals_jun_2011.pdf (last accessed Sept. 5, 2011)).

B. Second, requiring the introduction of readily-available evidence at the PTO prevents forum shopping because it ensures that the district court will have the benefit of the PTO's viewpoint in evaluating complex technical facts and evidence.

In *Microsoft Corp. v. i4i Limited Partnership*, this Court recently reaffirmed the proposition that issued patents are presumed valid, and can be overturned only with clear and convincing evidence. 131 S. Ct 2238, 2245 (2011). In this context, the Court cited the expertise the PTO brings to the task of patent examination. *Id.* at 2249-51. For example, most of the determinations made during the examination process are assessed from the viewpoint of an artisan skilled in the relevant art (*e.g.*, a chemist, a physicist, or a Ph.D. in biotechnology). The issues include claim construction, whether the claimed inventions would have been obvious, and whether the original specification actually describes the invention that was later claimed—the issue in this case. *See, e.g., Graham v. John Deere Co.*, 383 U.S. 1 (1966) (obviousness judged from perspective of person having ordinary level of skill in the particular technology); *Ariad Pharma., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (*en banc*) (written description requirement is measure from the perspective of a skilled artisan). A district court

certainly benefits, in a Section 145 action, from having an examiner's skilled views in the first instance and a careful second view by three technically-trained administrative law judges on such issues.

The Federal Circuit's standard, in contrast, leaves the decision about whether to obtain the PTO's input solely in the hands of the applicant, allowing the applicant to forum shop for the evidence's audience. The applicant thus can determine whether the better audience for this evidence is the particular examiner who has already rejected the patent claims or a district court judge. Even though some district court judges do possess technical expertise, an applicant could weigh the likelihood that the district court judge assigned to its Section 145 action would view the evidence as critically as would the application's current examiner. Putting the decision as to who should review critical technical evidence in the hands of the party most interested in getting a patent based on such evidence does not serve the public good.

C. Third, a quick resolution of patentability is important for the public, in addition to the patentee and the PTO (with its ever-present backlog of applications).

Prompt disclosure may cause the examiner to allow the claims, so that the patentee can assert the patent if it truly has value, and the public can change course before it has already committed to the technology. If the applicant is allowed to hold evidence, however, the informed decision on patentability—from which the public can measure its actions—cannot occur until years later. This sort of delay unfairly prejudices the public by letting

applicants extend their patent term[7] while the public moves forward with technologies (and perhaps getting locked into them), not knowing whether the technologies will fall under a future patent. Such delay also makes it much more difficult for the examiner and an alleged infringer (in later litigation) to find prior art that is decades old.

Hyatt's own prosecution is a perfect example of the problems with the Federal Circuit's approach. Hyatt claims to have filed a patent application on the claims at-issue here in 1975. Yet he did not present his ultimate evidence until 2004. Intervening proceedings have delayed the patent even more years. And whatever patent he gets will not expire until seventeen years after it issues.[8] Therefore, Hyatt could potentially pursue companies that adopted technologies in the 1970s all the way until 2030—a true impediment to innovation.[9]

---

[7] Current-day patents are eligible for a Patent Term Adjustment rules that add term to an issuing patent, for the period of the appeal from the notice of appeal at the Board to a favorable decision in a Section 145 action. *See* 35 U.S.C. § 154 (b)(1)(C); 37 C.F.R. 1.701(a); 37 C.F.R. 1.702(e).

[8] Because Hyatt filed his application before June 8, 1995, the term of the patent that issues from that application will be seventeen years from the issue date. See 35 U.S.C. § 154(c); Golan v. Pingel Enters., 310 F.3d 1360, 1364-65 n.1 (Fed. Cir. 2002).

[9] Hyatt has used similar dilatory tactics in filing lawsuits on other of his patents. For example, he asserted an eventually-invalidated submarine patent against a variety of microprocessors in *Hyatt v. Boone*, 146 F.3d 1348 (Fed. Cir. 1998). That patent issued in 1990 and claimed priority to an application filed in 1970. *Id.* at 1352. Between 1970 and 1990, microprocessor sales had grown from zero to billions of dollars.

The statute's requirement that the patent applicant pay the expenses of the action does not meaningfully reduce the incentive for strategic delay and gamesmanship. First, the taxable expenses in a Section 145 action are trivial, relating to court transcripts, and reasonable printing, travel, and expert costs. *See Watson v. Allen*, 274 F.2d 87, 88-89 (D.C. Cir. 1959) (awarding reasonable printing expenses); *Robertson v. Cooper*, 46 F.2d 766, 769 (4th Cir. 1931) (awarding the government's expenses for travelling to a deposition); *Sandvik Aktiebolag v. Samuels*, 1991 WL 25774, *1-2 (D.D.C. Feb. 7, 1991) (awarding court transcript and reasonable expert fees). Given Hyatt's frequent resort to section 145 actions, he apparently does not find the cost or the delay a deterrent from what he perceives are the rewards gained by those "strategic delays."[10]

D. Requiring the presentation of reasonably available evidence imposes no hardship on a patent applicant. The PTO provides ample opportunity to present evidence. For example, in each round with the PTO, an applicant gets at least two chances to make arguments, adjust claims, and introduce evidence. *See* 37 C.F.R. § 1.113; Manual of Patent Examining Procedure ("MPEP") 706.07. If the applicant overcomes a rejection and the examiner issues a new rejection on a different ground, the

---

[10] As the original panel noted, Hyatt is "familiar with this Court," *Hyatt v. Kappos*, 576 F.3d 1248 n.2 (Fed. Cir. 2009) (listing sixteen appeals to the Federal Circuit, many of which concern section 145, including *Hyatt v. Dudas* 492 F3.d 1365, 1367 (Fed. Cir. 2007) (section 145 action involving "continuation applications with lineages that can be traced back decades," and 1100 claims that Hyatt filed "rather than respond to the merits of the [examiner's] rejection")).

examiner must give the applicant a chance to respond to the new rejection, and cannot issue a "final" rejection—and applicants can even make "after-final" arguments to point out errors in a "final" rejection. Similarly, if an examiner takes any new positions on appeal, the examiner must allow the applicant to re-open prosecution so that the applicant has a fair chance to respond and introduce evidence. *See* 37 C.F.R. § 41.39(a)(2); MPEP 1207.03. Finally, applicants can continue the back-and-forth essentially indefinitely—even when the examiner is right and they are wrong—through the simple and common filing of a Request for Continued Examination or a continuation application. *See* 37 C.F.R. § 1.114; MPEP 706.07(h). In short, there are no "gotchas" for applicants in the PTO's system, and applicants have many ways to have their arguments and evidence heard and evaluated by the PTO before a district court does so in a section 145 action.

Furthermore, the Government's proposed standard does not preclude evidence that was not reasonably available earlier. The applicant can easily identify reasons for not previously presenting evidence (*e.g.*, it was newly discovered or it is testimony that could not be presented in the PTO) and the applicant and Government can brief the issue for a decision by the district court. Indeed, district courts make these same types of determinations every day in non-patent cases.

E. Finally, there is no compelling policy argument to support the need for late introduction of evidence for which the applicant had a full and fair opportunity to present evidence earlier. Other amici have argued that withholding evidence from the PTO and submitting it for the first time to a district

allows applicants and the PTO to avoid addressing evidence that may turn out to be irrelevant. *See* Brief of Amicus Curiae Intellectual Property Owners Association on En Banc Rehearing in Support of Neither Party, at 16-18. The argument rests on the flawed presumption that applicants will be frightened into over-disclosure. But the patent examiner's rejections define and significantly narrow the issues an applicant is required to address—*e.g.*, if the examiner provides only a "written description" rejection, then the applicants need introduce only evidence to counter that particular rejection, and need not provide declarations or evidence about other issues. If such an approach would truly lighten the prosecution load, one would expect the over-burdened PTO to be the first to advocate for it.[11] There is simply no support for the proposition that sandbagging is superior in terms of efficiency.

---

[11] Again, Hyatt's own course of conduct illustrates the problems with the Federal Circuit's standard. Hyatt was invited by the examiner to submit very specific evidence—there was no danger of him not knowing what to provide, and having to provide a wasteful amount of evidence. But when asked to show where the concepts in his claims appeared in his specification, he submitted an index of claim terms, and not of actual concepts. This wasteful back-and-forth not only delayed a useful decision on Hyatt's application, but it pulled PTO resources away from other applicants.

CONCLUSION

The judgment of the court of appeals should be reversed.

Respectfully submitted.

LAUREN A. DEGNAN
Fish & Richardson P.C.
1425 K Street, N.W. Suite 1100
Washington, DC 20005
(202) 783-5070

JOHN A. DRAGSETH
Counsel of Record
Fish & Richardson P.C.
3200 RBC Plaza
60 South 6th Street
Minneapolis, MN 55402
(612) 335-5070
dragseth@fr.com

Counsel for Amici

SEPTEMBER 2011

AMICUS CURIAE BRIEF

No. 10-1219

IN THE

Supreme Court of the United States

DAVID J. KAPPOS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR, UNITED STATES PATENT AND TRADEMARK OFFICE
Petitioner,
v.

GILBERT P. HYATT
Respondent.

ON WRIT OF CERTIORARI TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

BRIEF OF *AMICUS CURIAE* INTELLECTUAL PROPERTY OWNERS ASSOCIATION IN SUPPORT OF NEITHER PARTY

DOUGLAS K. NORMAN,
President
KEVIN H. RHODES
Chair, Amicus Brief Committee
INTELLECTUAL PROPERTY OWNERS ASSOCIATION
1501 M. Street, N.W.
Suite 1150
Washington, D.C. 20005
(202) 507-4500

ROBERT M. ISACKSON
Counsel of Record
JACOB A. SNOW
NICHOLAS H. LAM
ORRICK, HERRINGTON & SUTCLIFFE LLP
51 West 52nd Street
New York, NY 10019
(212) 506-5000
rmisackson@orrick.com

September 6, 2011

Counsel for Amicus Curiae

TABLE OF CONTENTS

TABLE OF AUTHORITIES iii

INTERESTS OF AMICUS CURIAE 1

SUMMARY OF ARGUMENT 2

ARGUMENT 4

I. **THE FEDERAL CIRCUIT'S RULING ON THE INTRODUCTION OF NEW EVIDENCE IS CONSISTENT WITH THE STATUTE'S TEXT AND PURPOSE.** 4

A. **The Main Purpose of Civil Action Remedies Under Section 145 and its Sister Section 146 is to Allow Consideration of Evidence not Submitted to the PTO.** 5

B. **The Administrative Procedure Act Does Not Limit Introduction of New Evidence Under Section 145.** 6

C. **The Government's Proposed Rule Would Effectively Eliminate Review in District Court Under Section 145.** 7

D. **The Government's Proposed "No Reasonable Opportunity" Rule Will Force Applicants to Burden the PTO With Unnecessary Submissions.** 11

II. **ALL FACTUAL FINDINGS IN SECTION 145 ACTIONS SHOULD BE *DE NOVO*.** 13

A. **A Single Uniform Standard of Review Should Apply to All District Court Factfinding in Section 145 Actions.** 14

B. The Government's "Thorough Conviction" Standard of Review is Practically Unworkable. 17

CONCLUSION 19

TABLE OF AUTHORITIES

Cases

Burlington Indus., Inc. v. Quigg,
822 F.2d 1581 (Fed. Cir. 1987) 6, 15

Dickinson v. Zurko,
527 U.S. 150 (1999) ..... passim

Digital Control, Inc. v. Charles Machine Works,
437 F.3d 1309 (Fed. Cir. 2006) 11

Fregeau v. Mossinghoff,
776 F.2d 1034 (Fed. Cir. 1985) 11, 15

Genentech, Inc. v. Chiron Corp.,
220 F.3d 1345 (Fed. Cir. 2000) 11

Goldberg v. Kelly,
397 U.S. 254 (1970) 9

Hoover Co. v. Coe,
325 U.S. 79 (1945) 7

In re Watts,
354 F.3d 1362 (Fed. Cir. 2004) 8

Johnson v. Mukasey,
248 F.R.D. 347 (D.D.C. 2008) 9

Koki v. Dudas,
556 F. Supp. 2d 41 (D.D.C. 2008) 10

Mazzari v. Rogan,
323 F.3d 1000 (Fed. Cir. 2003) 5, 11, 15

McKart v. United States,
395 U.S. 185 (1969) 7

Microsoft Corp v. i4i Ltd. Partnership,
131 S.Ct. 2238 (2011) 3, 14

Morgan v. Daniels,
153 U.S. 120 (1894) 16

Tagg Bros. & Moorhead v. United States,
280 U.S. 420 (1930) 7

Therasense, Inc. v. Becton, Dickinson, and Co.,
--- F.3d. ---, 2011 WL 2028255, (Fed. Cir. 2011). 12

United States v. Banks,
546 F.3d 507 (7th. Cir. 2008) 9

Winner International Royalty Corp. v. Wang,
202 F.3d 1340 (Fed. Cir. 2000) 5, 16

Regulations

37 C.F.R. §1.56 10

Statutes

35 U.S.C. §141 ..... passim

35 U.S.C. §145 ..... passim

Other Authorities

Brief for the Petitioner, April 7, 2011 18

IRAH H. DONNER, PATENT PROSECUTION: LAW, PRACTICE, AND PROCEDURE, (2009) 6

PATENT AND TRADEMARK OFFICE, PROCESS PRODUCTION REPORT FY 2004, http://www.uspto.gov/ip/boards/bpai/stats/process/fy2004.pdf (last visited September 1, 2011) 12

PATENT AND TRADEMARK OFFICE, PROCESS PRODUCTION REPORT FY 2010 http://www.uspto.gov/ip/boards/bpai/stats/process/fy2010sepb.pdf (last visited September 1, 2011). 12

INTERESTS OF AMICUS CURIAE[1]

Amicus curiae Intellectual Property Owners Association (IPO) is a trade association representing companies and individuals in all industries and fields of technology who own or are interested in U.S. intellectual property rights. IPO's membership includes more than 200 companies and more than 12,000 individuals who are involved in the association either through their companies or as inventor, author, executive, law firm, or attorney members. Founded in 1972, IPO represents the interests of all owners of intellectual property. IPO members receive about thirty percent of the patents issued by the Patent and Trademark Office to U.S. nationals. IPO regularly represents the interests of its members before Congress and the United States Patent and Trademark Office (PTO) and has filed *amicus curiae* briefs in this Court and other courts on significant issues of intellectual property law. The members of IPO's Board of Directors, which

---

[1] Pursuant to Supreme Court Rule 37.6, *amicus curiae* certifies that no counsel for a party authored this brief in whole or in part, and that no person or entity, other than *amicus*, its members, or its counsel, has made any monetary contribution to the preparation or submission of this brief. *Amicus curiae's* counsel researched and drafted this brief with the advice and consent of *amicus curiae*. Both parties in this case have consented to the filing of this *amicus curiae* brief in support of neither party. Petitioner consented to the filing of this brief in the attached letter. Respondent consented to the filing of all amicus briefs in a letter to this Court.

approved the filing of this brief, are listed in the Appendix.[2]

IPO has no interest in any party to this litigation nor does IPO have a stake in the outcome of this case *per se*, other than its interest in seeking a correct and consistent interpretation and administration of the law on behalf of its members. IPO respectfully submits this *amicus curiae* brief in support of neither party.

SUMMARY OF ARGUMENT

IPO advocates in support of intellectual property laws that provide, strong, cost-effective, and reliable intellectual-property protection. IPO believes that the government's position in this case will render prosecution before the PTO less reliable and more costly, unduly limit statutorily guaranteed rights to seek factual review of adverse patentability determinations, and further burden the PTO examiners with factual submissions aimed at laying a predicate for a hypothetical, and quite unlikely, eventual challenge in district court.

First, Congress enacted 35 U.S.C. §145 for the specific purpose of allowing an applicant to introduce new evidence not offered at the PTO, in contrast to 35 U.S.C. §141, which permits a direct appeal from the PTO to the Federal Circuit based solely on the PTO record. The government's "no reasonable opportunity" standard would exclude almost all new

---

[2] IPO procedures require approval of positions in *amicus curiae* briefs by a three-fourth majority of directors present and voting.

evidence, since the Director of the PTO (Director) will almost always be able to argue that the new evidence in question could have been submitted to the PTO. Foreclosing the introduction of almost all new evidence under such a rule would effectively eviscerate district court review under section 145. Moreover, the general agency-review principles of the Administrative Procedure Act (APA) have no proper application limiting the introduction of new evidence in civil actions filed pursuant to section 145, as Congress enacted the statute to allow new evidence, as opposed to the APA-type judicial review under section 141.

Second, the government proposes an ambiguous, and ultimately unworkable standard, both for admitting new evidence and weighing it against the existing PTO record. The government's overly restrictive rule will disturb practice before the PTO, because applicants, concerned about being foreclosed from supplementing the record in district court, will burden themselves and the already overwhelmed PTO with unnecessary evidentiary submissions that examiners must consider in determining patentability.

Third, the government's shifting, variable standard of review – including a novel remand procedure for the PTO to consider evidence in the first instance – is an unnecessarily complicated and impractical rule with no basis in the statute. This Court should follow its recent guidance in *Microsoft Corp v. i4i Ltd. Partnership*, 131 S.Ct. 2238, 2250 (2011), in which the Court cautioned against "a standard of proof that would rise and fall with the facts of each case." As a result, the district court's

entire review should be *de novo* regardless of whether new evidence is submitted, consonant with Congress's intent in establishing section 145 as an alternative to section 141.

The Federal Rules of Civil Procedure and the Federal Rules of Evidence adequately govern the admissibility and weighing of evidence in district courts. Without explicit Congressional direction to the contrary, the same rules should govern admissibility in civil actions brought under section 145, and review of all evidence should be *de novo*.

ARGUMENT

I. The Federal Circuit's Ruling on The Introduction of New Evidence is Consistent With the Statute's Text and Purpose.

The Federal Circuit correctly held that there is no limitation on an applicant's right to introduce new evidence in a section 145 civil action merely because it was not submitted to the PTO. Furthermore, the realities of prosecution practice demonstrate that the imposition of additional barriers to introduction of new evidence in district court threatens to undermine Congress's primary purpose in providing a remedy for denial of a patent by civil action challenge before a fact-finding body – allowing the introduction of evidence not submitted to the PTO in the patentability determination. Moreover, understanding the interests of applicants proceeding before the PTO and the district court reveals that the government's concern that patentees will "game the system" by withholding evidence from the PTO is without basis.

A. The Main Purpose of Civil Action Remedies Under Section 145 and its Sister Section 146 is to Allow Consideration of Evidence not Submitted To The PTO.

An applicant dissatisfied with a ruling of the PTO's Board of Patent Appeals and Interferences (the Board) has two avenues for relief: an appeal to the Federal Circuit, or a civil action in district court in the District of Columbia. *See* 35 U.S.C. §§ 141, 145. The Federal Circuit's review under section 141 is limited to the proceedings before the PTO, and determines only whether the Board's conclusions are supported by substantial evidence. *Dickinson v. Zurko*, 527 U.S. 150, 165 (1999). In civil actions brought under sections 145 (patent applications) and 146 (patent interferences), on the other hand, evidence not submitted to the PTO is admissible. *Winner International Royalty Corp. v. Wang*, 202 F.3d 1340, 1345-46 (Fed. Cir. 2000). It has long been Federal Circuit law that when new evidence is introduced on a particular issue of fact considered by the PTO, the district court's review of the PTO's conclusion on that issue is *de novo*. *Id.*

A patent applicant selects a district court challenge to an adverse decision of the Board, as opposed to a Federal Circuit appeal, solely in order to supplement the record with evidence and testimony not submitted to the PTO or considered by the Board; there is no other purpose under the statute. *See* 35 U.S.C. § 141, 145; *Mazzari v. Rogan*, 323 F.3d 1000 (Fed. Cir. 2003) ("A section 145 review is

distinct from a section 141 appeal in that it affords the applicant an opportunity to present additional evidence . . . ."); *Zurko*, 527 U.S. at 164 (contrasting district court with Federal Circuit review on the basis that applicants in section 145 district court actions can "present to the court evidence that the applicant did not present to the PTO"). Indeed, a leading patent prosecution practice guide recommends that applicants seek district court review when they wish to "gather additional facts outside the prosecution history," but notes that an appeal to the Federal Circuit "is proper when the applicant is satisfied with [the prosecution history] record." IRAH H. DONNER, PATENT PROSECUTION: LAW, PRACTICE, AND PROCEDURE, 430-31 (2009).

The Federal Circuit has long recognized the critical importance of district court review of new evidence, emphasizing that a district court's reversal of the PTO's conclusion based on new evidence "is not contrary to the legislative purpose of section 145 *de novo* review. Indeed, it is a fulfillment of that purpose." *Burlington Indus., Inc. v. Quigg*, 822 F.2d 1581, 1584 (Fed. Cir. 1987). Review of new evidence, the Federal Circuit wrote, is a "powerful advantage over the patent examiner" that is "characteristic of section 145 appeals." *Id.* at 1584.

B. The Administrative Procedure Act Does not Limit Introduction of new Evidence Under Section 145.

The government, while admitting that section 145 does not "wholly preclude" introduction of new evidence (in contrast to review under the APA), argues that the "principles" of administrative

exhaustion should nonetheless apply. This argument is misplaced; neither the statutory scheme nor sound concerns of public policy support the application of exhaustion principles to bar the introduction of new evidence in section 145 actions.

The cases the government relies on, including *Tagg Bros. & Moorhead v. United States*, 280 U.S. 420, 444 (1930), and *McKart v. United States*, 395 U.S. 185 (1969), arise in circumstances where APA authorized review is limited to the agency record. To the extent these cases reflect a general principle that agencies should, whenever possible, serve as an initial factfinder, this Court already concluded in *Zurko* that section 145 constitutes a departure from that principle. If Congress had intended that the PTO review all possible evidence in the first instance, it would not have provided applicants with an option to seek a remedy by civil action, where the district court may hear live testimony, make findings of fact, and reach conclusions of law on patentability. *See Hoover Co. v. Coe*, 325 U.S. 79, 83 (1945) (noting that the statutory predecessor to section 145 allows for "a formal trial...on proof which may include evidence not presented in the Patent Office").

C. The Government's Proposed Rule Would Effectively Eliminate Review in District Court Under Section 145.

As enacted by Congress, the statute ensures that the opportunity to supplement the record before the PTO in district court comes at a significant cost and carries no assurance of success. First, section 145 requires that the applicant pay "all the expenses of the proceedings." 35 U.S.C. § 145. Second,

generally, no new legal issues can be raised that were not presented to the PTO. *In re Watts*, 354 F.3d 1362, 1367 (Fed. Cir. 2004).

The practical result of these limits is that an applicant's assessment whether to bear the significant additional cost of a district court challenge depends largely on the likelihood that his contemplated new evidence will result in a reversal of the PTO's determination of unpatentability. The applicant must, then, have significant confidence that evidence offered for the first time will be persuasive if not dispositive for the district court. That so few district court actions are filed under section 145 confirms that applicants carefully consider and then select the case-appropriate avenue for relief.[3]

---

[3] A search in Lex Machina's (https://lexmachina.com/) patent filings database for citations to 35 U.S.C. § 145 in patent complaints in the United States District Court for the District of Columbia revealed only four actions filed pursuant to 35 U.S.C. § 145 so far in 2011, two such actions in 2010, and five in 2009 (including two filed by Mr. Hyatt). For the years stated, patent complaints in the District Court for the District of Columbia were searched for "'35 U.S.C. 145' ~10" which will return all documents including "35" "U.S.C." and "145" with a maximum of 10 words separating each term. Lex Machina is a commercial subscription service that pulls documents and docket information from the United States Courts' Public Access to Court Electronic Records (PACER) database. While the PACER database may not have a record of every

But these same considerations raise the possibility that the government's novel rule will effectively eliminate the "Civil Action to Obtain Patent" under section 145. This is because the Director will almost always be able to argue that an applicant had a reasonable opportunity to present the new evidence to the PTO examiner. Indeed, the government's proposed gate-keeping standard would appear to limit new evidence in section 145 actions to material discovered after PTO proceedings have concluded (or perhaps evidence in a form the PTO does not hear, such as live testimony[4]). Once the

---

section 145 action, and the stated search results may not be perfectly accurate, the results provide as a useful estimate of the volume of section 145 actions. Appeals to the Federal Circuit pursuant to section 141 do not appear to be any more common. According to a review of all Federal Circuit opinions and orders matching citing to 35 U.S.C. § 141, there were six such orders or opinions in 2010, three in 2009, and one in each of 2008, 2007, 2006, and 2005.

[4] In many cases, a court can make assessments of the veracity of testimony through a transcript or affidavit without the need for a live hearing. *See, e.g., Johnson v. Mukasey*, 248 F.R.D. 347 (D.D.C. 2008) (noting that magistrate reviewed, on a written record, objections to the veracity of an affidavit); *see also United States v. Banks*, 546 F.3d 507, 511 (7th. Cir. 2008). In other circumstances, live testimony may be necessary. *See, e.g., Goldberg v. Kelly*, 397 U.S. 254 (1970) ("[W]ritten submissions do not afford the flexibility of oral presentations; they do not permit the recipient to mold his argument to the issues the decision maker appears to regard as

Director has advanced such an argument, the applicant must rebut it or face exclusion of critical new evidence – the applicant's only reason for pursing a district court action in the first instance – from his case.

The government's proposed "no reasonable opportunity" rule thus threatens to "render an appeal under section 145 nearly indistinguishable from a direct appeal to the Federal Circuit" under section 141, based solely on the PTO record, "and would render the purpose of the statute duplicative and meaningless." *See Koki v. Dudas*, 556 F. Supp. 2d 41, 47 (D.D.C. 2008) (considering a far less restrictive rule).

The government argues that its restrictive rule is necessary to encourage full disclosure by applicants before the PTO. But the policy of encouraging disclosure needs no further intrusion from the courts. Preliminarily, the PTO has adopted, and the courts have enforced, 37 C.F.R. § 1.56, which ably incents applicants to make a full disclosure to the PTO in seeking patent protection. More fundamentally, Congress understood the importance

---

important. Particularly where credibility and veracity are at issue, as they must be in many termination proceedings, written submissions are a wholly unsatisfactory basis for decision."). Thus, under the government's proposed "no reasonable opportunity" standard of review, the Director may successfully foreclose even live testimony when the new evidence proffered to the district court could have been submitted in written form by declaration to the PTO.

of applicants presenting their full case to the PTO, and ensured that applicants are able to by requiring that the applicant pay expenses of a district court action under section 145. Congress thus struck a policy balance between encouraging disclosure to the PTO and allowing supplementation of the PTO record on which the district court may find facts and reach conclusions of law. By placing its thumb on the scales, the government's proposed rule would unnecessarily disturb practice before both the district court and the PTO.

D. The Government's Proposed "No Reasonable Opportunity" Rule Will Force Applicants to Burden the PTO With Unnecessary Submissions.

The government's proposed rule would disturb the settled expectations of applicants before the PTO and upend current district court practice in section 145 proceedings. The Federal Circuit has long allowed district courts to admit new evidence irrespective of whether an applicant had a "reasonable opportunity" to present the evidence to the PTO. *See, Mazzari*, 323 F.3d at 1003 (Fed. Cir. 2003) (considering new prior art references and expert declarations offered by the PTO and applicants); *Genentech, Inc. v. Chiron Corp.*, 220 F.3d 1345 (Fed. Cir. 2000) (considering testimony of four new experts despite fact that none had offered testimony in PTO proceedings); *Fregeau v. Mossinghoff*, 776 F.2d 1034, 1036 (Fed. Cir. 1985) (considering applicant's new expert declaration setting forth additional data and new theory). The Federal Circuit has furthermore consistently recognized that the only obligation of disclosure

imposed on applicants is 37 C.F.R.1.56. *See e.g., Digital Control, Inc. v. Charles Machine Works*, 437 F.3d 1309, 1314-16 (Fed. Cir. 2006) (discussing standard of materiality in "new" Rule 56). *See also Therasense, Inc. v. Becton, Dickinson, and Co.*, --- F.3d. ---, 2011 WL 2028255, *14-*16 (Fed. Cir. 2011) (declining to adopt Rule 56's definition of materiality for inequitable conduct).

Should this Court adopt the government's restrictive rule, applicants, justifiably concerned about the exclusion of evidence from a later civil action challenge, would be incented to overwhelm the PTO examiners with extraneous facts and evidentiary submissions.[5] This threat is made all the more likely given the dramatic increase in appeals to the Board in recent years.[6] Presently,

---

[5] There is strong precedent that applicants will, out of caution, burden the PTO with a deluge of additional evidence. As the Federal Circuit noted in *Therasense*, "[w]ith inequitable conduct casting the shadow of a hangman's noose, it is unsurprising that patent prosecutors regularly bury the PTO examiners with a deluge of prior art references, most of which have marginal value...This tidal wave of disclosure makes identifying the most relevant prior art more difficult....This flood of information strains the agency's examining resources and directly contributes to the backlog." 2011 WL 2028255 at *9.

[6] According to statistics published by the PTO, in 2004 there were a total of 2469 appeals to the Board. PATENT AND TRADEMARK OFFICE, PROCESS PRODUCTION REPORT FY 2004, available at http://www.uspto.gov/ip/boards/bpai/stats/process/fy2004.pdf (last visited September 1, 2011). In 2010

applicants proceeding before the PTO strike a strategic balance, submitting evidence likely sufficient to obtain a patent while avoiding overburdening the PTO because, should it be necessary and important enough, applicants can present additional evidence to the district court under section 145. And if no further evidence is needed, review may instead be had before the Federal Circuit under section 141. This is the framework Congress enacted.

The government's proposed rule, and the burden on applicants, the PTO, and the courts that will follow from it, are entirely unnecessary. This Court should reject that rule and hold that evidence in section 145 challenges is admissible according to the same clear, established standards that apply in other civil actions: the Federal Rules of Civil Procedure and the Federal Rules of Evidence.

II. All Factual Findings in Section 145 Actions Should be *De Novo*.

The Federal Circuit erred in creating a standard of review for section 145 civil actions that varies based on whether evidence was considered by the PTO or newly introduced in the district court. Further, the language of the statute and Court's precedent indicate that a section 145 civil action should be a completely *de novo* proceeding whether

---

that number had increased five-fold to 12,380. PATENT AND TRADEMARK OFFICE, PROCESS PRODUCTION REPORT FY 2010, available at http://www.uspto.gov/ip/boards/bpai/stats/process/fy2010sepb.pdf (last visited September 1, 2011).

or not new evidence is submitted by one of the parties.

A. A Single Uniform Standard of Review Should Apply to All District Court Factfinding in Section 145 Actions.

A standard of review in district court that varies, factual issue by factual issue, has no statutory basis and will cause unnecessary practical difficulties in section 145 civil actions. As the Court recently wrote in *Microsoft*, 131 S.Ct. at 2250:

> Nothing in [the statute's] text suggests that Congress meant to depart from that understanding to enact a standard of proof that would rise and fall with the facts of each case. Indeed, had Congress intended to drop the heightened standard of proof where the evidence before the jury varied from that before the PTO – and thus take the highly unusual and impractical step of enacting a variable standard of proof that must itself be adjudicated in each case – we assume it would have done so expressly.

This Court should be no more inclined to erect a variable standard of review for section 145 actions. *See Zurko*, 527 U.S. at 164 (1999) ("Recognizing the importance of maintaining a uniform approach to judicial review of administrative action, we have closely examined the Federal Circuit's claim for an exception to that uniformity.") (finding no exception). No basis for any variation exists here: section 145

says nothing of a varying standard of review, commanding instead that the district court judge review the facts in the case "as they may appear." 35 U.S.C. § 145.

A long line of Federal Circuit cases hold that the statute's language requires that factual issues are reviewed *de novo* when new evidence is submitted. *See Mazzari*, 323 F.3d at 1005 (Fed. Cir. 2003) (deciding that following *Zurko*, "if the parties choose to present additional evidence to the district court...the district court would make *de novo* factual findings..."); *Burl ington Indus., Inc. v. Quigg*, 822 F.2d 1581, 1584 (Fed. Cir. 1987) (noting that in a section 145 civil action "when additional evidence is adduced beyond that before the PTO the factual weight must be determined afresh"); *Fregeau*, 776 F.2d at 1038 (Fed. Cir. 1985) (noting that "where new evidence is presented to the district court on a disputed fact question, a *de novo* finding will be necessary to take such evidence into account together with the evidence before the board").

Indeed, there are strong practical reasons for the Court's aversion to a shifting standard of review. Under a single *de novo* standard, it is not necessary for the district court to determine (based on argument of the parties) how—or whether—each piece of new evidence should affect the standard of review. Only a single, uniform standard of review is appropriate in a section 145 civil action, because in many cases it will be difficult or impossible to draw the line between discrete "issues" to which variable standards should apply.

As the Federal Circuit has recognized, it can be difficult or impossible to distinguish such factual issues for the purpose of determining which pieces of evidence apply to which facts. "[W]e do not decide whether a given dispute could be parsed into discrete "issues" or facts such that a determination could be made, or if it could, how a court would draw the line between such facts or issues." *Winner Int'l*, 202 F.3d at 1347 n.4 (Fed. Cir. 2000).

Moreover, a single, simple standard is easier for district court judges – and parties – to apply. A variable standard will result in litigants wasting the court's and the parties' resources by arguing that the standard of review should be strict or lenient on particular issues for reasons of expedience (i.e., encouraging deference for favorable PTO rulings, *de novo* for unfavorable ones). Certainly newly-introduced evidence must be reviewed *de novo* – there is no record to which deference can be afforded. Thus, *de novo* is the only uniform standard of review possible. It is better, more efficient, and more effective to avoid the dual-standard quagmire entirely with a single, uniform *de novo* standard of review for all evidence.

Petitioner's arguments to the contrary should be rejected. Petitioner relies heavily on *Morgan v. Daniels*, 153 U.S. 120, 125 (1894). In *Morgan*, however, no new evidence was introduced and the *Morgan* court did not discuss what the standard of review would have been in such a circumstance. Furthermore, the government's broad interpretation of *Morgan* applying it to section 145, cannot be reconciled with the Court's later holdings. First, as the Court pronounced in *Zurko*, "[t]he presence of

such new or different evidence makes a factfinder of the district judge." 527 U.S. at 164.[7] And second, such an interpretation of *Morgan* conflicts with *Microsoft*'s admonition that a standard of proof should not "rise and fall with the facts of each case." *Microsoft*, 131 S.Ct. at 2250. The Court should reconcile the tension between *Morgan* and the Court's more recent pronouncements in *Zurko* and *Microsoft* by requiring across-the-board *de novo* factual review in section 145 civil actions.

B. The Government's "Thorough Conviction" Standard of Review is Practically Unworkable.

The government's proposed standard of review is unworkable for at least two reasons. First, it erects yet another barrier to district court fact-finding by requiring that, if the applicant submits any evidence that could have been submitted to the PTO, then the district court shall remand to the PTO for consideration in the first instance. Brief for the Petitioner, April 7, 2011 at 24. And second, it provides for a sliding, flexible standard of review

---

[7] *Zurko*'s earlier statement that a court reviewing a "record-based factual conclusion" should inquire only whether the conclusion in question is supported by "substantial evidence" is not to the contrary. 527 U.S. at 164. *Zurko*'s holding, like other cases the government cites, was limited to Federal Circuit review under section 141, which is limited to the record before the PTO. In this regard, IPO's position here on the scope of *de novo* review evolved from that stated in its *amicus curiae* brief in the Federal Circuit based on a reassessment under *Microsoft*.

depending on the nature of the evidence presented. Neither of these rules have any basis in the statute, and both would create unnecessary costs for applicants and courts and delay applicants their relief.

Consider the analytical and procedural steps the government would require of a district judge faced with evidence not presented to the PTO. First, after determining that evidence is new, the court must determine whether the applicant had a "reasonable opportunity" to present the evidence to the PTO. Pet. at 23. If not, then the court must decide whether the evidence "consists of materials that the PTO can consider as part of its examination process." *Id.* at 24. If the evidence can be considered by the PTO, the district court should remand to the PTO. *Id.* If it cannot, the district court should make an assessment of the facts to determine if "the new evidence, considered together with the administrative record, creates a 'thorough conviction' that the PTO erred. *Id.* at 25. Such an intricate procedure will only dissuade applicants from exercising their statutorily guaranteed rights, and it serves no useful purpose. Instead, the district court should adjudicate questions of patentability "as the facts in the case may appear," just as the statute directs. 35 U.S.C. § 145.

As for the standard of review, the government notes that "the court may give the new evidence more weight in the analysis, in recognition of the fact that the PTO's conclusions did not take that evidence into account." Pet. at 24. As the government admits, under this standard, "the manner in which [new] evidence is considered may vary depending on the

nature of the evidence." *Id.* The deference to the PTO, in other words, will depend on the nature and type of evidence for each new piece of evidence introduced. This is exactly the kind of shifting standard of review that will "rise and fall with the facts of each case" that the Court cautioned against in *Microsoft*. 131 S.Ct. at 2250.

CONCLUSION

For the foregoing reasons, IPO respectfully requests that the Court hold that 1) admissibility of new evidence in civil actions under 35 U.S.C. § 145 is governed only by the Federal Rules of Civil Procedure and the Federal Rules of Evidence; and 2) that all of the district court's factual findings in such civil actions shall be decided *de novo*.

RESPECTFULLY SUBMITTED,

DOUGLAS K. NORMAN,
President
KEVIN H. RHODES
Chair, Amicus Brief Committee
INTELLECTUAL PROPERTY OWNERS ASSOCIATION
1501 M. Street, N.W.
Suite 1150
Washington, D.C. 20005
(202) 507-4500

ROBERT M. ISACKSON
Counsel of Record
JACOB A. SNOW
NICHOLAS H. LAM
ORRICK, HERRINGTON & SUTCLIFFE LLP
51 West 52nd Street
New York, NY 10019
(212) 506-5000

APPENDIX

APPENDIX — MEMBERS OF THE BOARD OF DIRECTORS INTELLECTUAL PROPERTY OWNERS ASSOCIATION

APPENDIX[1]

Members of the Board of Directors Intellectual Property Owners Association

T.J. Angioletti
Oracle USA, Inc.

Russell W. Binns
Avaya Inc.

William J. Coughlin
Ford Global Technologies LLC

Timothy J. Crean
SAP AG

Robert DeBerardine
Sanofi-Aventis

Bart Eppenauer
Microsoft Corp.

Mark Farber
Covidien

---

1. IPO procedures require approval of positions in briefs by a three-fourths majority of directors present and voting.

Appendix

Scott M. Frank
AT&T

Darryl P. Frickey
Dow Chemical Co.

Bernard J. Graves, Jr.
Eastman Chemical Co.

Krish Gupta
EMC Corporation

Jack E. Haken
Koninklijke Philips Electronics N.V.

Dennis R. Hoerner, Jr.
Monsanto Co.

Carl B. Horton
General Electric Co.

Soonhee Jang
Danisco U.S. Inc.

Michael Jaro
Medtronic, Inc.

Philip S. Johnson
Johnson & Johnson

George William Johnston
Roche Inc.

Appendix

Lisa K. Jorgenson
STMicroelectronics, Inc.

Dean Kamen
DEKA R&D Corp.

Charles M. Kinzig
GlaxoSmithKline

David J. Koris
Shell International B.V.

Mark W. Lauroesch
Corning Inc.

Scott P. McDonald
Mars Inc.

Jonathan P. Meyer
Motorola, Inc.

Steven W. Miller
Procter & Gamble Co.

Jeffrey L. Myers
Adobe Systems Inc.

Douglas K. Norman
Eli Lilly and Co.

Sean O'Brien
United Technologies Corp.

Richard F. Phillips
Exxon Mobil Corp.

Kevin H. Rhodes
3M Innovative Properties Co.

Mark L. Rodgers
Air Products & Chemicals, Inc.

Curtis Rose
Hewlett-Packard Co.

Manny Schecter
IBM Corp.

Steven J. Shapiro
Pitney Bowes Inc.

David M. Simon
Intel Corp.

Dennis C. Skarvan
Caterpillar Inc.

Russ Slifer
Micron Technology, Inc.

Daniel J. Staudt
Siemens Corp.

Brian K. Stierwalt
ConocoPhillips

Thierry Sueur
Air Liquide

James. J. Trussell
BP America, Inc.

Cheryl J. Tubach
J.M. Huber Corp.

Danise Van Vuuren-Nield
The Coca-Cola Co.

Roy Waldron
Pfizer, Inc.

Michael Walker
DuPont

BJ Watrous
Apple Inc.

Stuart L. Watt
Amgen, Inc.

Jon D. Wood
Bridgestone Americas Holding, Inc.

Paul D. Yasger
Abbott Laboratories

AMICUS CURIAE BRIEF

RECORD
AND
BRIEFS

No. 10-1219

IN THE

Supreme Court of the United States

DAVID J. KAPPOS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR, UNITED STATES PATENT AND TRADEMARK OFFICE,

Petitioner,

v.

GILBERT P. HYATT,

Respondent.

ON WRIT OF CERTIORARI TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

BRIEF OF *AMICUS CURIAE* NEW YORK INTELLECTUAL PROPERTY LAW ASSOCIATION IN SUPPORT OF NEITHER PARTY

JOHN M. HINTZ
Co-Chair, Committee on Amicus Briefs
NEW YORK INTELLECTUAL PROPERTY LAW ASSOCIATION
c/o CHADBOURNE & PARKE LLP
30 Rockefeller Plaza
New York, NY 10112
(212) 408-1036

DAVID F. RYAN
Co-Chair, Committee on Amicus Briefs
NEW YORK INTELLECTUAL PROPERTY LAW ASSOCIATION
1214 Albany Post Road
Croton-on-Hudson, NY 10520
(914) 271-2225

CHARLES E. MILLER
Counsel of Record
DICKSTEIN SHAPIRO LLP
1633 Broadway
New York, NY 10019-6708
(212) 277-6500
millercharles@dicksteinshapiro.com

THERESA M. GILLIS
President
NEW YORK INTELLECTUAL PROPERTY LAW ASSOCIATION
c/o MAYER BROWN LLP
1675 Broadway
New York, NY 10019-5820
(212) 506-2500

September 6, 2011

237876

Library of Congress
Law Library

TABLE OF CONTENTS

Page

TABLE OF CONTENTS i

TABLE OF CITED AUTHORITIES ii

INTEREST OF *AMICUS CURIAE* 1

I. INTRODUCTION 4

II. SUMMARY OF ARGUMENT 11

III. ARGUMENT 14

POINT I — The APA Does Not Conflict With the Statutory Enablement of Article III Court Adjudication of Government-Agency Actions Wherein the Admission of New Evidence is Governed By the Federal Rules of Evidence 14

POINT II — The Patent Act at 35 U.S.C. § 145 Enables a Full Trial *De Novo* in a District Court for Adjudication of PTO Decisions in Other Settings 24

IV. CONCLUSION 27

TABLE OF CITED AUTHORITIES

Page

CASES

Anderson v. Liberty Lobby, Inc.,
477 U.S. 242 (1986) 15

Bally Gaming, Inc. v. Kappos,
Civil Action 1:10-cv-1906 (D.D.C.)..... 27

Barrett Co. v. Koppers Co.,
22 F.2d 395 (3d Cir. 1927)..... *passim*

California Research Corp. v. Ladd,
356 F.2d 813 (D.C. Cir. 1966)..... 10, 11

Chandler v. Roudebush,
425 U.S. 840 (1976) 7

Chevron, U.S.A., Inc. v.
National Resources Defense Council, Inc.,
467 U.S. 837 (1984) 21

Citizens to Preserve Overton Park, Inc. v. Volpe,
401 U.S. 402 (1971) 19

Delano Farms, Co. v.
California Table Grape Commission,
__ F.3d ___, 2011 WL 3689249
(Fed. Cir. 2011) 5

DeSeversky v. Brenner,
424 F.2d 857 (D.C. Cir. 1970)..... 10, 11, 15

Cited Authorities

Page

Dickinson v. Zurko,
527 U.S. 150 (1999) 14

Dome Patent L.P. v. Kappos,
Civil Action 07-cv-1695 (D.D.C.) 27

Federal Housing Administration, Region 4 v. Burr,
309 U.S. 242 (1940) 9

Globe Union v. Chicago Tel. Supply Co.,
103 F.2d 722 (7th Cir. 1939) 10

Hyatt v. Doll,
576 F.3d 1246 (Fed. Cir. 2009) 9, 24

Hyatt v. Kappos,
625 F.3d 1320 (Fed. Cir. 2010) 9-10, 20, 26

In re Watts,
354 F.3d 363 (Fed. Cir. 2004) 15

Invitrogen Corp. v. President and Fellows of Harvard College,
2007 U.S. Dist. LEXIS 74282 (S.D. Cal. 2007) .. 19

Killian v. Watson,
121 U.S.P.Q. 507 (D.D.C. 1958) 10, 11

Marbury v. Madison,
5 U.S. (1 Cranch) 137 (1803) 4

Cited Authorities

Page

Mazzari v. Rogan,
323 F.3d 1000 (Fed. Cir. 2003) 14, 15

Minnesota Mining & Mfg. Co. v. Carborundum,
155 F.2d 746 (3d Cir. 1946) 11

Monsanto Co. v. Kamp,
269 F. Supp. 818 (D.D.C. 1967) 10

Morgan v. Daniels,
153 U.S. 120 (1894) 15, 16, 17

Morsemere Sav. & Loan Ass'n v. Marston,
500 F. Supp. 1253 (D.N.J. 1980) 7

Newton County Wildlife Ass'n v. Rogers,
141 F.3d 803 (8th Cir. 1998) 7

Power Integrations, Inc. v. Kappos,
Civil Action 1:11-cv-1254 27

Takeda Pharmaceutical Co. v. Dudas,
511 F. Supp. 2d 81 (D.D.C. 2007), *vacated and remanded*, 561 F.3d 1372 (Fed. Cir. 2009).. 10

Teles A.G. v. Kappos,
Civil Action 1:11-cv-0476 (D.D.C.) 27

Tse v. Kappos,
Civil Action 1:11-cv-1127 (D.D.C.) 27

Cited Authorities

Page

STATUTES

5 U.S.C. § 702 ..... 5, 6

5 U.S.C. § 706 19

5 U.S.C. § 706(2)(A) 6

5 U.S.C. § 706(2)(E) 6

5 U.S.C. § 706(2)(F) 6

15 U.S.C. § 1071(b) 5, 12, 26

15 U.S.C. § 1071(b)(1) 5

28 U.S.C. § 1295(a)(1) 14

28 U.S.C. § 1295(a)(4)(C) 14

35 U.S.C. § 2(b)(2) 21

35 U.S.C. § 24 17

35 U.S.C. § 32 26

35 U.S.C. §§ 131-133 16

35 U.S.C. § 134 ..... 16, 24

Cited Authorities

	Page
35 U.S.C. § 134(a)	16
35 U.S.C. § 135	16
35 U.S.C. § 141	*passim*
35 U.S.C. § 144	6, 14
35 U.S.C. § 145	*passim*
35 U.S.C. § 146	17, 21
35 U.S.C. § 154(b)(4)	26
35 U.S.C. § 251	16
35 U.S.C. § 305	24
35 U.S.C. § 306	*passim*
21st Century Department of Justice Appropriations Authorization Act of 2002	27
America Invents Act	25, 26, 27
American Inventors Protection Act of 1999	27
Civil Rights Act	7
Clean Water Act	7

Page

Endangered Species Act 7

Patent Act of 1952 ..... 3, 4

RULES

37 C.F.R. § 1.56 22

37 C.F.R. § 41.2 16

37 C.F.R. §§ 41.100-41.158 16

37 C.F.R. §§ 41.200-208 16

Fed. R. Civ. P. 1 8

Fed. R. Civ. P. 4(i)(2) 8

Fed. R. Civ. P. 24(b)(1)(B) 23

Fed. R. Civ. P. 26(a)(1)(A) 19

Fed. R. Civ. P. 26(a)(1)(B)(i) 19

Fed. R. Civ. P. 45 17

Fed. R. Civ. P. 56 19

Fed. R. Evid. 101 8

Fed. R. Evid. 102 13

Page

Fed. R. Evid. 401 9

Fed. R. Evid. 402 9

Fed. R. Evid. 403 ..... 9, 13

Fed. R. Evid. 702 20

Fed. R. Evid. 706 20

Fed. R. Evid. 1101 8

PENDING LEGISLATION

H.R. 1249, SEC. 6(h)(2)(A) 25

H.R. 1249, SEC. 7(c)(1) 25

S. 23, SEC. 5 (h)(2)(A) 25

S. 23, SEC. 6(c)(1) 25

OTHER AUTHORITIES

Moore's Federal Practice, 3d ed., § 24.10 (2008) ... 23

Charles E. Miller and Daniel P. Archibald, *Interpretive Agency-Rulemaking vs. Statutory District Court Review Jurisdiction in Ex Parte Patent Reexaminations*, 92 J. Pat. & Trademark Off. Soc'y, 498 (2011) 27

Cited Authorities

Page

Charles E. Miller and Daniel P. Archibald, *The "America Invents Act" and its Restriction on Judicial Recourse*, 39 AIPLA Q. J. 397 (Summer 2011) 25, 26

Gregory C. Sisk, *Litigation With The Federal Government*, 4th ed., § 3.22 (American Law Institute 2006) 5

Magna Carta (1215) 4

M.P.E.P. § 1216VI (8th ed., rev. 8, July 2010) 21

M.P.E.P. § 1260.02 (8th ed., rev. 8, July 2010) 21

INTEREST OF *AMICUS CURIAE*

With the parties' written consents, copies of which are submitted herewith, the New York Intellectual Property Law Association ("NYIPLA") respectfully submits this brief as *amicus curiae*, in support of neither party, pursuant to Rule 37 of the Rules of this Court.[1]

Amicus curiae NYIPLA has no financial stake in either party to this appeal nor any interest in its outcome other than the just and proper application of the law as it relates to the issue presented. The NYIPLA's sole purpose herein is to offer what assistance it can to the Court as it considers and decides this important case at the juncture of patent law, the rules of evidence and civil procedure, and administrative law. In particular, the NYIPLA files this brief in order to present certain observations that are intended to supplement rather than duplicate the arguments of the parties by bringing to the Court's attention material that may be quite different from that presented by the parties and which is relevant to some of the broader policy implications and heretofore unrecognized ramifications of widespread import in other contexts raised by the issue before the Court in respect to the Federal Circuit's en banc opinion for the review of which certiorari has been granted.[2]

---

1. Upon reasonable inquiry and investigation, *amicus curiae* NYIPLA believes that no party or its counsel authored or participated in preparing this brief in whole or in part, and that no one other than NYIPLA, its members, or its Counsel of Record herein made any contribution, in money or services, intended to fund or facilitate the preparation or submission of this brief.

2. The NYIPLA's silence on points and issues not addressed in this brief does not necessarily indicate agreement with positions taken by either of the parties on those points and issues.

Amicus curiae NYIPLA and its Counsel of Record appearing in this proceeding represent that they alone prepared this brief. The arguments set forth herein were approved as of September 2, 2011 by an absolute majority of the total number of officers and members of the Board of Directors of the NYIPLA (including officers and Board members who did not vote for any reason including recusal), but do not necessarily reflect the views of a majority of the members of the NYIPLA or of the firms with which those members are associated. After reasonable investigation, the NYIPLA believes that no officer, or member of its Board or Amicus Committee who voted in favor of this brief, or any attorney in the law firm or corporation of such an officer, Board or Committee member, or attorney who aided in preparing this Brief, represents a party with respect to the present litigation. Some officers, Board, or Committee members, or other attorneys in their respective law firms or corporations may represent entities, including other *amici curiae*, which have an interest in other matters that may be affected by the outcome of the present appeal.

The NYIPLA is one of the largest regional intellectual property ("IP") bar associations in the United States. Its membership consists of approximately 1,600 lawyers whose professional interests and practices lie mainly in the areas of patents, copyrights, trademarks, trade secrets and other forms of IP. NYIPLA's members include in-house counsel serving businesses and other organizations that deal with IP rights in all technologies and disciplines, as well as attorneys in private practice who represent IP owners and their adversaries. Entities served by the NYIPLA include inventors, entrepreneurs, venture capitalists, companies, universities, and industry and trade associations. NYIPLA members represent both

plaintiffs and defendants in IP litigations and regularly participate in matters before government agencies, including the prosecution of patent applications and other proceedings before the Patent and Trademark Office ("PTO").

Founded in 1922, the NYIPLA has achieved national recognition by its continuous, historic commitment to maintaining the integrity of the United States patent system, and to the proper application and observance of United States patent law by courts and agencies. Noteworthy in that regard are the contributions made by the Honorable Giles S. Rich, a celebrated member of the Court of Appeals for the Federal Circuit and its predecessor, the Court of Customs and Patent Appeals. While serving as the NYIPLA's 28th President (from 1951 to 1952) he was instrumental in the drafting and enactment of, and contributed to the preparation of an official commentary on, the Patent Act of 1952 embodied in title 35 of the United States Code (hereinafter referred to in its current form as the "Patent Act"). Later, during his career both as a patent lawyer and then as a jurist, Judge Rich continued to contribute significantly to the promotion of the Patent Act's vitality and relevance to both the American and global economies. Since then, the expeditious, efficient, and economical operation of the U.S. patent system, in accordance with sound legal principles, as embodied in the Patent Act, remains what is arguably one of the most important factors promoting the innovation-driven economy and well-being of the United States.

The NYIPLA supports the continued development of the principles and procedures governing judicial recourse from decisions of the PTO aimed at improving the process

for examining and granting patent applications, and the quality of patents issued by the Agency. However, restricting the right of patent applicants to exercise the broad, long-standing statutory right to judicial scrutiny of PTO decisions under the Patent Act is not a valid option. The NYIPLA believes that the challenges facing the U.S. patent system in the context of the judicial treatment of PTO decisions stem from issues raised by the Petitioner that can and should be addressed by applying sound jurisprudential principles.

I. INTRODUCTION

Since the early days of our Republic, the Judicial Branch has served as a recourse against unlawful conduct of the Executive. In *Marbury v. Madison*, 5 U.S. (1 Cranch) 137, 166 (1803), Chief Justice John Marshall noted that "[w]here a specific duty is assigned by law [to the Executive Branch], and individual rights depend upon the performance of that duty, it seems equally clear that the individual who considers himself injured has a right to resort to the laws of his country for a remedy". A more distant antecedent can be found in the *Magna Carta* (1215), ¶ 61 ("[I]f . . . any one of our officers, shall in anything be at fault towards anyone, and the offense be notified to four barons, . . . [they] shall . . . petition to have that transgression redressed without delay.")

Given the pervasive influence of the modern administrative state on the nation's affairs, decisions of federal agencies often concern issues whose plenary judicial resolution is justified by their far-reaching economic and social consequences. It is for this reason that the recognized need for a meaningful judicial check on agency action requires full access to the courts for

those aggrieved by the acts of such agencies. That access is provided by broad statutory waiver under the *Administrative Procedure Act* ("APA"), at 5 U.S.C. § 702 (1976), of the Government's sovereign immunity from suit by civil action seeking court adjudication of the merits of non-monetary, adverse agency-decisions. *Delano Farms, Co. v. California Table Grape Commission*, __ F.3d ___, 2011 WL 3689249 (Fed. Cir. 2011). *See also* Gregory C. Sisk, *Litigation With The Federal Government*, 4th ed., § 3.22 (American Law Institute 2006).

In the field of intellectual property respecting patents and trademarks, this principle is specifically enabled in two statutes -- 35 U.S.C. § 145, entitled "Civil action to obtain patent", and 15 U.S.C. § 1071(b), entitled "Civil action; persons entitled to; jurisdiction of court; status of Director; procedure," respectively.[3] The importance of the right of civil action under these organic statutes as one of the two mutually exclusive avenues of judicial recourse for those adversely affected by rulings of the Patent and Trademark Office ("PTO" or "Agency") has long been recognized and cannot be disputed.

At the interface between Article III court jurisdiction and the activities of government agencies, the word "review" connotes a type of judicial recourse which in

---

3. The wordings in 35 U.S.C. § 145 and 15 U.S.C. § 1071(b)(1) are essentially the same with respect to providing a remedy by "civil action", and the two statutes may therefore be read *in pari materia* in the present context. The Federal Circuit's en banc decision in respect to 35 U.S.C. § 145 is consistent with the interpretation of 15 U.S.C. § 1071(b)(1) in other circuits. *See* pp. 8-9 in "Brief of Amicus Curiae American Intellectual Property Law Association in Support of Neither Party" filed April 9, 2010 in the Federal Circuit en banc rehearing.

one of its aspects entails a process by which a court of appellate jurisdiction like the Federal Circuit in an appeal under 35 USC § 141, entitled "Appeal to the Court of Appeals for Federal Circuit", or a court of original jurisdiction, like the D.C. federal district court in a § 145 action sounding in equity under the APA at 5 U.S.C. § 702 and § 706(2)(F), examines ("reviews") the predicates in the administrative record of an agency's decision on each issue. The absence of the word "review" from § 145 stands in contrast to 35 U.S.C. § 144 which expressly cabins the scope of Federal Circuit jurisdiction over decisions of the PTO to the "review" of the administrative record in the Agency. If a civil action is based solely on such a record, then the court can remand (set aside) the Agency's decision on a given issue essential to the ultimate outcome if the Agency's fact-findings thereon are not supported by evidence 'substantial' enough to enable a reasonable observer to infer a factual conclusion required to decide the issue. 5 U.S.C. § 706(2)(E). Also, the court can reverse the decision if the Agency's conclusion(s) of law flowing from a substantial evidentiary record are incorrect ("erroneous"). 5 U.S.C. § 706(2)(A).

On the other hand, *because the enabling statute,* 35 U.S.C § 145, *authorizes* a "civil action" in Federal district court to "adjudicate" the Agency's decisions, and if the parties introduce further evidence in such action, then the district court does more than simply "review" the administrative record. Rather, the court *adjudicates* the factual issues, i.e., in a "de novo" trial proceeding at a level of judicial scrutiny that accords no deference – i.e., does not accept at face value -- the administrative finding(s) of fact underlying the agency's decision. In doing

so, the court takes a "hard look" at the agency's findings based on the administrative record supplemented with non-cumulative new evidence and/or different evidentiary modalities pertinent to disputed question(s) of fact on each issue, as though the agency had never addressed any of the evidence. *Morsemere Sav. & Loan Ass'n v. Marston*, 500 F. Supp. 1253, 1256-7 (D.N.J. 1980) (explaining the types of judicial review of agency decisions); *Chandler v. Roudebush*, 425 U.S. 840, 845-846 (1976) (discussing trial de novo under the Civil Rights Act); *Newton County Wildlife Ass'n v. Rogers*, 141 F.3d 803, 808 (8th Cir. 1998) (discussing citizen-suit provisions of the Endangered Species Act and the Clean Water Act). The decision of the Agency will not be overturned unless the new evidence introduced, considered, and weighed in conjunction with the administrative record persuades the court that the Agency erred.

A civil action under 35 U.S.C. § 145 is a lawsuit against the PTO in the person of the "Director" [of the Agency] "in the United States District Court for the District of Columbia." Unlike a direct appeal to the Federal Circuit under 35 U.S.C. § 141, a civil action under § 145 in which additional evidence is introduced is nothing at all like an appeal to a court of appellate jurisdiction that merely "reviews" judgments of a lower tribunal on a fixed record. Rather, § 145 provides a recourse to a specific federal district court, having original jurisdiction, in a proceeding that is adjudicatory in nature, aimed at a trial of the issues that were decided by the Agency. It is axiomatic that in absence of any legal authority to the contrary – of which there is none here -- the proceedings and the treatment of evidence in a § 145 action are governed by the *Federal*

Rules of Civil Procedure[4] and the *Federal Rules of Evidence*.[5] Thus, in order to avoid redundancy with § 141, one must read § 145 as authorizing the taking of additional evidence into account, which may be adduced by either or both parties, i.e., by the defendant PTO as well as by the plaintiff patent-applicant, by court-specific discovery mechanisms such as third-party subpoenas, or which could have been presented at the administrative stage, such as additional prior art which the PTO did not site.

That the named defendant in a § 145 civil action is the head of the PTO who is being sued in an official capacity,

---

4. In particular, Fed.R.Civ.P. 1 states in relevant part: "*These rules govern the procedure in all civil actions and proceedings in United States district courts . . . .*" In light of Fed.R.Civ.P. 4(i)(2), "civil actions" include suits against federal agencies.

5. In particular, Fed.R.Evid. 101 ("Scope") states in pertinent part: "*These rules govern proceedings in the courts of the United States . . . and before United States magistrate judges to the extent and with the exceptions stated in rule 1101.*" (Emphasis added). Fed.R.Evid. 1101 ("Applicability of Rules") states in pertinent part: *(a) Courts and judges. These rules apply to the United States district courts, . . . United States courts of appeals and to . . . United States magistrate judges, in these actions, cases, and proceedings and to the extent herein after set forth . . . (e) Rules applicable in part. In the following proceedings, these rules apply to the extent that matters of evidence are not provided for in the statutes that govern procedures therein or in other rules prescribed by the Supreme Court pursuant to statutory authority: . . . review of agency actions when the facts are subject to trial de novo under section 706(2)(F) of title 5, United States Code; . . .* (Emphasis added). In its "Notes to Subdivision (e)" on the 1972 Proposed Rules, the Committee states:

> "[the] rules of evidence are applicable to the proceedings enumerated in this subdivision . . .".

and that the action seeks judicial recourse from the final decision of an administrative agency, do not differentiate such lawsuits from other types of civil action insofar as the question now before this Court is concerned. As this Court held in *Federal Housing Administration, Region 4 v. Burr*, 309 U.S. 242, 245 (1940), "[w]hen Congress launched a governmental agency into the commercial world and endowed it with authority to 'sue or be sued', that agency is not less amenable to judicial process than a private enterprise under like circumstances would be." The question then is: whether there is any basis, in a § 145 action, for restricting the admission of additional evidence proffered by either party (separate and apart from the weight to be accorded to it) when such evidence is relevant under Fed. R. Evid. 401 to the issue(s) decided by the BPAI, admissible under Fed. R. Evid. 402, and not excludable under Fed. R. Evid. 403? The NYIPLA respectfully submits that the answer is no.[6]

It is believed that this Court, like the Federal Circuit and its predecessor, the Court of Customs and Patent Appeals, "has [never] squarely addressed the issue of exactly what standard governs district courts in ruling on the admissibility of evidence in a § 145 action that was withheld during [prosecution] in the PTO." *Hyatt v. Doll*, 576 F.3d 1246, 1259-60, 1269-70 (Fed. Cir. 2009) (panel decision); *Hyatt v. Kappos*, 625 F.3d 1320, 1322 (Fed.

6. An interesting "what if" would be the situation where the examiner's rejection of a Government-owned patent application or a patent in an ex parte reexamination is affirmed by the BPAI. Since nothing in § 145 or § 306 respectively, precludes a civil action by such an applicant or patent owner against the PTO, quaere whether the government would be as enthusiastic about its present position if the shoe were on the other foot?

Cir. 2010) (decision in rehearing en banc).[7] By granting certiorari, the Court can now definitively answer the question.[8]

In particular, the Court is urged to consider and clarify the admissibility standard(s) to be applied by the district court in § 145 actions involving newly submitted evidence when:

(i) the evidence was either unavailable to or unknown by the patent applicant during the proceedings in the PTO as in *Takeda, supra*, and in *Globe Union v. Chicago Tel. Supply Co.*, 103 F.2d 722, 288 (7th Cir. 1939), or

(ii) the evidence was available to or known by the applicant during the PTO proceedings, but the Agency lacked adequate means, resources, and/or procedures for considering such evidence (*e.g.*, oral testimony and

---

7. Some courts have held that evidence withheld from the PTO due to fraud, bad faith, or gross negligence, may be excluded in a district court civil action. *See DeSeversky v. Brenner*, 424 F.2d 857, 858 n.5 (D.C. Cir. 1970); *California Research Corp. v. Ladd*, 356 F.2d 813, 821 n.18 (D.C. Cir. 1966); *Monsanto Co. v. Kamp*, 269 F. Supp. 818, 822 (D.D.C. 1967); and *Killian v. Watson*, 121 U.S.P.Q. 507, 507 (D.D.C. 1958). However, none of those holdings is binding precedent on this Court or on the Federal Circuit. Hence, the present appeal presents an opportunity for this Court to establish such precedent.

8. In *Takeda Pharmaceutical Co. v. Dudas*, 511 F.Supp. 2d 81 (D.D.C. 2007), *vacated and remanded*, 561 F.3d 1372 (Fed. Cir. 2009), the district court allowed the proffer of evidence newly uncovered in a civil action under § 306 for district-court adjudication of the PTO's decision adverse to the patent owner in an ex parte patent reexamination. However, on appeal, the Federal Circuit did not reach the issue now before this Court.

cross-examination) as in *Minnesota Mining & Mfg. Co. v. Carborundum*, 155 F.2d 746 (3rd Cir. 1946), or

(iii) the applicant was negligent in failing to present evidence to the PTO which could have considered it during the administrative proceeding as in *California Research Corp. v. Ladd*, 356 F.2d 813, 820 n. 18 (D.C. Cir. 1966); *DeSeversky v. Brenner*, 424 F.2d 857, 858 n. 5 (D.C. Cir. 1970), or

(iv) the applicant knew of or had access to the newly proffered evidence during the proceeding before the Agency, but either willfully or inexplicably failed to submit it, as was deemed to be the case, for example, in *Barrett Co. v. Koppers Co.*, 22 F.2d 395 (3d Cir. 1927), or in *Killian v. Watson*, 121 USPQ 507 (D.D.C. 1958).

II. SUMMARY OF ARGUMENT

The ability to introduce new evidence in district court in furtherance of a position taken by the profferor in traversing the PTO's fact-finding(s) on an issue of contention before the Agency is the hallmark of civil actions under 35 U.S.C§ 145. That enables district-court adjudication -- which the plaintiff must pay for entirely -- of the full merits of PTO decisions adverse to patent applicants based on evidence both in and outside the administrative record with no express restrictions on its admissibility. It is from this aspect that civil actions under § 145, as a distinct alternative to direct appellate review under § 141, derive much of their worth for inventors, companies, and many industries, as well as universities that create, develop, value, and rely upon their intellectual property portfolios to augment and protect their technology assets.

Direct appellate review in the Federal Circuit, characterized by deference to the Agency's fact-findings (if based on a "substantial" evidentiary record), may often be sufficient to give the aggrieved party its proverbial 'right to a "day in court".' Nevertheless, an across-the-board exclusionary rule that deprives all patent applicants of the full, unfettered right to introduce evidence subject only to the *Federal Rules of Evidence* through district-court adjudication and trial under the *Federal Rules of Civil Procedure* in effect leaves direct appellate review as their only effective recourse from erroneous PTO decisions. Such a rule does nothing to encourage, and indeed can only discourage investments in the obtaining and development of patent assets. It is not only unfair but also unworkable for those who, in order to secure judicial disposition of their cases on the full factual merits, and of which the statute obligates them to pay the entire cost, may need to rely on additional evidence that was available or known to the profferor during the administrative stage of the proceeding but for whatever reason was not presented at that time in one form or another to the PTO.

Because the district court possesses what historically has been recognized as equity jurisdiction over the parties appearing before it under § 145, there is a need and an opportunity presented by the facts in this case to definitively establish that parties in § 145 civil actions (and correspondingly in civil actions under 15 U.S.C. § 1071(b) relating to trademark registration applications[9]) are no less entitled than parties in other non-jury litigations to submit evidence for the court to consider in deciding cases, subject only to the strictures on admissibility based

9. *See supra* note 3.

on relevancy; probity; unfair prejudice; competency; credibility; fairness; and duplicativeness as are imposed by the *Federal Rules of Evidence*[10] and the *Federal Rules of Civil Procedure*. The Federal Circuit's en banc majority opinion correctly rejected the special, restrictive, heightened standard of evidence-admissibility announced by the district court and the Federal Circuit panel majority, and urged by the present Petitioner.

For the reasons set forth below, *amicus* NYIPLA urges this Court to resolve the issue herein presented in favor of a *Federal Rules of Evidence* standard allowing the proffer of evidence in § 145 civil actions governed by the *Federal Rules of Civil Procedure*, unfettered by the fact that the evidence was available, but for whatever reason was not made of record in the proceedings before the PTO. That standard enables under § 145, and the APA does not preclude, district court adjudication of the material issues decided by the PTO on the basis of the record that was before the Agency, coupled with any new evidence (i) relevant to those issues; (ii) that might have been -- but for whatever reason was not -- presented during the administrative proceedings; and (iii) without inquiry or concern as to why such evidence was not previously presented.

---

10. Fed. R. Evid. 102 ("These rules shall be construed to secure fairness in administration, elimination of unjustifiable expense and delay, . . ."); Fed. R. Evid. 403 ("Although relevant, evidence may be excluded if its probative value is substantially outweighed by the danger of unfair prejudice, . . . or by considerations of undue delay, waste of time, . . ."). (Emphasis added).

III. ARGUMENT

POINT I — The APA Does Not Conflict With the Statutory Enablement of Article III Court Adjudication of Government-Agency Actions Wherein the Admission of New Evidence is Governed By the Federal Rules of Evidence

Dickinson v. Zurko, 527 U.S. 150 (1999), held that, direct appeals to the Federal Circuit under 35 U.S.C. § 141 must be decided on the basis of and subject to, (i) the APA's deferential, "substantial evidence" standard of review of the BPAI's fact-findings in the administrative record, 35 U.S.C. § 144, and (ii) a non-deferential, *de novo* standard of review of the BPAI's conclusions of law. Thus, if the court finds that the PTO's decision is supported by substantial evidence whereby the findings of fact are to be deemed conclusive, and if the PTO's conclusions of law are not erroneous, then the decision should be affirmed.

Mazzari v. Rogan, 323 F.3d 1000 (Fed. Cir. 2003), held that, in § 145 civil actions in district court, if the only evidence presented by either party was already made of record in the PTO, then the court must examine the Agency's decision under the same standard that the Federal Circuit would have applied if a direct appeal had been taken under §141. *Id.* at 1004-5. In such case, insofar as the likely outcome is concerned, there is no practical difference between the two routes of judicial treatment (aside from the obligation of the plaintiff to pay all the expenses of a civil action as required by the last sentence of § 145, and the appealability to the Federal Circuit from the judgment of the district court per 28 U.S.C. § 1295(a)(1) and § 1295(a)(4)(C)).

There is a difference, however, when either party – be it the plaintiff or the PTO – presents additional evidence (or presents prior evidence in a different modality, *e.g.*, live testimony, etc.) to the district court (which is not possible, of course, on direct appeal to the Federal Circuit) relevant to material fact-issues, i.e., "that might affect the outcome of the suit under governing law." *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 248 (1986). In such case, the "substantial evidence" standard of review of agency fact-findings does not apply; rather, the district court, whether in deciding a dispositive motion (as was the case here) or at trial, considers and weighs all of the parties' admissible evidence relevant to the issues of contention in the case and without deference to the manner by which the BPAI arrived at its factual conclusions. In other words, such review is de novo both as to the facts as well as the conclusions of law (albeit not the issues which usually remain fixed as they were at the Agency level). *DeSeversky v. Brenner*, 424 F.2d 857, 858 (D.C. Cir. 1970); *In re Watts*, 354 F.3d 363, 367 (Fed. Cir. 2004)). Thus, if new evidence is admitted, "the district court takes on the roll of fact-finder and may need to make factual findings." *Mazzari*, 323 F.2d at 1004.

Under *Morgan v. Daniels*, 153 U.S. 120 (1894) and *Barrett Co. v. Coppers, Co.* 22 Fed.2d 395 (3d cir. 1927), the trial of a bill in equity must be heard upon all competent evidence adduced, and upon the entire merits of the case, and not merely de novo *sub modo* by ignoring the administrative record. The operative language in § 145 confirms this principle:

> An applicant dissatisfied with the decision of the Board of Patent Appeals and Interferences

> . . . may, . . . *have remedy by civil action* against the Director in the United States District Court for the District of Columbia . . . . The court may *adjudge* that such applicant is entitled to receive a patent for his invention, as specified in any of his claims involved in the decision of the Board of Patent Appeals and Interferences, *as the facts in the case may appear* and such *adjudication* shall authorize the Director to issue the patent . . .

35 USC § 145 (Emphasis added).

But neither *Morgan* nor *Barrett* involved civil actions seeking the adjudication of PTO decisions in proceedings in the examination of patent applications; rather, they involved priority contests, between competing inventors (i.e., interferences).

Most PTO proceedings are either "contested" or "non-contested." A "contested" case is defined in the PTO's own rules as a proceeding that does not entail an administrative appeal to the BPAI under 35 U.S.C. § 134 from an examiner's action. *See* 37 C.F.R. § 41.2 (¶ 5, first sentence); §§ 41.100 – 41.158. Rather, the PTO's decision emanates from a contest between adversaries conducted under the direct auspices of the BPAI. Patent interferences under 35 U.S.C. § 135 are contested cases. *See* 37 C.F.R. §§ 41.200-208, esp. § 41.200(a). Conversely, original and reissue patent application proceedings under 35 U.S.C. §§ 131-133, § 251, and § 134(a) are non-contested cases that begin with an examiner's action and then proceed to the BPAI for an administrative ruling on an examiner's final rejection.

Though seldom dwelt upon in discourse outside the PTO, the dichotomy between non-contested and contested cases has profound implications in the present context – both substantively and procedurally, and for this reason neither *Morgan* nor *Barrett* are apposite. For one thing, judicial recourse from PTO decisions in non-contested cases is by direct appeal to the Federal Circuit under § 141 or by adjudication through civil against the Agency, under § 145. On the other hand, judicial recourse from PTO decisions in contested cases is by direct appeal to the Federal Circuit under § 141 or by civil action between the disputants under § 146 in which the PTO is usually not a party.[11] Moreover, while the U.S. district court has broad subpoena power under Fed. R. Civ. P. 45 to summon witnesses and documents in § 145 civil actions as in other court litigations, under 35 U.S.C. § 24 the power of the court to issue subpoenas in PTO proceedings expressly applies only to contested cases. Hence, subpoenas are not

---

11. 35 U.S.C. § 146 provides in pertinent part:

§ 146 Civil Action in Case of Interference

> "Any party to an interference dissatisfied with the decision of the Board of Patent Appeals and Interferences on the interference, may have remedy by civil action, ... In such suits the record in the Patent and Trademark Office shall be admitted on motion of either party upon the terms and conditions as to costs, expenses, and the further cross-examination of the witnesses as the court imposes, *without prejudice to the right of the parties to take further testimony*. The testimony and exhibits of the record in the Patent and Trademark Office when admitted shall have the same effect as if originally taken and produced in the suit." (Emphasis added.)

available in the administrative stage of patent application proceedings. In a broader sense, patent application proceedings require an *examination* by the PTO to determine by its own analysis if the granting of a patent on an application is warranted under the law, and in which the burden of persuading the Agency shifts from the examiner to the applicant if the examiner is able to make out a *prima facie* case of unpatentability. In contrast, a contested case is in the nature of an Agency-*adjudicated, revocation/opposition* proceeding in the BPAI between adverse-parties-in-interest, wherein the opposer (e.g., a junior party in an interference) must persuade the PTO that a patent claim is undeserved, and the PTO ultimately decides whether that party has met its burden of persuasion which does not shift at any time during the proceeding.

There are reasons why a patent applicant may choose not to, or cannot, provide the PTO with all of the available evidence that supports his or her case. But regardless of what they are, the district court in a § 145 action should not be distracted and burdened with the task of divining them in a hearing-within-a-hearing initiated by an objection to its admissibility on those grounds. There is no statute, rule, or policy that would – or should – require the district court to act as gatekeeper beyond what is required by the *Federal Rules of Evidence*, and whose decision whether or not to exclude or admit evidence would depend on the facts of each case that are unrelated to the substantive issue(s). In order that § 145 can serve its purpose as a meaningful – and at times necessary – alternative to a § 141 appeal, a party – whether it be the patent applicant or the PTO – should have the same right to prove its case in conformity with the *Federal Rules of Evidence* as do the

parties in any other civil action under the *Federal Rules of Civil Procedure.*[12]

The provision in Fed. R. Civ. P. 26(a)(1)(B)(i) exempting parties in district court actions seeking review on an administrative record from the initial disclosure requirements of Fed. R. Civ. P. 26(a)(1)(A) do not apply to civil actions where a party intends to rely on additional evidence at trial. *Invitrogen Corp. v. President and Fellows of Harvard College*, 2007 U.S. Dist. LEXIS 74282 (S.D.Cal. 2007). ("The Advisory Committee Notes to the 2000 Amendments to Rule 26, state that this exemption 'should not apply to a proceeding in a form that commonly permits admission of new evidence to supplement the record.' The present action, filed under *35 U.S.C. § 146*, does not fall within this exemption.") The initial disclosure of such evidence does not require that any reason(s) be given why the evidence was not adduced during the administrative proceeding, thus signaling that the district court will admit and consider such evidence, subject to whatever weight the court should choose to give it.

Citing *Citizens to Preserve Overton Park v.Volpe*, 401 U.S.402, 414-420 (1971), the dissenting judges in the en banc decision opined that § 145 actions should not depart from settled administrative law under 5 U.S.C. § 706 in that new evidence may be excluded by the district court only if it could have been introduced and considered by the agency during the administrative proceeding, for example, when agency procedures are inadequate to do

12. The fact that the Government's motion for summary judgment in the § 145 civil action was grounded on Fed. R. Civ. P. 56 suggests that the Government is correct not to dispute the point.

so (e.g., direct and cross-examination of live witnesses, inter partes tests and replications, and the like). They were concerned that the majority opinion would lead to the deliberate withholding of evidence from the PTO by patent applicants seeking "a more hospitable forum" in the district court where non-expert judges would be more likely to accept it on face value. But that is a fallacy. In order to buttress it, the dissenting judges took it upon themselves to try and take judicial notice of what they assert to be the superior technical and patent law expertise of the PTO Corps of Examiners and the BPAI compared to the district court. 625 F.3d at 1342-44. No mention was made, however, of the ability of either or both parties in a § 145 civil action to present the testimony of expert witnesses under Fed. R. Evid. 702 as well as the ability of the court itself under Fed. R. Evid. 706 to appoint its own expert(s) – all at the patent applicant's expense as required by the last sentence in § 145 ("All expenses of the proceeding shall be paid by the applicant"). If anything, this shows that plaintiff-applicants do not embark on such proceedings lightly – which accounts for the relatively infrequent resort to § 145 actions in comparison to § 141 appeals.

The commencement of a § 145 action does not signal the "termination" of the application proceeding. Rather, it continues the prosecution of the application, and the court proceedings will become part of the prosecution record. The overall process is not seamless since the principle of administrative exhaustion of the applicant's recourse against the Agency's rejection of the application requires that the case be decided on the *issue(s)* by the BPAI before the district court can acquire jurisdiction. After that, the proceeding lies beyond the reach of the PTO's

rulemaking authority which is limited by 35 U.S.C. § 2(b)(2) to "establish[ing] regulations, not inconsistent with law, which . . . shall govern proceedings in the Office, . . ." The PTO recognizes this in its own official pronouncements in the *Manual of Patent Examining Procedure* (M.P.E.P.) at § 1216VI (8th ed., rev. 8, July 2010) ("During judicial review, the involved application or reexamination is not under the jurisdiction of the examiner or the Board, unless remanded to the U.S. Patent and Trademark Office by the court. Any amendment can be admitted only under the provisions of. . . ."). That is not to say that the PTO hasn't tried to extend its influence into the judicial process and shape PTO stakeholders' understanding of the law by ultra vires pronouncements on the issue before this Court which merits no deference under *Chevron, U.S.A., Inc. v. National Resources Defense Council, Inc.*, 467 U.S. 837 (1984). *See M.P.E.P.* § 1260.02 ("In an action under 35 U.S.C. § 145, the plaintiff may introduce evidence not previously presented to the U.S. Patent and Trademark Office. However, new evidence is not admissible in district court where it was available to the parties but was withheld from the U.S. Patent and Trademark Office as a result of fraud, bad faith, or gross negligence".) citing the cases mentioned herein at *supra* note 7.

While the language in § 145 is not as explicit as that in § 146 which explicitly allows parties to "take further testimony," i.e., to seek to admit additional evidence,[13] § 145 nevertheless cannot be validly interpreted or understood in any way other than to authorize parties (be it a plaintiff patent applicant or the defendant PTO) to proffer new evidence for the trial court to consider

13. *See supra* note 11.

and weigh pursuant to the *Federal Rules of Evidence.* Logic requires this. After all, withholding evidence from the PTO that would support the allowance of a patent application is the antithesis of inequitable conduct in withholding prejudicial information from the PTO contra to 37 C.F.R. § 1.56 in order to avoid the negative impact on the examination of the application that would be adverse to the applicant. It would be counterintuitive to think that an applicant – particularly when represented (as is usually the case) by and with the sage advice and judgment of a patent lawyer or agent licensed by the PTO to represent others before the Agency[14] – to knowingly refuse to respond to an examiner's rejection by not supplying requested information, or to intentionally suppress or negligently to withhold from the PTO non-redundant, non-cumulative evidence that supports the merits of the application so as to avoid building an administrative record that might persuade the BPAI to rule in the applicant's favor. Doing so in order to present it later on in a costly civil action in which the applicant (as plaintiff) would be obligated to pay all the expenses – including the defendant PTO's expenses – makes no sense. It simply defies credulity and it is certainly not condusive to "gamesmanship". And the boundary condition that drives home the point is when the evidence presented to the district court was simply not available or did not exist when the case was pending before the BPAI.

---

14. Such may not have been the case here. Respondent is an electrical engineer, businessman, and registered patent agent who prosecuted his present application *pro se* in the PTO. *See* ¶¶ 1-6 Respondent's evidentiary declaration filed in district court, a copy of which is Appendix H to the Government's petition for certiorari.

As a logical subset of the principle that civil actions under § 145 are subject to and are conducted in accordance with the *Federal Rules of Civil Procedure*, where there is a court proceeding involving the validity of an issued patent having a related pending application which is involved in a § 145 action, the court in the § 145 action has the discretion under Fed. R. Civ. P. 24(b)(1)(B) to order the joinder of the party challenging the patent in the validity litigation, in situations where both actions share a common question of law or fact (e.g., patentability in view of the prior art). *Moore's Federal Practice*, 3d ed., § 24.10 (2008). The same applies to a patent involved in a civil action under § 306 for de novo review of the BPAI's adverse decision in an ex parte reexamination requested by any party, including the patent owner or defendant in the enforcement action. In either of these scenarios (i.e., patent applications and patents in ex parte reexaminations) the intervener would have the right, not only to make legal arguments on issues already presented to the court in the civil action, but also to introduce evidence (e.g., published prior art) in support of those arguments that had come to light in the patent validity litigation but which was not of record in the PTO proceedings involving the related patent application(s). Therefore, it would be inconsistent with the even-handed interpretation of the operative statutes and rules, to preclude the plaintiff in a § 145 action from introducing evidence that for whatever reason was not made of record in the PTO, while permitting an intervener to do so.

POINT II — The Patent Act at 35 U.S.C. § 145 Enables a Full Trial De Novo in a District Court for Adjudication of PTO Decisions in Other Settings

The Petitioner has asserted that a district court should exclude evidence on grounds referred to in this case and in *Barrett Co. v. Koppers Co.*, 22 F.2d 395 (3d Cir. 1927). *Hyatt v. Doll*, 576 F.3d at 1275 n.31. However, if the Federal Circuit's en banc decision is not affirmed, then the antecedent panel majority's broad holding that "evidence owed, requested, and willfully withheld from the PTO" may be excluded from a subsequent § 145 action involving patent applications, *Id.* at 1278, will apply by analogy to actions under 35 U.S.C. § 306/§ 145 seeking adjudication of PTO rejections in ex parte reexaminations of issued patents.

It is no secret that civil actions in relation to patent applications under 35 U.S.C. § 145 and in relation to ex parte patent reexaminations under 35 U.S.C. § 306,[15] whose administrative procedures are similar under 35 U.S.C. § 305, are odious to the PTO. This is evident from

---

15. 35 U.S.C. § 306 reads as follows:

§ 306. Appeal.

> The patent owner involved in a reexamination proceeding under this chapter may appeal under the provisions of section 134 of this title, and may seek court review under the provisions of sections 141 to 145 of this title, with respect to any decision adverse to the patentability of any original or proposed amended or new claim of the patent. [Emphasis added].

identical provisions in both the Senate- and House-passed versions of the *America Invents Act*, S.23 and H.R. 1249. In particular, SEC. 5 (h)(2)(A) of S.23 and SEC. 6(h)(2)(A) of H.R. 1249 would abolish district-court jurisdiction over PTO decisions in ex parte reexaminations – a right that has existed since the inception of ex parte reexamination in 1980 – by means of a seemingly simple amendment of § 306:

> The patent owner involved in a reexamination proceeding under this chapter may . . . seek court review under the provisions of sections 141 to 144 ~~145~~ of this title . . . .

SEC. 6(c)(1) of S.23 and SEC. 7(c)(1) of H.R. 1249 would rewrite 35 U.S.C. § 141 in four parts, (a) - (d). Part (b) of § 141 would read as follows:

> (b) REEXAMINATIONS.—A patent owner who is dissatisfied with the final decision in an appeal of a reexamination to the Patent Trial and Appeal Board under section 134(b) may appeal the Board's decision only to the United States Court of Appeals for the Federal Circuit.

See Charles E. Miller and Daniel P. Archibald, *The "America Invents Act" and its Restriction on Judicial Recourse*, 39 AIPLA Q. J. 397 (Summer 2011).

The concern now is that the present legislation foreshadows the further enlargement of the PTO's decision-making power and influence over the patent system at the expense of the Judiciary, by the eventual

undoing of trial-court jurisdiction over original and reissue patent application proceedings.[16] *Id.*

Because of the aforementioned procedural similarities between the prosecution of patent applications and that of ex parte patent reexaminations, particularly with respect to judicial recourse from BPAI decisions, this Court's decision will have implications for civil actions under 35 U.S.C. § 306 which otherwise will continue to enable district-court trial de novo jurisdiction over PTO decisions in ex parte reexaminations until such time as the *America Invents Act* is signed into law. Given the increasing resort to post-patent-grant review in the PTO as an adjunct to patent validity litigation in the courts, it is important that the law governing district-court trial de novo jurisdiction over PTO examination proceedings remain fully available to patent owners in all non-contested cases.[17]

---

16. The aforementioned aversion of the PTO to civil actions against it in the context of patent application proceedings was discussed by the dissent from the Federal Circuit's en banc decision, 625 F.3d at 1349-52. Other rights of adjudication of PTO decisions that may soon appear on the legislative horizon can be found in 35 U.S.C. § 32 (suspension or exclusion of persons from practicing before the PTO); 35 U.S.C. § 154(b)(4) (final PTO determinations of patent term adjustments); and in the aforementioned 15 U.S.C. § 1071(b) (PTO Trademark, Trial & Appeal Board decisions affirming examiners' rejections of trademark registration and renewal applications).

17. The PTO has argued in other settings, and its own erroneous interpretive rulemaking presupposes, that 35 U.S.C. § 141, third sentence, and § 306 as currently written are to be read *in pari materia* such that § 141 somehow trumps § 306, whereby district court jurisdiction over the Agency's decisions in ex parte

IV. CONCLUSION

Amicus curiae NYIPLA respectfully urges the Court, upon considering all the submissions in this case, to hold that 35 U.S.C. § 145 enables trial de novo in Federal district court of BPAI decisions affirming examiners' rejections of patent applications, wherein the admissibility of newly-proffered evidence is determined solely in accordance with the *Federal Rules of Civil Procedure* and the *Federal Rules of Evidence*, with no judicially imposed obligation on patent applicants to present such

---

reexaminations requested post-November 28, 1999 was eliminated by the *American Inventors Protection Act* of 1999 and the *21st Century Department of Justice Appropriations Authorization Act* of 2002, and that the current legislation merely serves as a clarification of the PTO's view of the present state of affairs. But such rulemaking and the PTO's supporting argument are grounded on the false premise that the 1999 and 2002 legislative enactments had anything to do with judicial review in *ex parte* reexaminations, and are refuted in a recently-published analysis. *See* Charles E. Miller and Daniel P. Archibald, *Interpretive Agency-Rulemaking vs. Statutory District Court Review Jurisdiction in Ex Parte Patent Reexaminations*, 92 J. Pat. & Trademark Off. Soc'y, 498-535 (2011). In any event, the PTO's position is being tested in the courts in a number of pending § 306 civil actions. See *Teles A.G. v. Kappos*, Civil Action 1:11-cv-0476 (D.D.C.); *Dome Patent L.P. v. Kappos*, Civil Action 07-cv-1695 (D.D.C.); *Tse v. Kappos*, Civil Action 1:11-cv-1127 (D.D.C.); *Bally Gaming, Inc. v. Kappos*, Civil Action 1:10-cv-1906 (D.D.C.); and *Power Integrations, Inc. v. Kappos*, Civil Action 1:11-cv-1254. The issue of subject matter jurisdiction raised by Section 145/306 cases will be mooted if the *American Invents Act* becomes law. Yet, if the PTO's interpretation of existing law is already correct, then why would the Agency try to vindicate it through legislation? It is believed the answer lies in the PTO's desire to forestall adverse judicial interpretation by pressing its views in Congress.

evidence to the PTO in the administrative stage. To rule otherwise would stymie the use of § 145 in providing a meaningful and necessary *adjudicatory* alternative to direct *appellate* review under 35 U.S.C. § 141 based solely on the PTO's evidentiary record as required by § 144.

Respectfully submitted,

JOHN M. HINTZ
Co-Chair, Committee on Amicus Briefs
NEW YORK INTELLECTUAL PROPERTY LAW ASSOCIATION
c/o CHADBOURNE & PARKE LLP
30 Rockefeller Plaza
New York, NY 10112
(212) 408-1036

DAVID F. RYAN
Co-Chair, Committee on Amicus Briefs
NEW YORK INTELLECTUAL PROPERTY LAW ASSOCIATION
1214 Albany Post Road
Croton-on-Hudson, NY 10520
(914) 271-2225

CHARLES E. MILLER
Counsel of Record
DICKSTEIN SHAPIRO LLP
1633 Broadway
New York, NY 10019-6708
(212) 277-6500
millercharles@dicksteinshapiro.com

THERESA M. GILLIS
President
NEW YORK INTELLECTUAL PROPERTY LAW ASSOCIATION
c/o MAYER BROWN LLP
1675 Broadway
New York, NY 10019-5820
(212) 506-2500

September 6, 2011

AMICUS CURIAE BRIEF

RECORD
AND
BRIEFS

No. 10-1219

In the
Supreme Court of the United States

DAVID J. KAPPOS, UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR, UNITED STATES PATENT AND TRADEMARK OFFICE,
Petitioner,

v.

GILBERT P. HYATT,
Respondent.

On Writ of Certiorari to the United States Court of Appeals for the Federal Circuit

BRIEF OF VERIZON COMMUNICATIONS INC., GOOGLE INC., HEWLETT-PACKARD CO., AND HTC CORP. AS *AMICI CURIAE* IN SUPPORT OF NEITHER PARTY

JOHN THORNE
GAIL F. LEVINE
VERIZON
COMMUNICATIONS INC.
1320 North Courthouse Road
Arlington, VA 22201
(703) 351-3900
Counsel for Verizon Communications Inc.

DARYL JOSEFFER
Counsel of Record
ADAM CONRAD
KING & SPALDING LLP
1700 Pennsylvania Ave., NW
Washington, DC 20006
(202) 737-0500
djoseffer@kslaw.com
Counsel for Amici Curiae

September 6, 2011

Library of Congress
Law Library

Additional counsel:

PAUL H. ROEDER HEWLETT-PACKARD CO. 3000 Hanover Street Palo Alto, CA 94304-1112 (650) 857-5459 *Counsel for Hewlett-Packard Co.*	

TABLE OF CONTENTS

TABLE OF AUTHORITIES iii

INTEREST OF *AMICI CURIAE* 1

INTRODUCTION AND SUMMARY OF ARGUMENT 1

ARGUMENT 4

I. THE ADEQUACY OF A WRITTEN DESCRIPTION PRESENTS A QUESTION OF LAW, NOT FACT 4

A. The Patent Specification Itself, As Opposed To Any External Materials, Must Provide A Full And Detailed Disclosure Of The Claimed Invention 4

B. The Adequacy Of A Written Description Is A Question Of Law. 6

1. The written-description requirement looks to the disclosure within the patent specification itself. 6

2. Construing the patent specification is a question of law. 8

II. RESPONDENT'S "NEW EVIDENCE" IS LEGAL ARGUMENT ON THIS QUESTION OF LAW, NOT "EVIDENCE" AT ALL. 16

III. THE CORRECT CLASSIFICATION OF THE WRITTEN-DESCRIPTION REQUIREMENT IS EXCEPTIONALLY IMPORTANT 17

A. The Question Is Properly Before This Court 17

B. The Question Is Exceptionally Important Throughout Patent Law. 18

1. Courts decide questions of law without deference to the PTO's issuance of a patent. 18

2. Judicial review of the adequacy of a written description is especially important. 23

CONCLUSION 26

TABLE OF AUTHORITIES

Page(s)

CASES

Addington v. Texas,
441 U.S. 418 (1979) 19-20

Am. Hoist & Derrick Co. v. Sowa & Sons, Inc.,
725 F.2d 1350 (Fed. Cir. 1984) 21

Anascape, Ltd. v. Nintendo of Am., Inc.,
601 F.3d 1333 (Fed. Cir. 2010) 12

Ariad Pharms., Inc. v. Eli Lilly & Co.,
598 F.3d 1336 (Fed. Cir. 2010) (en banc) ...passim

Battin v. Taggert,
58 U.S. (17 How.) 74 (1854) 14

Baumstimler v. Rankin,
677 F.2d 1061 (5th Cir. 1982) 21

Bilski v. Kappos,
130 S. Ct. 3218 (2010) 22

Bischoff v. Wethered,
76 U.S. (9 Wall.) 812 (1869) 15

Bonito Boats, Inc. v. Thunder Craft Boats, Inc.,
489 U.S. 141 (1989) 5

Branson Sch. Dist. RE82 v. Romer,
161 F.3d 619 (10th Cir. 1998) 20

Brown v. Huger,
62 U.S. (21 How.) 305 (1858) 8

Connell v. Sears, Roebuck & Co.,
722 F.2d 1542 (Fed. Cir. 1983) 21

Cybor Corp. v. FAS Techs., Inc.,
138 F.3d 1448 (Fed. Cir. 1998) (en banc) 9

Dual Mfg. & Eng'g, Inc. v. Burris Indus., Inc.,
619 F.2d 660 (7th Cir. 1980) (en banc)..... 20-21

Eon-Net LP v. Flagstar Bancorp,
__ F.3d __, 2011 WL 3211512 (Fed. Cir.
2011) 23

Evans v. Eaton,
20 U.S. (7 Wheat.) 356 (1822)..... 4, 5, 15

Exxon Research & Eng'g Co. v. United States,
265 F.3d 1371 (Fed. Cir. 2001) 11, 13

Festo Corp. v. Shoketsu Kinzoku Kogyo
Kabushiki Co.,
535 U.S. 722 (2002) 5

Forbes v. Barstow Stove Co.,
9 F. Cas. 395 (C.C. D. R.I. 1864) (No. 4923)..... 14

Gill v. Wells,
89 U.S. 1 (1874) 7

Grant v. Raymond,
31 U.S. (6 Pet.) 218 (1832) 4

In re Aoyama,
__ F.3d __, 2011 WL 3796243 (Fed. Cir. Aug. 29, 2011) 24

In re Ruschig,
379 F.2d 990 (C.C.P.A. 1967) 10, 11

In re Wertheim,
541 F.2d 257 (C.C.P.A. 1976) 11

In re Winship,
397 U.S. 358 (1970) 20

Int'l Longshoremen's Ass'n v. Davis,
476 U.S. 380 (1986) 17

Interactive Gift Exp., Inc. v. Compuserve Inc.,
256 F.3d 1323 (Fed. Cir. 2001) 18

KSR Int'l Co. v. Teleflex, Inc.,
550 U.S. 398 (2007) 22

Lear, Inc. v. Adkins,
395 U.S. 653 (1969) 22

Lotus Dev. Corp. v. Paperback Software Int'l,
740 F. Supp. 37 (D. Mass. 1990) 24

Mackay Radio & Telegraph Co. v. Radio Corp. of Am.,
306 U.S. 86 (1939) 7

Maritimes & Ne. Pipeline, LLC v. Echo Easement Corridor, LLC,
604 F.3d 44 (1st Cir. 2010) 8

Markman v. Westview Instruments, Inc.,
517 U.S. 370 (1996) ..... passim

Markman v. Westview Instruments, Inc.,
52 F.3d 967 (Fed. Cir. 1995) (en banc) 9

McDermott Int'l, Inc. v. Wilander,
498 U.S. 337 (1991) 18

Merrill v. Yeomans,
94 U.S. 568 (1876) 6

Mfg. Research Corp. v. Graybar Elec. Co.,
679 F.2d 1355 (11th Cir. 1982) 21

Microsoft Corp. v. i4i Ltd. P'ship,
131 S. Ct. 2238 (2011) ..... passim

Miles Labs., Inc. v. Shandon, Inc.,
997 F.2d 870 (Fed. Cir. 1993) 13

Newell Cos., Inc. v. Kenney Mfg. Co.,
864 F.2d 757 (Fed. Cir. 1989) 19

O'Reilly v. Morse,
56 U.S. (15 How.) 62 (1853) 6, 15

O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co., Ltd.,
521 F.3d 1351 (Fed. Cir. 2008) 22

Permutit Co. v. Graver Corp.,
284 U.S. 52 (1931) 7, 12, 15

Phillips v. AWH Corp.,
415 F.3d 1303 (Fed. Cir. 2005) (en banc) 5, 7, 9

Raytheon Co. v. Roper Corp.,
724 F.2d 951 (Fed. Cir. 1983) 11

Reese Exploration, Inc. v. Williams Natural Gas Co.,
983 F.2d 1514 (10th Cir. 1993) 8

Rempfer v. Sharfstein,
583 F.3d 860 (D.C. Cir. 2009) 16

Saturn Mfg., Inc. v. Williams Patent Crusher & Pulverizer Co.,
713 F.2d 1347 (8th Cir. 1983) 21

Schriber-Schroth Co. v. Cleveland Trust Co.,
305 U.S. 47 (1938) 5, 6, 7, 12, 15

Smoot v. Boise Cascade Corp.,
942 F.2d 1408 (9th Cir. 1991) 8

Spectralytics, Inc. v. Cordis Corp.,
Nos. 2009-1564, 2010-1004 (Fed. Cir. June 13, 2011) 21

SSIH Equip. S.A. v. ITC,
718 F.2d 365 (Fed. Cir. 1983) 19

Terran v. Kaplan,
109 F.3d 1428 (9th Cir. 1997) 8

United States v. Dubilier Condenser Corp.,
289 U.S. 178 (1933) 5

United States v. Farnham,
791 F.2d 331 (4th Cir. 1986) 20

United States v. Giacalone,
587 F.2d 5 (6th Cir. 1978) 20

United States v. Hausmann,
711 F.2d 615 (5th Cir. 1983) 20

United States v. Telectronics, Inc.,
857 F.2d 778 (Fed. Cir. 1988) 11-12

Warner-Jenkinson Co. v. Hilton Davis Chem. Co.,
520 U.S. 17 (1997) 20

Winans v. Denmead,
56 U.S. (15 How.) 330 (1853) 10, 15

Winans v. N.Y. & E.R. Co.,
62 U.S. (21 How.) 88 (1858) 8

Wood v. Underhill,
46 U.S. (5 How.) 1 (1847) 12, 14

Yee v. City of Escondido,
503 U.S. 519 (1992) 17-18

STATUTES

5 U.S.C. § 706 16

35 U.S.C. § 112 ..... 4, 9, 11, 13, 19

OTHER AUTHORITIES

A. Walker, Patent Laws (3d ed. 1895) 9

Adam B. Jaffe & Josh Lerner, Innovation and Its Discontents (2004) 21

AIPLA, Report of the Economic Survey 2011 22-23

Allen N. Littman, *The Jury's Role in Determining Key Issues in Patent Cases:* Markman, Hilton Davis, *and Beyond*, 37 IDEA 207 (1997) 15

Curtis, The Law of Patents (1873) 14

Dennis Crouch, *An Empirical Study of the Role of the Written Description Requirement in Patent Prosecution* (Univ. of Mo. Sch. of Law Legal Studies Research Paper No. 2010-06, 2010) 25

FTC, *The Evolving IP Marketplace: Aligning Patent Notice and Remedies with Competition* (2011) 23, 25

Jeffrey A. Lefstin, *The Formal Structure of Patent Law and the Limits of Enablement*, 23 Berkeley Tech. L.J. 1141 (2008) 15

Jesse S. Keene, *Fact or Fiction: Reexamining the Written Description Doctrine's Classification as a Question of Fact*, 18 Fed. Cir. B.J. 25 (2008) 15

Kimberly Moore, *Juries, Patent Cases, & a Lack of Transparency*, 39 Hous. L. Rev. 779 (2002) 21

Mark A. Lemley, *Rational Ignorance at the Patent Office*, 95 Nw. U. L. Rev. 1495 (2001) 21

Mark A. Lemley & Kimberly A. Moore, *Ending Abuse of Patent Continuations* (George Mason Univ. Sch. of Law, Law & Econ. Research Paper No. 03-52, 2003) 23

MPEP § 2163 25

Nathan Myhrvold, *Funding Eu[illegible]*, Harv. Bus. Rev., Mar. 2010 24

PTO, Supplementary Examination Guidelines for Determining Compliance With 35 U.S.C. § 112 and for Treatment of Related Issues in Patent Applications 7162 (Feb. 9, 2011) 26

R. Polk Wagner, *Understanding Patent-Quality Mechanisms*, 157 U. Pa. L. Rev. 2135 (2009) 25

Stephen Breyer, The Uneasy Case for Copyright: A Study of Copyright in Books, Photocopies, and Computer Programs, 84 Harv. L. Rev. 281 (1970) 24

INTEREST OF *AMICI CURIAE*[1]

Amici are innovative leaders in a wide variety of high-technology fields. Having obtained a number of patents based on their own extensive research and development efforts, and having also had to defend themselves against hundreds of infringement claims involving invalid patents, *amici* support a strong and rational patent system.

INTRODUCTION AND SUMMARY OF ARGUMENT

The Court should decide this case on the logically antecedent, dispositive, and important basis that the written-description requirement presents a question of law, not fact. The government argues that a disappointed patent applicant may not generally present "new evidence" in court, and that a court's consideration of such evidence should not change the level of deference. Pet. Br. 11-12. But the adequacy of a patent's written description presents a question of law, not of fact, and respondent sought only to advance legal arguments concerning the adequacy of various portions of the patent's written description. For that reason, the district court should not have rejected respondent's submission on the ground that it was new evidence, and the Federal Circuit should not have held that consideration of the new submission would implicate the level of deference to

---

[1] Petitioner has consented to the filing of this brief in a letter filed herewith. Respondent has consented in a letter on file with the Clerk. No counsel for any party authored this brief in whole or in part, and no person or entity, other than *amici* and their counsel, made a monetary contribution intended to fund the preparation or submission of this brief.

which the Patent and Trademark Office ("PTO") is entitled.

The written-description requirement's status as a legal question is more important and recurring than the administrative-law questions presented by the government. While questions of fact concerning patent validity are decided by juries under the heightened clear-and-convincing-evidence standard of proof, questions of law are decided by courts and are not governed by a heightened standard of proof.

I. Because the written-description requirement is a disclosure requirement, it turns on analysis of "the four corners of the [patent] specification . . . ." *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc). This Court has already held that interpretation of a patent specification is a "purely legal" question "exclusively within the province of the court." *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 372, 391 (1996).

The Federal Circuit appears to trace its contrary view, that interpretation of the specification is a question of fact for this purpose, to a decision of its predecessor, the Court of Customs and Patent Appeals ("CCPA"). But that decision cites nothing for the proposition, and it cannot be reconciled with this Court's precedents. Nor can it be reconciled with the Federal Circuit's own view that two related requirements—that claims be definite and that the specification enable a person skilled in the art to practice the patented invention—are questions of law. If those are questions of law, written description surely is.

II. In this case, the "new evidence" is simply legal argument concerning the content and adequacy of the patent specification, the same kind of argument that lawyers routinely make in briefs. That confirms that respondent raised purely legal issues for a court to decide, not factual issues or new "evidence."

III. The distinction between questions of law and fact is important for a number of reasons. Judges decide questions of law, while juries can decide questions of fact. And as Justice Breyer emphasized in his concurrence for three Justices in *Microsoft Corp. v. i4i Ltd. P'ship*, 131 S. Ct. 2238, 2253 (2011), the clear-and-convincing-evidence standard of proof applies only to factual determinations, not to legal conclusions.

Whether a question is a legal or factual one is especially important in patent law because juries applying the clear-and-convincing-evidence standard are extremely deferential to the PTO's issuance of a patent. By correctly distinguishing between questions of law and fact, and then "preventing the 'clear and convincing' standard from roaming outside its fact-related reservation, courts can increase the likelihood that [alleged] discoveries or inventions will not receive legal protection where none is due." *id.* (Breyer, J., concurring). Thus, the proper characterization of the written-description requirement as a question of law is necessary to prevent this Court's decision in *i4i* from extending beyond its intended reach.

The importance of the fact-law distinction is further confirmed by the importance of the written-description requirement itself. The requirement is necessary to prevent abuse, in part because patent

applicants could otherwise submit broad and vague claims and later, with the benefit of hindsight, assert that the claims cover more than the applicants had actually invented. Nonetheless, the PTO has long instructed its examiners to apply a strong presumption that all written descriptions are adequate, and to issue written-description rejections on only rare occasions. That makes it imperative for courts to review the adequacy of a written description *de novo*, lest no one do so.

ARGUMENT

I. THE ADEQUACY OF A WRITTEN DESCRIPTION PRESENTS A QUESTION OF LAW, NOT FACT.

A. The Patent Specification Itself, As Opposed To Any External Materials, Must Provide A Full And Detailed Disclosure Of The Claimed Invention.

"[A] correct specification and description of the thing discovered" is "the foundation of the power to issue the patent." *Grant v. Raymond*, 31 U.S. (6 Pet.) 218, 247 (1832). The Patent Act thus requires "a written description of the invention" in "full, clear, concise, and exact terms . . . ." 35 U.S.C. § 112, ¶ 1. To satisfy that requirement, a patent applicant must "distinguish[] in full, clear, and exact terms, the nature and extent of" the invention, so as to "put the public in possession of what the party claims as his own invention." *Evans v. Eaton*, 20 U.S. (7 Wheat.) 356, 433-34, 435 (1822).

This disclosure provision has two vitally important objectives. First, a detailed disclosure of the invention is the *quid pro quo* on which a patent

is granted: "In consideration of its disclosure and the consequent benefit to the community, the patent is granted." *United States v. Dubilier Condenser Corp.*, 289 U.S. 178, 186 (1933); *accord Bonito Boats, Inc. v. Thunder Craft Boats, Inc.*, 489 U.S. 141, 150-51 (1989).

Second, a full and detailed written description "tak[es] from the inventor the means of . . . pretending that his invention is more than what it really is." *Evans*, 20 U.S. (7 Wheat.) at 435. It provides notice of what the applicant "actually invented," *Ariad*, 598 F.3d at 1351, and demarcates "the nature and extent" of the patent right. *Evans*, 20 U.S. (7 Wheat.) at 432, 435. The patent grant is limited by the claims set forth in the patent's specification, and those claims are construed in light of the specification's written description, which provides "the single best guide to the meaning of a disputed [claim] term." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed. Cir. 2005) (en banc) (quotation marks and citation omitted). Because "clarity is essential to promote progress" and "enable[] efficient investment in innovation," a full and detailed written description is critical to clarify the meaning of otherwise ambiguous claim language. *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 535 U.S. 722, 730-31 (2002) (citation omitted). *See also* pp. 23-25, *infra*.

The written-description requirement serves its important functions by providing that "the patent . . . cannot be enlarged by claims in the patent not supported by the description." *Schriber-Schroth Co. v. Cleveland Trust Co.*, 305 U.S. 47, 57 (1938). As this Court has long emphasized, a patentee "can lawfully claim only what he has invented *and*

described, and if he claims more his patent is void." *O'Reilly v. Morse*, 56 U.S. (15 How.) 62, 121 (1853) (emphasis added); *accord Merrill v. Yeomans*, 94 U.S. 568, 569 (1876).

B. The Adequacy Of A Written Description Is A Question Of Law.

Because the adequacy of a patent's written description turns on the disclosure within the four corners of the specification, it presents a question of law for a court to decide, not one of fact for a jury.

1. The written-description requirement looks to the disclosure within the patent specification itself.

As explained above, the written-description requirement is a disclosure requirement. The written description's adequacy therefore turns on "the four corners of the specification . . . ." *Ariad*, 598 F.3d at 1351; *see also Schriber-Schroth*, 305 U.S. at 58-59. "[A]ctual 'possession' or reduction to practice [of the invention] outside of the specification is not enough." *Ariad*, 598 F.3d at 1352. When read from the perspective of a person skilled in the art, the specification *itself* must fully describe the claimed invention. *See Schriber-Schroth*, 305 U.S. at 58-59; *Ariad*, 598 F.3d at 1351.

In *Schriber-Schroth*, for example, the application described a combination including a *rigid* web, and this Court held that an amendment claiming the combination with a *flexible* web was invalid for lack of written description. 305 U.S. at 54-58. The Court acknowledged that a person of ordinary skill in the art might know how to use the combination with a flexible web, but it held that undisclosed knowledge

could not augment the written description. *Id.* at 58-59; *see also Gill v. Wells*, 89 U.S. 1, 27 (1874). Even drawings in the patent, though useful, may not remedy "an entire absence of description of the alleged invention . . . ." *Permutit Co. v. Graver Corp.*, 284 U.S. 52, 60 (1931) (Brandeis, J.).

In some circumstances, courts may entertain expert testimony when construing the specification, just as courts sometimes do in construing claim language. *See Mackay Radio & Telegraph Co. v. Radio Corp. of Am.*, 306 U.S. 86, 101 (1939); *see also Phillips*, 415 F.3d at 1318. The reason is that the specification must be construed from the perspective of a person of skill in the art. But expert testimony is limited to how a person skilled in the art would understand *the written description in the specification*; the background knowledge of a person skilled in the art is no substitute for an actual disclosure in the specification. *See Schriber-Schroth*, 305 U.S. at 58-59; *Winans v. N.Y. & E.R. Co.*, 62 U.S. (21 How.) 88, 100-01 (1858).[2]

---

[2] In *Mackay*, for example, the patent-in-suit described an invention for an antenna system arranged according to the so-called Abraham formula, which characterizes certain properties of antenna wires with lengths that are multiples of half wave lengths. *See* 306 U.S. at 93-94. Expert testimony was helpful to confirm the scientific truth that the Abraham formula does not extend to anything other than multiples of half wave lengths. *See id.* at 101. The Court then rejected claims that encompassed variable lengths—and thereby departed from the Abraham formula—because the four corners of the specification described only an invention conforming to the formula. *Id.* at 98-100.

2. Construing the patent specification is a question of law.

Because the written-description requirement turns on consideration of the specification, it is a question of law.

a. "The construction of written instruments is one of those things that judges often do and are likely to do better than jurors unburdened by training in exegesis." *Markman*, 517 U.S. at 388. Historically, therefore, "judges, not juries, ordinarily construed written documents" in all areas of the law. *Id.* at 381-82, 383. "[P]rofessors or mechanics cannot be received to prove to the court or jury what is the proper or legal construction of *any* instrument of writing." *Winans*, 62 U.S. (21 How.) at 100-01 (emphasis added). Thus, courts, not juries, have construed a wide variety of different types of documents, including land patents, deeds, and natural-resource leases. *See, e.g.*, *Brown v. Huger*, 62 U.S. (21 How.) 305, 318 (1858); *Maritimes & Ne. Pipeline, LLC v. Echo Easement Corridor, LLC*, 604 F.3d 44, 47 (1st Cir. 2010); *Terran v. Kaplan*, 109 F.3d 1428, 1432 (9th Cir. 1997); *Smoot v. Boise Cascade Corp.*, 942 F.2d 1408, 1411 (9th Cir. 1991); *Reese Exploration, Inc. v. Williams Natural Gas Co.*, 983 F.2d 1514, 1518 (10th Cir. 1993).

Because there is no reason to treat patent law differently from other areas of law, this Court has already held "that the construction of a patent, including terms of art within its claim, is exclusively within the province of the court." *Markman*, 517 U.S. at 372, 391. After explaining that the question before it was whether claim construction "is a matter of law reserved entirely for the court," *id.* at 372, this

Court decided to "treat[] interpretive issues as *purely legal*," *id.* at 391 (emphasis added).

The *Markman* Court noted that claim construction is a "mongrel practice" because it sometimes involves receiving expert testimony on the perspective of a person skilled in the art. *Id.* at 378. Nonetheless, the Court concluded that claim construction always falls on the law side of "the fact-law distinction," *id.* at 388; *see also id.* at 384 & n.10, in part because earlier decisions of this Court treated claim construction (and construction of the specification in general) as a question of law, *see id.* at 384, 382; *see also id.* at 387 (quoting A. Walker, Patent Laws § 75 (3d ed. 1895)). The *en banc* Federal Circuit has recognized that, under *Markman*, claim construction is a question of law. *See Cybor Corp. v. FAS Techs., Inc.*, 138 F.3d 1448, 1455-56 (Fed. Cir. 1998) (en banc).

Although *Markman* involved the construction of patent claims, its reasoning applies equally to the written-description requirement. The claims and the written description are both found in the patent's specification. *See, e.g., Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc); *Phillips*, 415 F.3d at 1315; 35 U.S.C. § 112 ("The specification shall conclude with one or more claims . . . ."). And a court undertakes the same basic task when interpreting claims or determining the adequacy of a written description: it analyzes the claims and description from the perspective of a person skilled in the art.

Putting claim construction and written description on opposite sides of the fact-law divide could lead to anomalous results. A court might find,

as a matter of law, that a claim has a certain meaning in light of the specification, only then to have the jury find, as a fact, that the specification does not describe and support the claim. *See Ariad*, 598 F.3d 1364-65 (Rader, C.J., dissenting in part) (arguing that written description and claim construction should not be out of sync). That outcome would make little sense given that the judge and jury analyzed the same specification. Thus, the *Markman* Court recognized that "construing . . . *the description* of the invention *and* specification of *claims* annexed to them" is "a question of law, to be determined by the court." *Id.* at 384 (quoting *Winans v. Denmead*, 56 U.S. (15 How.) 330, 338 (1853)) (emphases added).

b. The Federal Circuit nonetheless treats the adequacy of a written description as a question of fact. *See, e.g., Ariad*, 598 F.3d at 1351. The rationale behind that approach is unclear. It does not appear that the Federal Circuit has attempted to reconcile its approach with this Court's precedents, or to explain why it makes sense to treat written description and claim construction differently for this purpose.

The Federal Circuit appears to trace the rule to *In re Ruschig*, 379 F.2d 990 (C.C.P.A. 1967), a decision of its predecessor, the CCPA. *Ruschig*, however, cited nothing for the proposition that the adequacy of a written description "is a question of fact." *Id.* at 996. Strangely, *Ruschig* openly struggled with whether the question before it was even based on Section 112's written-description requirement. *See id.* at 995 ("we doubt that the rejection is truly based on section 112 . . ."). That

case is hardly a solid foundation for turning the question over to a jury.

A later CCPA decision held that "[t]he primary consideration is factual and depends on the nature of the invention and the amount of knowledge imparted to those skilled in the art by the disclosure." *In re Wertheim*, 541 F.2d 257, 262 (C.C.P.A. 1976) (citing *Ruschig*, 379 F.2d at 995-96). But as discussed above, the *sole* consideration is what resides within the four corners of the specification. *See* pp. 6-7, *supra*. And while the specification is construed from the perspective of a person skilled in the art, that is equally true of claim construction, which *Markman* held to be a pure question of law. Thus, the Federal Circuit's approach is based on reasoning of its predecessor that is clearly wrong and contrary to this Court's subsequent decision in *Markman*.

The Federal Circuit's treatment of the written-description requirement as a question of fact is all the more strange because that court treats two related Section 112 requirements—enablement and definiteness—as questions of law. *See Raytheon Co. v. Roper Corp.*, 724 F.2d 951, 960 n.6 (Fed. Cir. 1983) (enablement); *Exxon Research & Eng'g Co. v. United States*, 265 F.3d 1371, 1376 (Fed. Cir. 2001) (definiteness).

The Patent Act requires that the specification "enable any person skilled in the art . . . to make and use the same." 35 U.S.C. § 112, ¶ 1. Enablement turns on "whether one reasonably skilled in the art could make or use the invention from disclosures in the patent coupled with information known in the art . . . ." *United States v. Telectronics, Inc.*, 857 F.2d

778, 785 (Fed. Cir. 1988); *see also Wood v. Underhill*, 46 U.S. (5 How.) 1, 4 (1847).[3]

It makes no sense for the Federal Circuit to treat written description as a question of fact and enablement as a question of law. Indeed, Federal Circuit judges have found the distinction "inexplicable." *Anascape, Ltd. v. Nintendo of Am., Inc.*, 601 F.3d 1333, 1342 (Fed. Cir. 2010) (Gajarsa, J., concurring); *see also Ariad*, 598 F.3d at 1366 (Rader, C.J., dissenting) (emphasizing that "other related, objective inquiries that focus on the four corners of the specification such as claim construction and enablement, are questions of law").

The written-description requirement is, if anything, *less* factual than enablement. As noted above, enablement turns on "whether one reasonably skilled in the art could make or use the invention from disclosures in the patent *coupled with information known in the art* . . . ." *Telectronics*, 857 F.2d at 785 (emphasis added). For written-description purposes, however, the disclosures in the specification must suffice by themselves. *See* pp. 6-7, *supra*. Unlike written description, therefore, enablement turns on inquiries that are at least arguably factual: the content of the background knowledge of a person skilled in the art and such a person's ability to reproduce the invention. If

---

[3] This Court has compared the enablement and description requirements by explaining that, even if the specification enables an invention because a person skilled in the art would have known how to practice it, the claim would still be invalid if it "was not the invention which [the patentee] described" in the specification. *Schriber-Schroth*, 305 U.S. at 58-59; *see also Permutit*, 284 U.S. at 60.

enablement is legal, it necessarily follows that the written-description requirement is as well.

Nor is there any justification for treating the definiteness and written-description requirements differently for this purpose. Under the Patent Act, applicants must "particularly point[] out and distinctly claim[]" their inventions. 35 U.S.C. § 112, ¶ 2. "The test for definiteness is whether one skilled in the art would understand the bounds of the claim when read in light of the specification." *Miles Labs., Inc. v. Shandon, Inc.*, 997 F.2d 870, 875 (Fed. Cir. 1993). As with claim construction, courts may consider some evidence outside of the patent specification in making that determination from the perspective of a person skilled in the art, but because the question turns on construction of the claims in the specification, the Federal Circuit correctly views definiteness as being "a legal conclusion." *Exxon*, 265 F.3d at 1376. The written-description requirement is a question of law for the same reason.

c. In modern times, this Court has not specifically addressed the question whether written description is a question of law. The Court's older cases do not always distinguish expressly between written description and enablement, and some of them interpret earlier versions of the Patent Act. Nonetheless, they confirm that written description is a question of law, and also treat enablement as a question of fact.

In a classic recitation, Justice Clifford, while riding circuit, drew that clear distinction:

> Whether the patentee has described the subject-matter, or what he claims to have invented, so as to enable the public *to know*

> *what his claim is, is in general a question of law* for the court on the construction of the patent. . . . But whether he has described the invention . . . as *to enable the public to practise it from the specification, is in general a question of fact* to be determined . . . by a jury.

Forbes v. Barstow Stove Co., 9 F. Cas. 395, 401 (C.C. D. R.I. 1864) (No. 4923) (emphases added). A leading treatise adopted Justice Clifford's formulation as settled law. *See* Curtis, The Law of Patents, §§ 229, 253 (1873).

As *Forbes* reflects, this Court has characterized the sufficiency of the specification as a question of fact in enablement cases. *See, e.g.*, *Battin v. Taggert*, 58 U.S. (17 How.) 74, 85 (1854) ("It was the right of the jury to determine . . . whether the specification, including the claim, were so precise as to enable any person skilled in the structure of machines, to make the one described."); *Wood*, 46 U.S. (5 How.) at 4 (stating that "the sufficiency of the description must, in general, be a question of fact" with respect to whether it would "enable any one skilled in the art . . . to [make] and use" the invention); *Evans*, 20 U.S. (7 Wheat.) at 428, 433-34 (stating, in *dictum*, that "if there had been any dispute on this subject [enablement], it would have been [a] matter of fact for the jury").

In contrast, this Court has treated the separate written-description requirement as a question of law. Thus, in *Evans*, after the Court stated that any enablement question would have been for the jury, the Court went on to resolve a written-description objection by itself, evidently as a matter of law. *See* 20 U.S. (7 Wheat.) at 428, 433-34. In other cases

where this Court reversed for lack of written description, it again treated the question as a matter of law, at least implicitly, by conducting a *de novo* review of the issue. *See Schriber-Schroth*, 305 U.S. at 57-61; *Permutit*, 284 U.S. at 54-55; *see also O'Reilly*, 56 U.S. (15 How.) at 118-20. As *Markman* recognized, therefore, "construing . . . *the description* of the invention" is "a question of law, to be determined by the court." 517 U.S. at 384 (quoting *Winans*, 56 U.S. (15 How.) at 338 (emphasis added)).[4]

Not surprisingly, the Federal Circuit's departure from this Court's cases has come under criticism. *See* Jesse S. Keene, *Fact or Fiction: Reexamining the Written Description Doctrine's Classification as a Question of Fact*, 18 Fed. Cir. B.J. 25, 62 (2008) ("[T]he classification of written description as a question of fact appears incorrect."); Jeffrey A. Lefstin, *The Formal Structure of Patent Law and the Limits of Enablement*, 23 Berkeley Tech. L.J. 1141, 1216 n.236 (2008) ("The current 'factual' state of written description is . . . curious."); Allen N. Littman, *The Jury's Role in Determining Key Issues in Patent Cases:* Markman, Hilton Davis, *and Beyond*, 37 IDEA 207, 247 (1997) ("Whether enablement is a question of law or fact has changed throughout the history of U.S. patent law.").

---

[4] *Markman* noted that this Court had also held that the distinct question whether a patent is invalid because it was anticipated by another patent claiming the same invention is a question of fact. *See Markman*, 517 U.S. at 385-86 (discussing, *e.g.*, *Bischoff v. Wethered*, 76 U.S. (9 Wall.) 812 (1869)).

II. RESPONDENT'S "NEW EVIDENCE" IS LEGAL ARGUMENT ON THIS QUESTION OF LAW, NOT "EVIDENCE" AT ALL.

Because the written-description requirement presents a question of law for a court to decide, this case is far more straightforward than the lower courts made it out to be. The Federal Circuit correctly explained that, apart from some irrelevant preliminary discussion, respondent's declaration simply "identified portions of the specification that one of skill in the art would understand to describe the limitations challenged by the Director." Pet. App. 6a. The government has agreed with that characterization. Pet. 7; Pet. Br. 8.

In other words, respondent simply submitted a number of citations to the specification and argued that those passages adequately describe the claimed invention. *See* Pet. App. 270a-279a. That written-description "evidence" is not evidence at all; it is *legal* argument concerning the content of the specification (which, of course, is in the administrative record, *see* Pet. Br. 6). Indeed, the relevant portion of respondent's declaration consists of the same kind of argument a lawyer would make in a legal brief about the adequacy of the specification. Respondent's decision to put the arguments in a declaration changes only their form, not their substance.

Any remaining doubt should be resolved by the basic principle of law that judicial review of administrative action is a task for courts, not juries. *See, e.g.*, *Rempfer v. Sharfstein*, 583 F.3d 860, 865 (D.C. Cir. 2009); 5 U.S.C. § 706. To be sure, juries review a number of factual issues concerning the

validity of granted patents, but on those issues the parties are free to introduce new evidence during litigation. *See i4i*, 131 S. Ct. at 2249. In contrast, the record as to written description is confined to the four corners of the specification filed with the PTO, as construed by a person skilled in the art. Thus, respondent's argument here—that the agency erred in assessing the specification—is closely analogous to a classic question of judicial review of administrative action.

III. THE CORRECT CLASSIFICATION OF THE WRITTEN-DESCRIPTION REQUIREMENT IS EXCEPTIONALLY IMPORTANT.

The Court should take this opportunity to reaffirm that the adequacy of a written description is a question of law. The fact-law distinction is vitally important to patent law, and is frankly more important, and much more recurrent, than the administrative-law questions presented by the government.

A. The Question Is Properly Before This Court.

The correct treatment of written description as a question of law is properly before this Court because it is logically antecedent to the questions presented. *See Int'l Longshoremen's Ass'n v. Davis*, 476 U.S. 380, 388 (1986). The questions presented in the government's petition concern only the consideration of "new evidence," not additional supporting legal arguments. Pet. Br. (i).

The distinction is dispositive here because, when a party has preserved a legal *issue* for judicial review, it may make additional supporting

arguments to a reviewing court. *See, e.g.*, *Yee v. City of Escondido*, 503 U.S. 519, 534-35 (1992); *Interactive Gift Exp., Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1347 (Fed. Cir. 2001). There appears to be no dispute that respondent has preserved his challenge to the PTO's determination that the patent application lacks an adequate written description. *See* Pet. App. 4a. Thus, respondent should be able to advance legal arguments concerning the application's contents, regardless of whether he could submit new evidence; and the government should be able to rely on normal standards of agency deference regardless of whether the introduction of new evidence would alter them.[5]

B. The Question Is Exceptionally Important Throughout Patent Law.

Justice Breyer's concurrence for three Justices in *i4i* underscores the broad importance of the fact-law distinction. *See* 131 S. Ct. at 2253.

1. Courts decide questions of law without deference to the PTO's issuance of a patent.

a. Questions of fact may be decided by juries, but *courts* must decide questions of law. *See, e.g.*, *McDermott Int'l, Inc. v. Wilander*, 498 U.S. 337, 355-

---

[5] The government might have been able to assert that respondent's failure to timely identify specific portions of the specification before the PTO constituted a failure to properly exhaust administrative remedies. *See* http://www.uspto.gov/web/offices/pac/mpep/documents/1200_1205_02.htm#sect1205.02. Regardless of the merits of that argument, it is irrelevant to the questions presented here, which turn on whether the submission constituted "new evidence." Pet. Br. (i).

56 (1991). Thus, when the *Markman* Court held that claim construction is a question of law, it reserved that question exclusively to the court. *See Markman*, 517 U.S. at 372.

b. The fact-law distinction also determines the degree of deference accorded to the PTO and trial courts. In *i4i*, this Court held that a party challenging the validity of a patent must prove invalidity by clear and convincing evidence. *See* 131 S. Ct. at 2242. As Justice Breyer explained, that heightened "evidentiary standard of proof applies to questions of fact and not to questions of law." *Id.* at 2253 (Breyer, J., concurring). Thus, it has no bearing on "how the law applied to facts as given." *Id.* And as Justice Breyer specified, that conclusion encompasses the question underlying this case, which is whether the facts "show that the patent applicant described his claims properly." *Id.* (citing 35 U.S.C. § 112).

The Federal Circuit has likewise found it "inappropriate to speak in terms of a particular standard of proof being necessary to reach a legal conclusion." *SSIH Equip. S.A. v. ITC*, 718 F.2d 365, 375 (Fed. Cir. 1983). "Standard of proof relates to specific factual questions. While undoubtedly certain facts in patent litigation must be proved by clear and convincing evidence, the formulation of a legal conclusion on validity from the established facts is a matter reserved for the court." *Id.* at 100-01 (citation omitted); *see also Newell Cos., Inc. v. Kenney Mfg. Co.*, 864 F.2d 757, 767 (Fed. Cir. 1989).

That conclusion is correct because standards of proof "instruct the *factfinder* concerning the degree of confidence our society thinks he should have in the

correctness of *factual* conclusions for a particular type of adjudication." *Addington v. Texas*, 441 U.S. 418, 423 (1979) (quoting *In re Winship*, 397 U.S. 358, 370 (1970) (Harlan, J., concurring)) (emphases added). As its name suggests, therefore, "a standard of proof [does not apply] to a purely legal question [such as] whether a statute is facially unconstitutional." *Branson Sch. Dist. RE82 v. Romer*, 161 F.3d 619, 636 n.15 (10th Cir. 1998).

Nor does it apply to conclusions of law that turn in part on underlying findings of fact. In patent cases where the underlying facts were not in dispute, this Court has routinely held patents invalid as a matter of law, without even mentioning the clear-and-convincing-evidence standard. *See, e.g.*, *i4i*, 131 S. Ct. at 2253 (Breyer, J., concurring) (citing cases). Numerous courts have similarly held, for example, that "[a] standard of proof, whether beyond a reasonable doubt or some other, simply has no application to the legal question whether a given statement is material," even though materiality depends on the factual context. *United States v. Hausmann*, 711 F.2d 615, 617 (5th Cir. 1983); *accord, e.g.*, *United States v. Farnham*, 791 F.2d 331, 334 (4th Cir. 1986); *United States v. Giacalone*, 587 F.2d 5, 7 (6th Cir. 1978).[6]

---

[6] When a question of law turns on subsidiary questions of fact that are determined by a jury, district courts "can help to keep the application of [the] 'clear and convincing' standard within its proper legal bounds" by means such as "interrogatories and special verdicts to make clear which specific factual findings underlie the jury's conclusions." *i4i*, 131 S. Ct. at 2253 (Breyer, J., concurring). This Court, the regional circuits, and commentators have all strongly encouraged or required that

c. Choosing the appropriate decisionmaker and level of deference is extremely important in patent cases. "Jurors are notoriously reluctant to second-guess patent examiners," even apart from the clear-and-convincing-evidence standard. Mark A. Lemley, *Rational Ignorance at the Patent Office*, 95 Nw. U. L. Rev. 1495, 1528 (2001). That standard can often dictate the outcome because "it is very difficult to ever make the evidence 'clear and convincing' to a group of people who do not have the necessary training and education to understand it." Adam B. Jaffe & Josh Lerner, Innovation and Its Discontents 1, 196 (2004).

Accused infringers therefore face an uphill battle on factual invalidity defenses. "By preventing the 'clear and convincing' standard from roaming outside its fact-related reservation," however, "courts can increase the likelihood that [alleged] discoveries or inventions will not receive legal protection where none is due." *i4i*, 131 S. Ct. at 2253 (Breyer, J., concurring). That is important because, as this

---

practice. *See, e.g.*, *Warner-Jenkinson Co. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 38 n.8 (1997); *Dual Mfg. & Eng'g, Inc. v. Burris Indus., Inc.*, 619 F.2d 660, 667 (7th Cir. 1980) (en banc); *Baumstimler v. Rankin*, 677 F.2d 1061, 1071 (5th Cir. 1982); *Mfg. Research Corp. v. Graybar Elec. Co.*, 679 F.2d 1355, 1364 n.19 (11th Cir. 1982); *Saturn Mfg., Inc. v. Williams Patent Crusher & Pulverizer Co.*, 713 F.2d 1347, 1352 (8th Cir. 1983); Kimberly Moore, *Juries, Patent Cases, & a Lack of Transparency*, 39 Hous. L. Rev. 779 (2002). The Federal Circuit has also determined that special interrogatories "should" be used, *Am. Hoist & Derrick Co. v. Sowa & Sons, Inc.*, 725 F.2d 1350, 1361 (Fed. Cir. 1984); *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1547 (Fed. Cir. 1983), but has held that they are not required, *see Spectralytics, Inc. v. Cordis Corp.*, Nos. 2009-1564, 2010-1004 (Fed. Cir. June 13, 2011).

Court has repeatedly recognized, invalid patents "stifle, rather than promote, the progress of useful arts." *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 427 (2007); *accord Lear, Inc. v. Adkins*, 395 U.S. 653, 656 (1969). Indeed, the patent system stimulates innovation by "not granting monopolies over procedures that others would discover by independent, creative application of general principles." *Bilski v. Kappos*, 130 S. Ct. 3218, 3228 (2010).

In *i4i*, this Court held that the wisdom behind the heightened standard of proof is best left to Congress. *See* 131 S. Ct. at 2251-52. For the same reason, there is no warrant for courts to *expand* the reach of that evidentiary standard by applying it to matters that are properly viewed as legal. Any such expansion would be Congress's prerogative, not the courts'.

d. The fact-law distinction is also important to *when* a question is decided. Following this Court's holding that claim construction is a question of law, courts now routinely hold *Markman* hearings to resolve claim construction disputes *before* trial. *See, e.g., O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co., Ltd.*, 521 F.3d 1351, 1359, 1361 (Fed. Cir. 2008). Defendants with meritorious written-description claims should similarly be able to nip those suits in the bud without having to wade through discovery and trial on all other issues in the case.

The soaring costs of patent litigation—which average $5 million in cases where plaintiffs seek more than $25 million in damages and $2.5 million for lesser damages demands—make efficient resolution of meritorious defenses especially

important. *See* AIPLA, Report of the Economic Survey 2011, 35. Discovery costs have become a powerful incentive for some patent plaintiffs to file strike suits for quick settlements. *See Eon-Net LP v. Flagstar Bancorp*, __ F.3d __, 2011 WL 3211512, *10-11 (Fed. Cir. 2011). By clarifying that the written-description requirement presents a question of law, this Court would enable judges to resolve that question at a relatively early stage in the litigation, saving defendants millions of dollars in litigation costs, deterring nuisance suits, and conserving scarce judicial resources.

2. Judicial review of the adequacy of a written description is especially important.

As discussed above, the written-description requirement is an essential bulwark against overreaching by patent applicants. *See* pp. 4-6, *supra*. Among other things, a full and detailed written description prevents applicants from filing applications that describe their inventions in only general terms while leaving key aspects ambiguous, so that, with the benefit of hindsight, the applicants could later assert that their patents cover more than they actually invented. *See* FTC, *The Evolving IP Marketplace: Aligning Patent Notice and Remedies with Competition*, Executive Summary, 15 (2011), http://www.ftc.gov/os/2011/03/110307patentreport.pdf ("FTC Report"); Mark A. Lemley & Kimberly A. Moore, *Ending Abuse of Patent Continuations* 13-16 (George Mason Univ. Sch. of Law, Law & Econ. Research Paper No. 03-52, 2003), *available at* http://ssrn.com/ abstract=462404.

Even with the written-description requirement on the books, such patents have become an enormous problem in the computer and communications industries. Consider, for example, "flowchart patents." Such patents do no more than present a breakdown of logic-centered processes in functional terms, with more concrete implementation left undetailed. In other words, they provide "a conceptualization of the goals of the program . . . [and] an early phase in the development of a software system." *Lotus Dev. Corp. v. Paperback Software Int'l*, 740 F. Supp. 37, 44-45 (D. Mass. 1990) (quoting Stephen Breyer, The Uneasy Case for Copyright: A Study of Copyright in Books, Photocopies, and Computer Programs, 84 Harv. L. Rev. 281, 341 n.235 (1970)). But they do not describe how to actually implement a solution. *Cf. In re Aoyama*, __ F.3d __, 2011 WL 3796243, *4, *6 (Fed. Cir. Aug. 29, 2011) (affirming the PTO's rejection of patent claims where flowchart disclosure provided insufficient structure).

Because they are easy to churn out, flowchart patents have become a big business with perverse results: easy brainstorming of ideas produces patents that impose a massive tax on enterprises that undertake the effort and investment required to invent ways of actually implementing those ideas. *See, e.g.*, Nathan Myhrvold, *Funding Eureka!*, Harv. Bus. Rev., Mar. 2010, at 7-8, *available at* https://archive.harvardbusiness.org/cla/web/pl/product.seam?c=3113&i=3115&cs=d2136ad4c8a573ff049df550a22fdeeb (discussing "invention sessions" to produce such patents).

Such patents fail the written-description requirement because they do not provide a full and

detailed description of the invention; instead, they leave the actual inventing to someone else, who the patentee will then sue for infringement. *See Ariad*, 598 F.3d at 1353 (holding invalid for lack of written descripiton "claims [that] merely recite a description of the problem to be solved while claiming all solutions to it . . . leaving it to the [relevant] industry to complete an unfinished invention"). Without a full and detailed description of the computer and algorithm that would implement a flowchart patent, the general, abstract terms of such patents threaten to exclude the public from far more than their practical contribution to usable technology. *See, e.g.*, FTC Report at 100.

Such patents have nonetheless proliferated, in part because the PTO's manual for patent examination procedures requires examiners to afford "a strong presumption that an adequate written description of the claimed invention is present." MPEP § 2163. The manual goes on to emphasize that the presumption is nearly unrebuttable: the PTO officially expects written-description rejections to be "rare." *Id.* And they have been. Dennis Crouch, *An Empirical Study of the Role of the Written Description Requirement in Patent Prosecution* 2 (Univ. of Mo. Sch. of Law Legal Studies Research Paper No. 2010-06, 2010), *available at* http://ssrn.com/abstract=1554949.

As a result, "serious § 112 analysis is left for litigation." R. Polk Wagner, *Understanding Patent-Quality Mechanisms*, 157 U. Pa. L. Rev. 2135, 2150 (2009). That makes judicial review of the adequacy of a written description, unencumbered by the clear-and-convincing-evidence standard of proof, essential

to ensure that *someone* meaningfully enforces the requirement.[7]

CONCLUSION

For the foregoing reasons, this Court should make clear that the adequacy of a patent's written description is a question of law.

---

[7] The PTO recently released supplemental guidelines under which an examiner must reject a claim for lack of written description if the application does not describe the computer and algorithm that perform the claimed function. *See* Supplementary Examination Guidelines for Determining Compliance With 35 U.S.C. § 112 and for Treatment of Related Issues in Patent Applications 7162, 7170-71 (Feb. 9, 2011). While that supplemental guidance confirms the importance of the issue, it covers only a subset of patent applications and does not address the perhaps two million unexpired patents that were issued under the PTO's older regime. Thus, it remains imperative that courts review written-description issues *de novo*, lest no one do so.

Respectfully submitted,

DARYL JOSEFFER
Counsel of Record
ADAM CONRAD
KING & SPALDING LLP
1700 Pennsylvania Ave., N.W.
Washington, D.C. 20006
(202) 737-0500
Counsel for Amici Curiae

JOHN THORNE
GAIL F. LEVINE
VERIZON
COMMUNICATIONS INC.
1320 North Courthouse Road
Arlington, VA 22201
(703) 351-3900
Counsel for Verizon Communications Inc.

PAUL H. ROEDER
HEWLETT-PACKARD CO.
3000 Hanover Street
Palo Alto, CA 94304-1112
(650) 857-5459
Counsel for Hewlett-Packard Co.

September 6, 2011